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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572ecvjaule

- Three inbound windows plus a configuration window on PCI Express
 - Four inbound windows plus a default window on Serial RapidIO®
 - Four outbound windows plus default translation for PCI Express
 - Eight outbound windows plus default translation for Serial RapidIO with segmentation and sub-segmentation support
- Two 64-bit DDR2/DDR3 memory controllers
 - Programmable timing supporting DDR2 and DDR3 SDRAM
 - 64-bit data interface per controller
 - Four banks of memory supported, each up to 4 Gbytes, for a maximum of 16 Gbytes per controller
 - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
 - Full ECC support
 - Page mode support
 - Up to 32 simultaneous open pages for DDR2 or DDR3
 - Contiguous or discontiguous memory mapping
 - Cache line, page, bank, and super-bank interleaving between memory controllers
 - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
 - Sleep mode support for self-refresh SDRAM
 - On-die termination support when using DDR2 or DDR3
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access through JTAG port
 - 1.8-V SSTL_1.8 compatible I/O
 - Support 1.5-V operation for DDR3. The detail is TBD pending on official release of appropriate industry specifications.
 - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts per processor with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high resolution timers/counters per processor that can generate interrupts
 - Supports a variety of other internal interrupt sources

- Regular expression (regex) pattern matching
 - Built-in case insensitivity, wildcard support, no pattern explosion
 - Cross-packet pattern detection
 - Fast pattern database compilation and fast incremental updates
 - 16000 patterns, each up to 128 bytes in length
 - Patterns can be split into 256 sets, each of which can contain 16 subsets
- Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
 - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
 - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
 - 8192 stateful rules
- Deflate engine
 - Supports decompression of DEFLATE compression format including zlib and gzip
 - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)
- Two Table Lookup Units (TLU)
 - Hardware-based lookup engine offloads table searches from e500 cores
 - Longest prefix match, exact match, chained hash, and flat data table formats
 - Up to 32 tables, with each table up to 16M entries
 - 32-, 64-, 96-, or 128-bit keys
- Two I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Enhanced local bus controller (eLBC)

- Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
 - Supports *RapidIO Interconnect Specification, Revision 1.2*
 - Both 1x and 4x LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto-detection of 1x- and 4x-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compliant message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox
 - Single inbound doorbell message structure
 - Facility to accept port-write messages

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8572E.

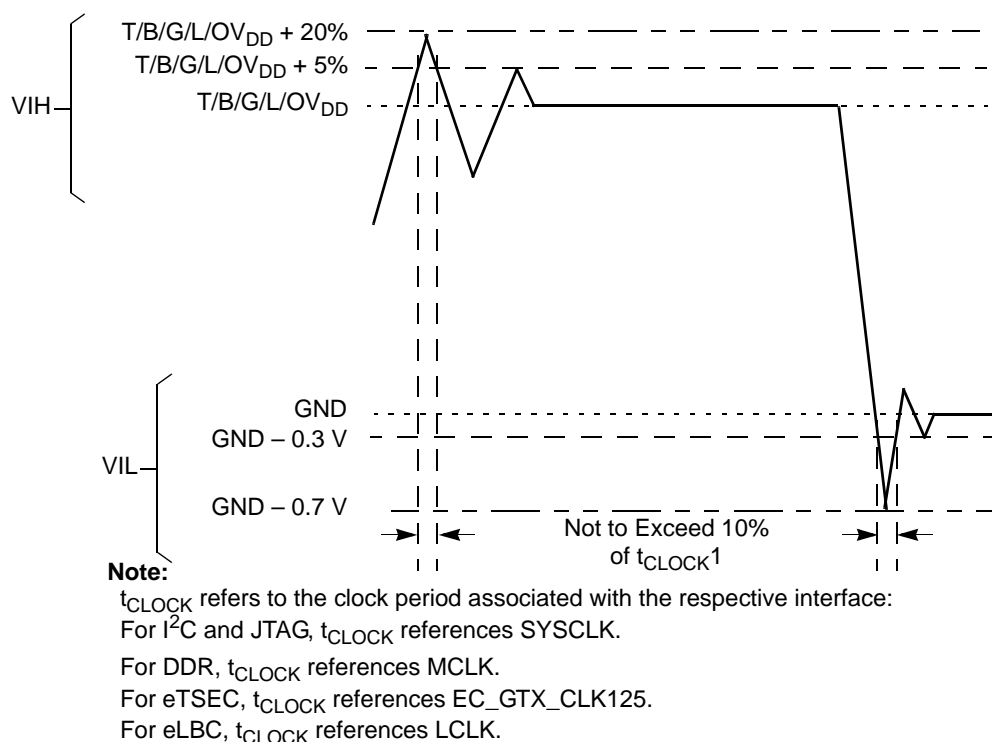


Figure 2. Overshoot/Undershoot Voltage for $TV_{DD}/BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core voltage must always be provided at nominal 1.1 V. (See Table 2 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. TV_{DD} , BV_{DD} , OV_{DD} , and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MV_{REFn} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in [Table 4](#).

Table 4. MPC8572E Power Dissipation ¹

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Notes:

¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.

² Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.

³ Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.

⁴ Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in [Table 5](#).

Table 5. MPC8572EL Power Dissipation ¹

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Notes:

¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.

² Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.

³ Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.

⁴ Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KH}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6
800 MHz		$-0.5 \times t_{MCK} - 0.375$	$-0.5 \times t_{MCK} + 0.375$		
≤ 667 MHz		$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$		
MDQS epilogue end	t_{DDKHME}			ns	6
800 MHz		-0.375	0.375		
≤ 667 MHz	t_{DDKHME}	-0.6	0.6	ns	6

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the $MCK[n]$ clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the $TIMING_CFG_2$ register. This typically be set to the same delay as in $DDR_SDRAM_CLK_CNTL[CLK_ADJUST]$. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of $MCK[n]$ at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in [Table 24](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -4.0 \text{ mA}$)	VOH	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 4.0 \text{ mA}$)	VOL	GND	0.50	V	—
Input high voltage	VIH	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	VIL	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	40	μA	1, 2,3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-600	—	μA	3

Notes:

¹ LV_{DD} supports eTSECs 1 and 2.

² TV_{DD} supports eTSECs 3 and 4 or FEC.

³ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#).

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -1.0 \text{ mA}$)	VOH	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 1.0 \text{ mA}$)	VOL	GND - 0.3	0.40	V	—
Input high voltage	VIH	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	VIL	-0.3	0.70	V	—

Table 35. RMII Transmit AC Timing Specifications (continued)

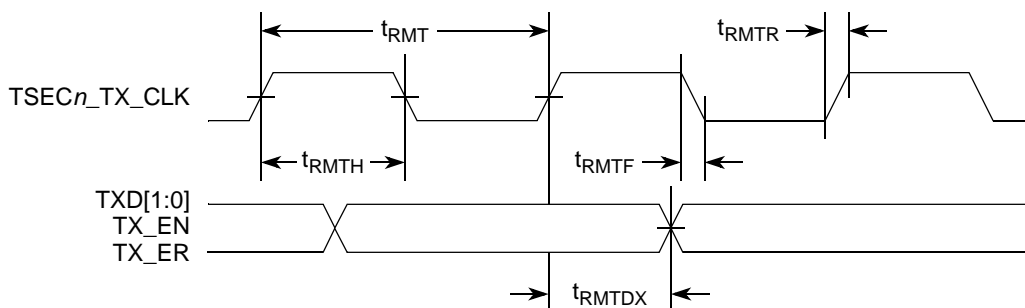
At recommended operating conditions with V_{DD}/V_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.


Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/V_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns

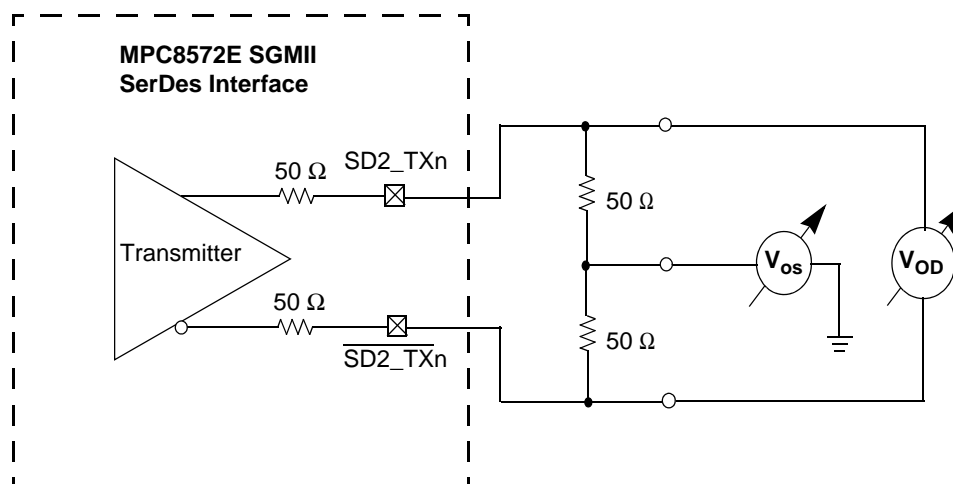


Figure 23. SGMII Transmitter DC Measurement Circuit

Table 39 lists the SGMII DC receiver electrical characteristics.

Table 39. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage		XV_{DD_SRDS2}	1.045	1.1	1.155	V	—
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 0	$V_{RX_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VLOS	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		V_{CM_ACp-p}		—	100	mV	5
Receiver differential input impedance		Z_{RX_DIFF}	80	100	120	Ω	—
Receiver common mode input impedance		Z_{RX_CM}	20	—	35	Ω	—
Common mode input voltage		V_{CM}	—	$V_{xcorevss}$	—	V	6

Note:

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTSAB or LSTSEF bit field of MPC8572E's SerDes 2 Control Register.
5. V_{CM_ACp-p} is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.4	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	6.67	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGT _A /LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LGT _A /LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LGT _A /LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4

15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND_SRDS_n (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

NOTE

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.

Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

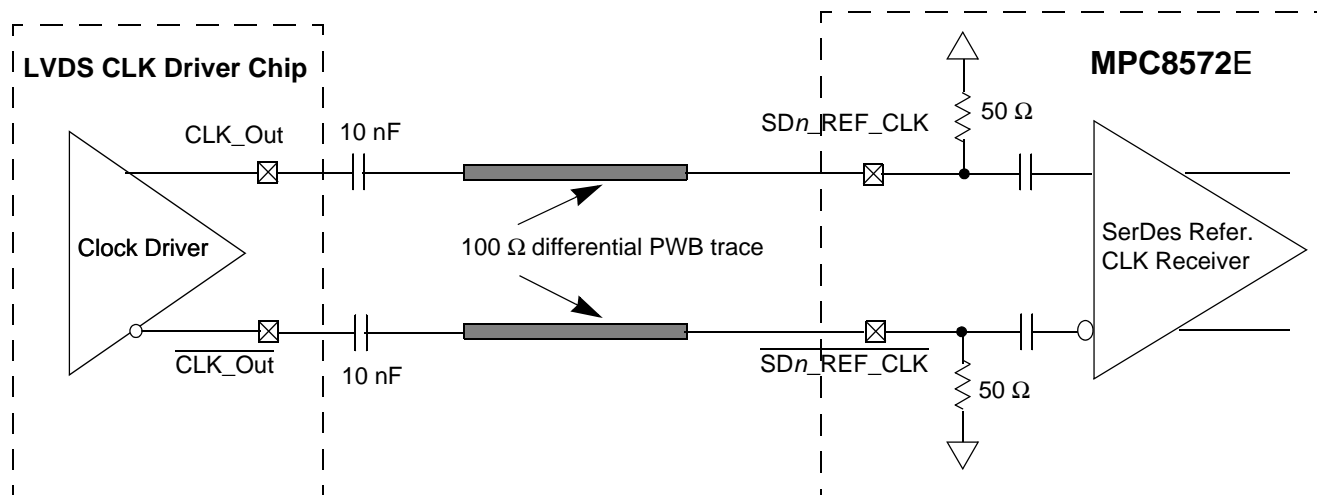


Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires $R2 = 25\Omega$. Consult

- [Section 17, “Serial RapidIO”](#)

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see [Section 15.2, “SerDes Reference Clocks.”](#)

16.2 AC Requirements for PCI Express SerDes Reference Clocks

[Table 61](#) lists AC requirements.

Table 61. SD1_REF_CLK and SD1_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:

1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

16.4.1 Differential Transmitter (TX) Output

[Table 62](#) defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

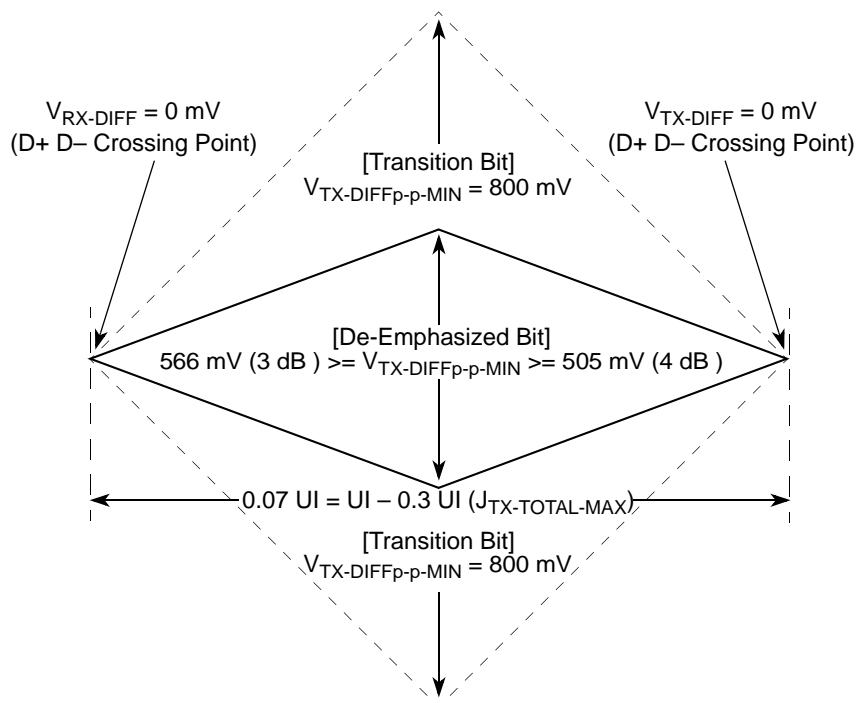


Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications

16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 63. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

Table 74. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 59](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.

18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

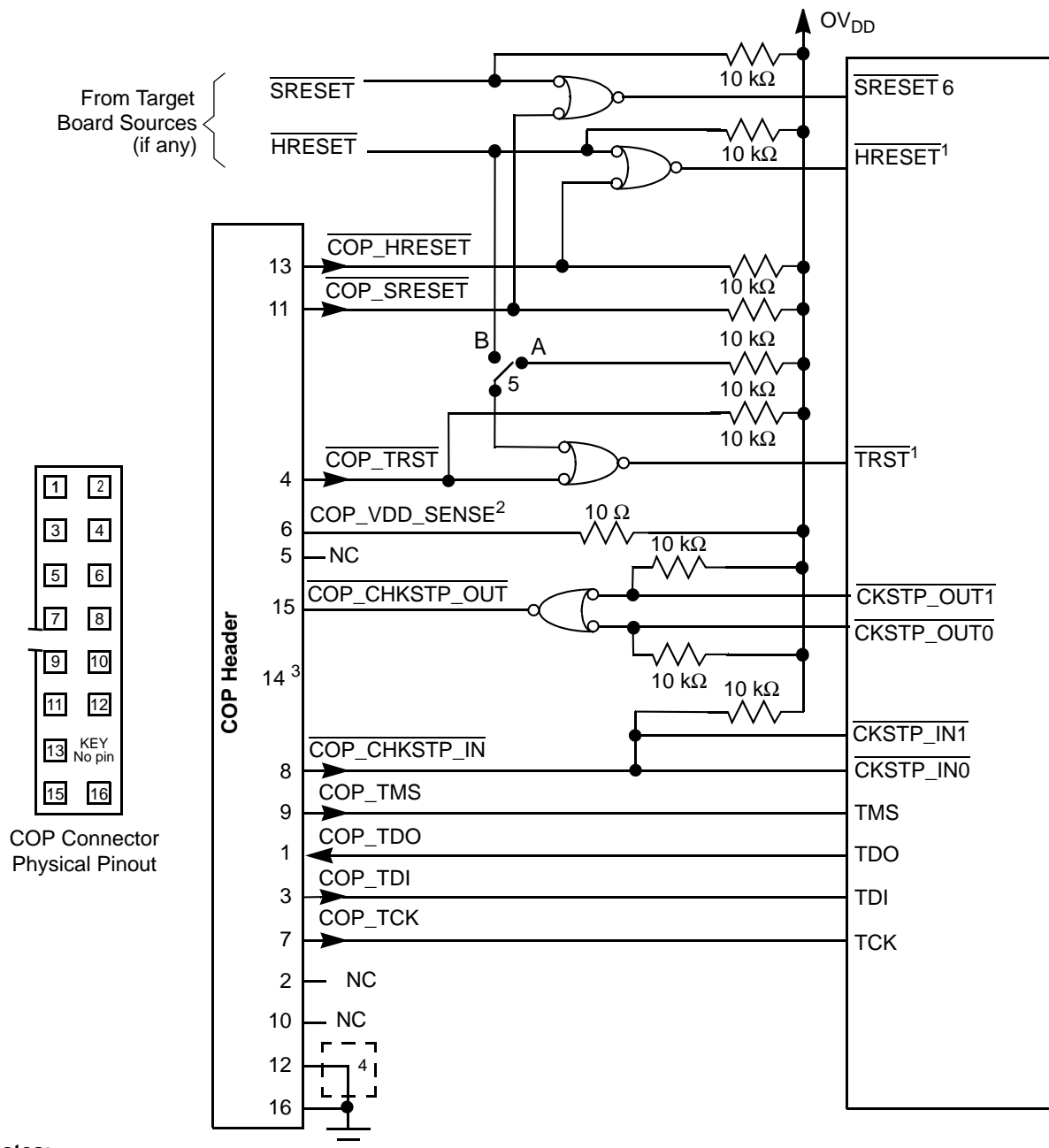
Table 76. MPC8572E Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MDQ[0:63]	Data	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17	I/O	GV _{DD}	—
D1_MECC[0:7]	Error Correcting Code	M10, M7, R8, T11, L12, L11, P9, R10	I/O	GV _{DD}	—
D1_MAPAR_ERR	Address Parity Error	P6	I	GV _{DD}	—
D1_MAPAR_OUT	Address Parity Out	W6	O	GV _{DD}	—
D1_MDM[0:8]	Data Mask	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11	O	GV _{DD}	—
D1_MDQS[0:8]	Data Strobe	A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9	I/O	GV _{DD}	—
D1_MDQS[0:8]	Data Strobe	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	GV _{DD}	—
D1_MA[0:15]	Address	Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7	O	GV _{DD}	—
D1_MBA[0:2]	Bank Select	AA7, AA8, R7	O	GV _{DD}	—
D1_MWE	Write Enable	AC12	O	GV _{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
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25. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
26. These pins should be connected to XVDD_SRDS1.
27. These pins should be pulled to ground (XGND_SRDS1) through a 300-Ω (±10%) resistor.
28. These pins should be left floating.
29. These pins should be pulled up to TVDD through a 2–10 KΩ resistor.
30. These pins have other manufacturing or debug test functions. It is recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
31. DDRCLK input is only required when the MPC8572E DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting `cfg_ddr_pll[0:2]=111`, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* Rev.0, Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
32. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
33. These pins should be pulled to ground (GND).
34. These pins are sampled at POR for General Purpose configuration use by software. Their value has no impact on the functionality of the hardware.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 cores.

Table 90. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
6	06/2014	<ul style="list-style-type: none"> Updated Table 76, “MPC8572E Pinout Listing,” TDO signal is not driven during HRSET* assertion. In Table 86, “Part Numbering Nomenclature—Rev 2.2.1,” added full Pb-free part code.
5	01/2011	<ul style="list-style-type: none"> Editorial changes throughout Updated Table 4, “MPC8572E Power Dissipation,” to include low power product. In Section 22.1, “Part Numbers Fully Addressed by this Document,” defined PPC as “Prototype” and changed table headings to say “Package Sphere Type”. Added Table 86, “Part Numbering Nomenclature—Rev 2.2.1.”
4	06/2010	<ul style="list-style-type: none"> In Section 18.3, “Pinout Listings,” updated Table 76 showing GPINOUT power rail as BVDD. Updated Section 14.1, “GPIO DC Electrical Characteristics.”
3	03/2010	<ul style="list-style-type: none"> In Section 2.1, “Overall DC Electrical Characteristics,” changed GPIO power from OVDD to BVDD. In Section 22.1, “Part Numbers Fully Addressed by this Document,” added Table 87 for Rev 2.1 silicon. In Section 22.1, “Part Numbers Fully Addressed by this Document,” updated Table 88 for Rev 1.1.1 silicon.
2	06/2009	<ul style="list-style-type: none"> In Section 3, “Power Characteristics,” updated CCB Max to 533MHz for 1200MHz core device in Table 5, “MPC8572EL Power Dissipation.” In Section 4.4, “DDR Clock Timing,” changed DDRCLK Max to 100MHz. This change was announced in Product Bulletin #13572. Clarified restrictions in Section 4.5, “Platform to eTSEC FIFO Restrictions.” In Table 9, “RESET Initialization Timing Specifications,” added note 2. Added Section 14, “GPIO.” In Section 18.1, “Package Parameters for the MPC8572E FC-PBGA,” updated material composition to 63% Sn, 37% Pb. In Section 18.2, “Mechanical Dimensions of the MPC8572E FC-PBGA,” updated Figure 61 to correct the package thickness and top view. In Section 19.1, “Clock Ranges,” updated CCB Max to 533MHz for 1200MHz core device in Table 77, “MPC8572E Processor Core Clocking Specifications.” In Section 19.5.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces,” changed minimum CCB clock frequency for proper PCI Express operation. Added LPBSE to description of LGPL4/LGTA/LUPWAIT/LPBSE/LFRB signal in Table 76, “MPC8572E Pinout Listing.” Corrected supply voltage for GPIO pins in Table 76, “MPC8572E Pinout Listing.” Applied note to SD1_PLL_TPA in Table 76, “MPC8572E Pinout Listing.” Updated note regarding MDIC in Table 76, “MPC8572E Pinout Listing.” Added note for LAD pins in Table 76, “MPC8572E Pinout Listing.” Updated Table 88, “Part Numbering Nomenclature—Rev 1.1.1” with Rev 2.0 and Rev 2.1 part number information. Added note indicating that silicon version 2.0 is available for prototype purposes only and will not be available as a qualified device.
1	08/2008	<ul style="list-style-type: none"> In Section 22.1, “Part Numbers Fully Addressed by this Document,” added SVR information in, Table 88 “Part Numbering Nomenclature—Rev 1.1.1,” for devices without Security Engine feature.
0	07/2008	<ul style="list-style-type: none"> Initial release.