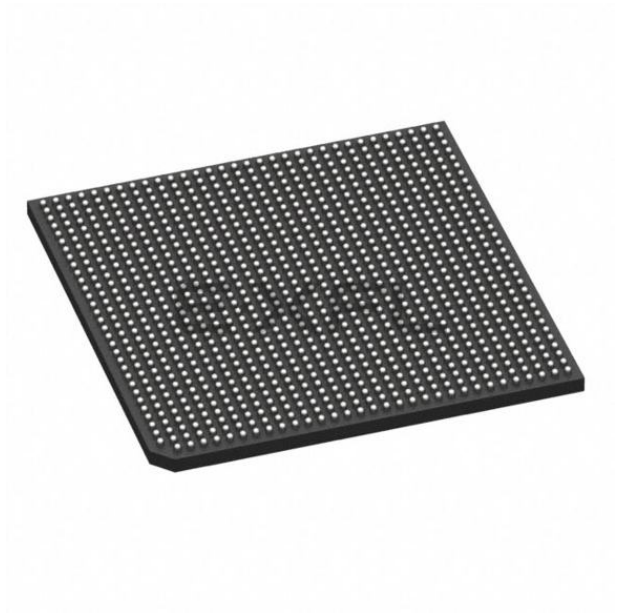

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.067GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 1023-BFBGA, FCBGA |
| Supplier Device Package | 1023-FCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572ecvtarlb |

Figure 1 shows the MPC8572E block diagram.

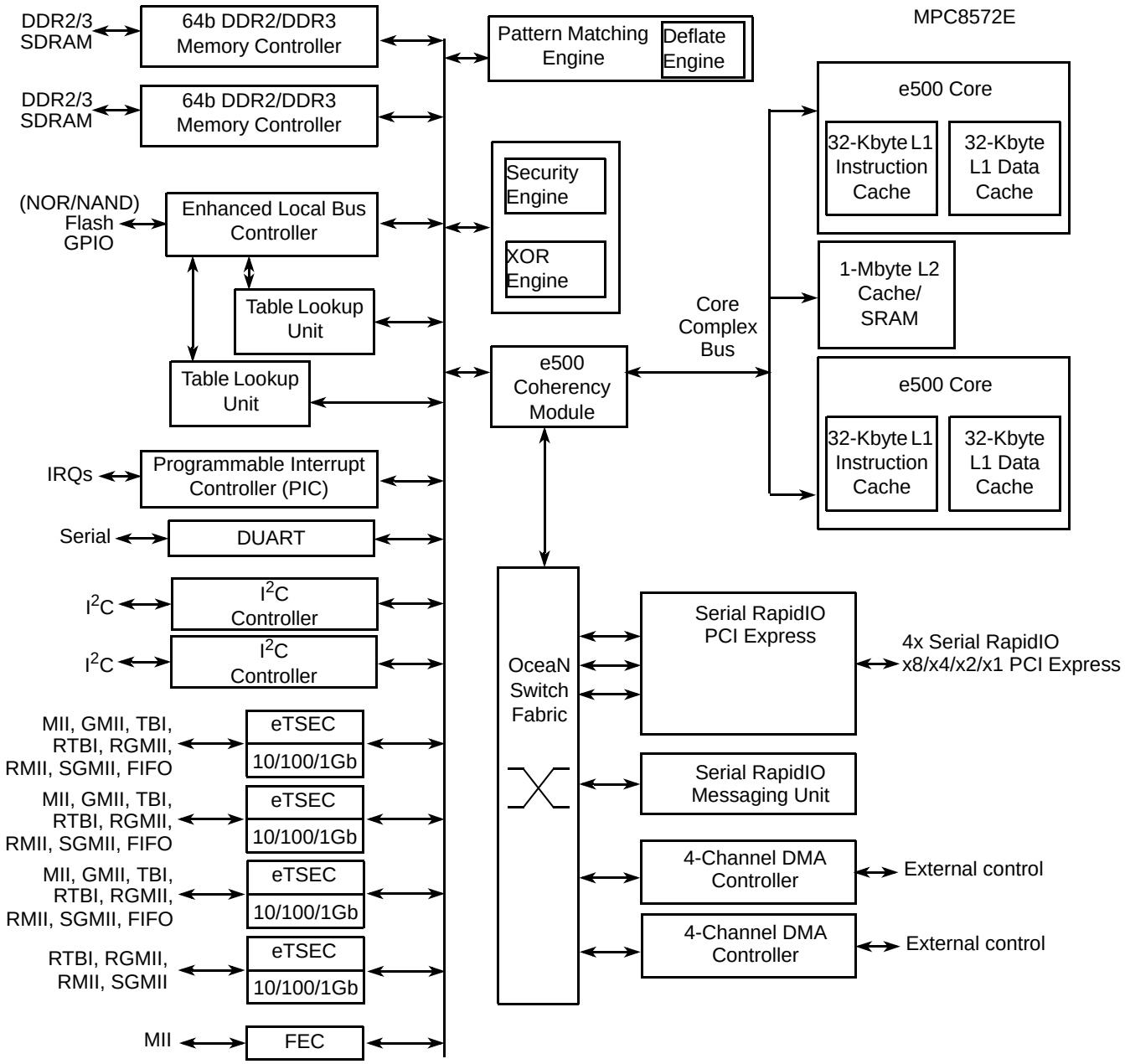


**Figure 1. MPC8572E Block Diagram**

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25<br>35 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V | 1 |
| | 45(default)<br>45(default)<br>125 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V<br>$BV_{DD}$ = 1.8 V | |
| DDR2 signal | 18<br>36 (half strength mode) | $GV_{DD}$ = 1.8 V | 2 |
| DDR3 signal | 20<br>40 (half strength mode) | $GV_{DD}$ = 1.5 V | 2 |
| eTSEC/10/100 signals | 45 | $L/TV_{DD}$ = 2.5/3.3 V | — |
| DUART, system control, JTAG | 45 | $OV_{DD}$ = 3.3 V | — |
| I2C | 150 | $OV_{DD}$ = 3.3 V | — |

**Notes:**
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j$ = 105°C and at $GV_{DD}$ (min).

## 2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. $V_{DD}$, $AV_{DD}\_n$, $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD\_SRDS1}$ and $SV_{DD\_SRDS2}$, $TV_{DD}$, $XV_{DD\_SRDS1}$ and $XV_{DD\_SRDS2}$
2. $GV_{DD}$

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for $GV_{DD}$ is not required.

Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR3 mode.

**Table 20. DDR3 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| DC Input Signal Voltage | $V_{IN}$ | — | — | mV | — |
| DC Differential Input Voltage | $V_{ID}$ | — | — | mV | — |
| AC Differential Input Voltage | $V_{IDAC}$ | — | — | mV | — |
| DC Differential Output Voltage | $V_{OH}$ | — | — | mV | — |
| AC Differential Output Voltage | $V_{OHAC}$ | — | — | mV | — |
| AC Differential Cross-point Voltage | $V_{IXAC}$ | — | — | mV | — |
| Input Midpoint Voltage | $V_{MP}$ | — | — | mV | — |

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

## 7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

**Table 21. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1.

Figure 16 shows the TBI receive AC timing diagram.

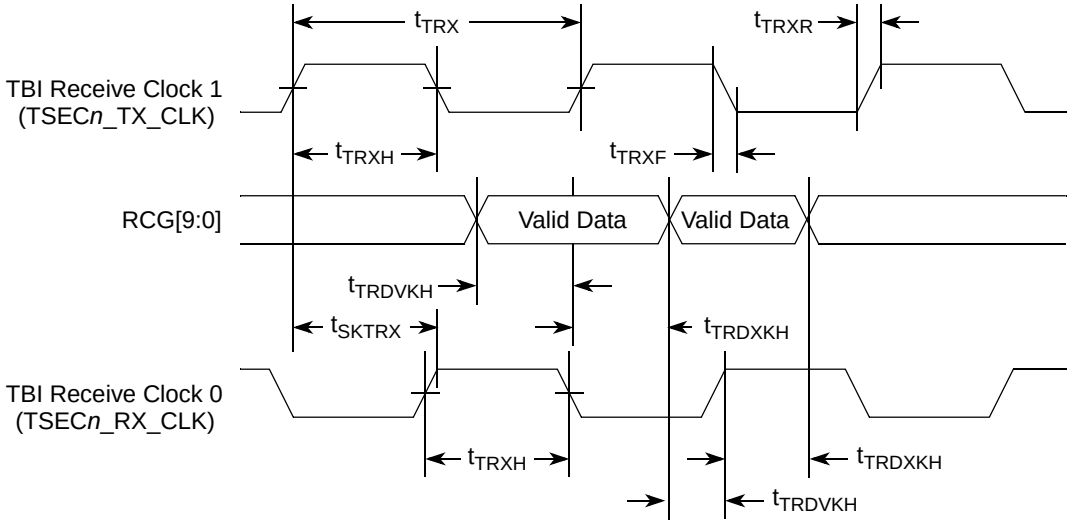


**Figure 16. TBI Receive AC Timing Diagram**

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

**Table 33. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRRX}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRRX}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

**Table 35. RMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 1.0 | — | 10.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

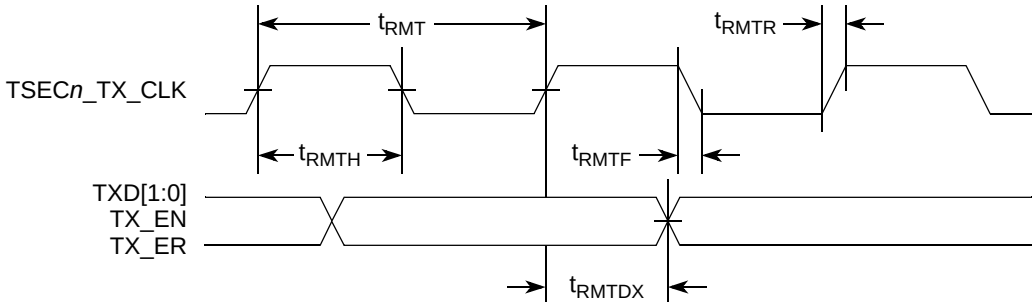


**Figure 19. RMII Transmit AC Timing Diagram**

### 8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

**Table 36. RMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_TX_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % |
| TSECn_TX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSECn_TX_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |

### 8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX[n]}}$) as depicted in Figure 23.

**Table 38. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| Output high voltage | VOH | — | — | $XV_{DD\_SRDS2-Typ}/2 + \lvert\overline{V_{OD}}\rvert_{-max}/2$ | mV | 1 |
| Output low voltage | VOL | $XV_{DD\_SRDS2-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | — |
| Output differential voltage[2, 3, 5] | $\lvert V_{OD}\rvert$ | 359 | 550 | 791 | mV | Equalization setting: 1.0x |
| | | 329 | 505 | 725 | | Equalization setting: 1.09x |
| | | 299 | 458 | 659 | | Equalization setting: 1.2x |
| | | 270 | 414 | 594 | | Equalization setting: 1.33x |
| | | 239 | 367 | 527 | | Equalization setting: 1.5x |
| | | 210 | 322 | 462 | | Equalization setting: 1.71x |
| | | 180 | 275 | 395 | | Equalization setting: 2.0x |
| Output offset voltage | $V_{OS}$ | 473 | 550 | 628 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | — |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | — |
| Change in $V_{OD}$ between “0” and “1” | $\Delta \lvert V_{OD}\rvert$ | — | — | 25 | mV | — |

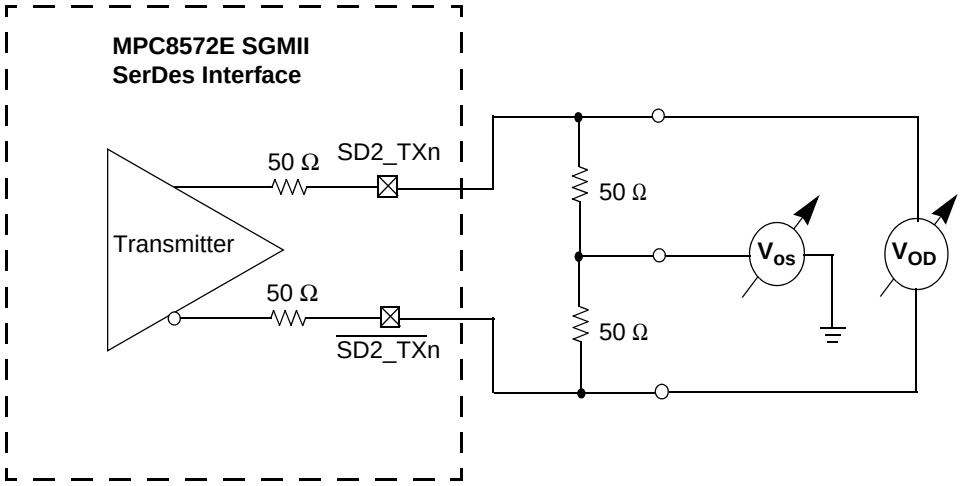


**Figure 23. SGMII Transmitter DC Measurement Circuit**

Table 39 lists the SGMII DC receiver electrical characteristics.

**Table 39. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX\_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM\_ACp-p}$ | | — | 100 | mV | 5 |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | | $Z_{RX\_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of MPC8572E's SerDes 2 Control Register.
5. $V_{CM\_ACp-p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

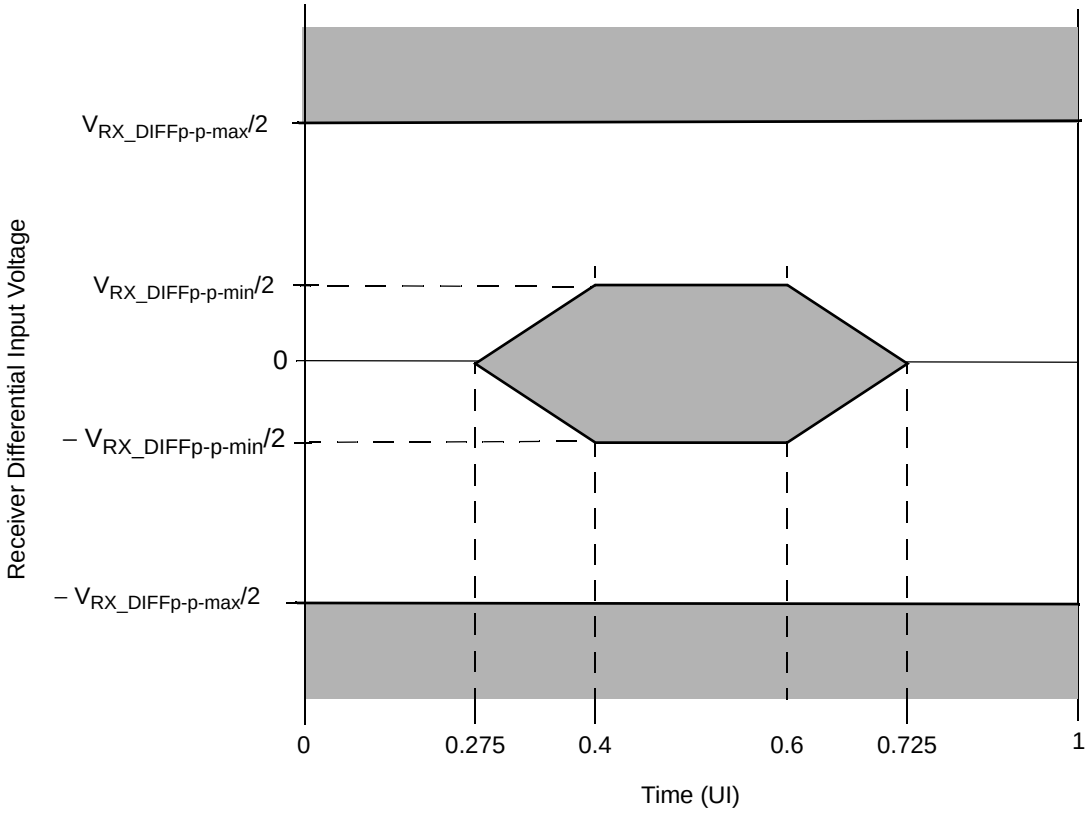


**Figure 24. SGMII Receiver Input Compliance Mask**

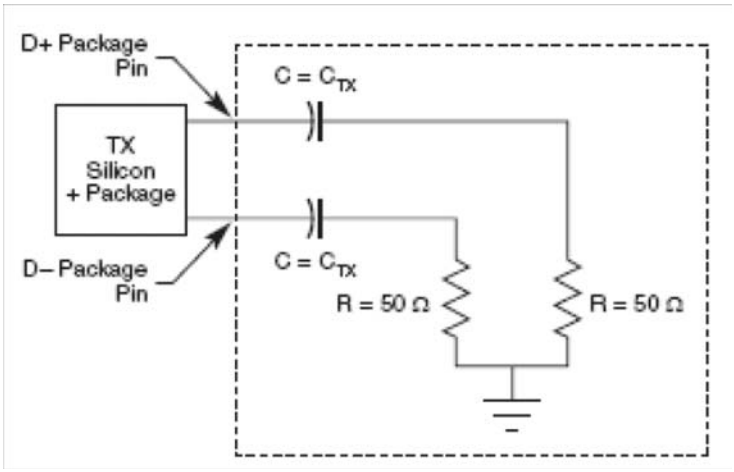


**Figure 25. SGMII AC Test/Measurement Load**

Table 48 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 48. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | 0.65 x $BV_{DD}$ | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.35 x $BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | TBD | TBD | µA |
| High-level output voltage ($I_{OH}$ = –100 µA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| High-level output voltage ($I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.45 | — | V |
| Low-level output voltage ($I_{OL}$ = 100 µA) | $V_{OL}$ | — | 0.2 | V |
| Low-level output voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.45 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 10.2 Local Bus AC Electrical Specifications

Table 49 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC.

**Table 49. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7,8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.4 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | 3 |

**Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | -1.3 | — | ns | 4, 5 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | –0.3 | ns | |
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | –0.1 | ns | 4 |
| Local bus clock to address valid for LAD | $t_{LBKLOV3}$ | — | 0.0 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0.0 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –3.3 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –3.3 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.2 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.2 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

## NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of $t_{LBKHKT}$. In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

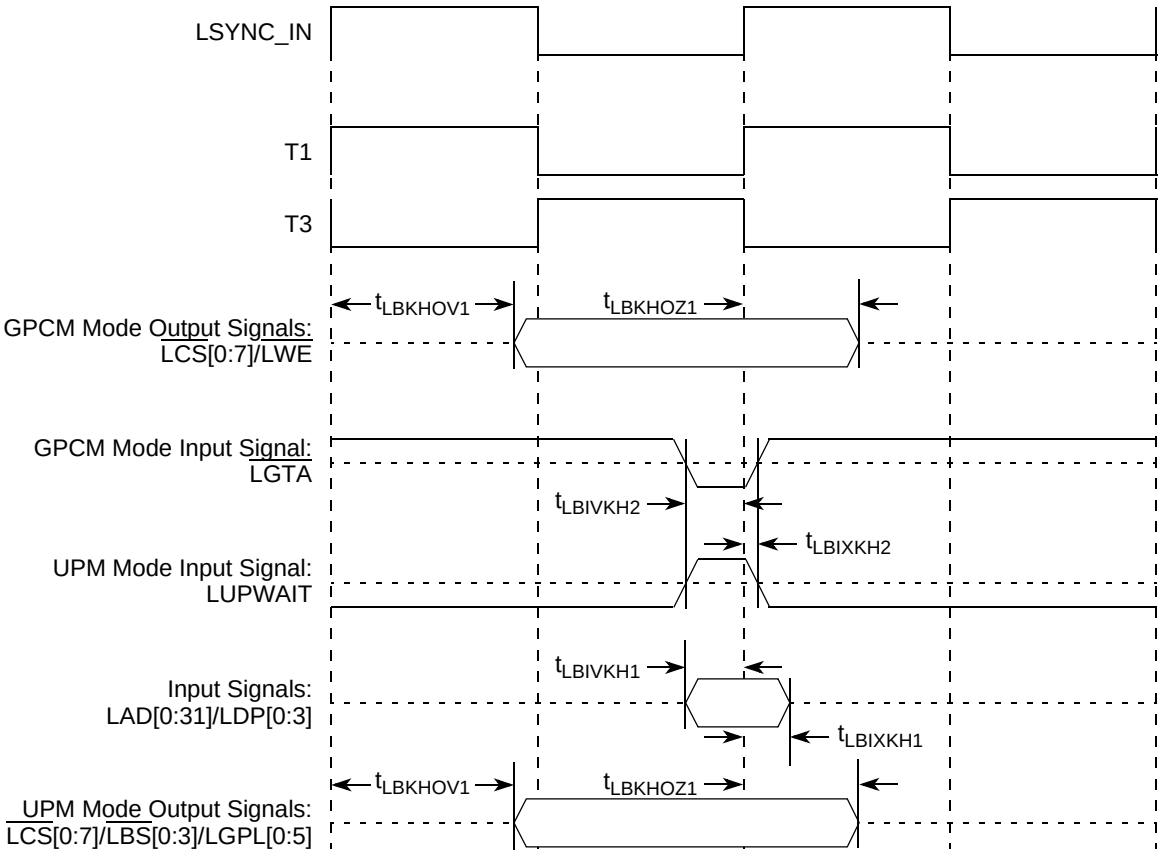


**Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)**

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.

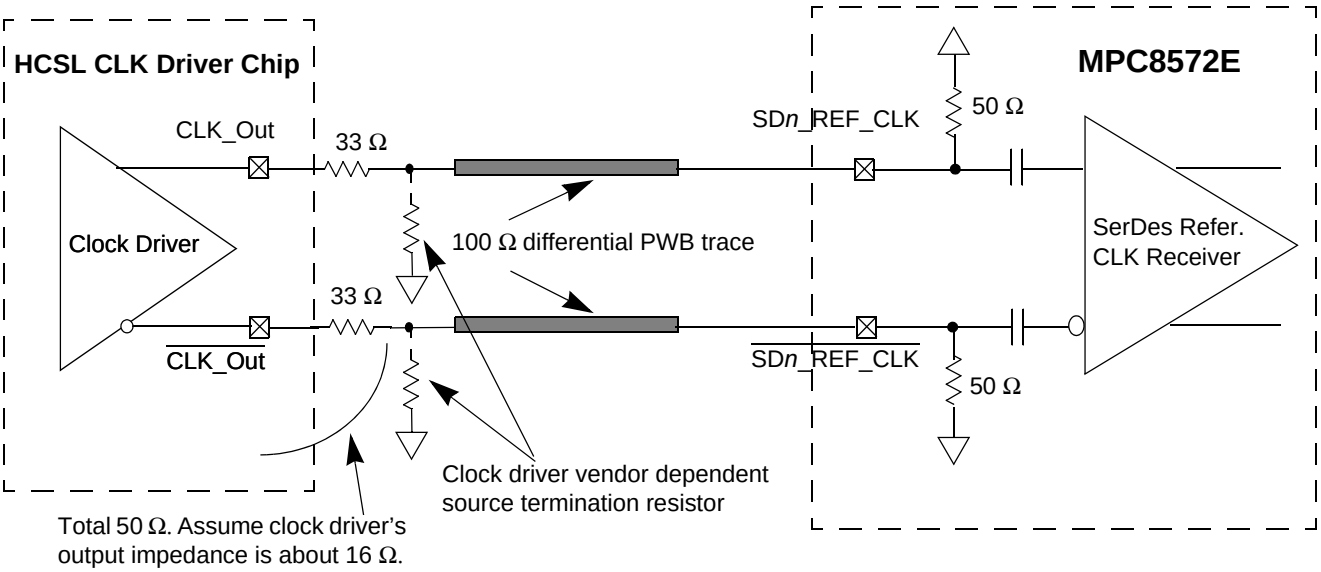


**Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

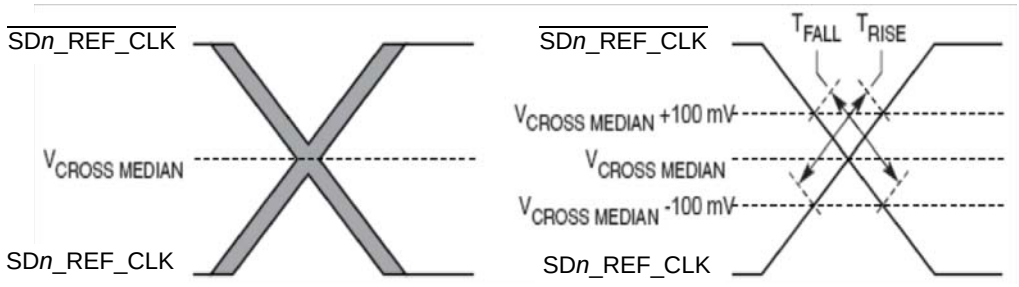


**Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$"
- Section 16.2, "AC Requirements for PCI Express SerDes Reference Clocks"
- Section 17.2, "AC Requirements for Serial RapidIO SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$"

### 15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ are designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not to be used with, and should not be clocked by, a spread spectrum clock source.

## 15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane's transmitter and receiver.

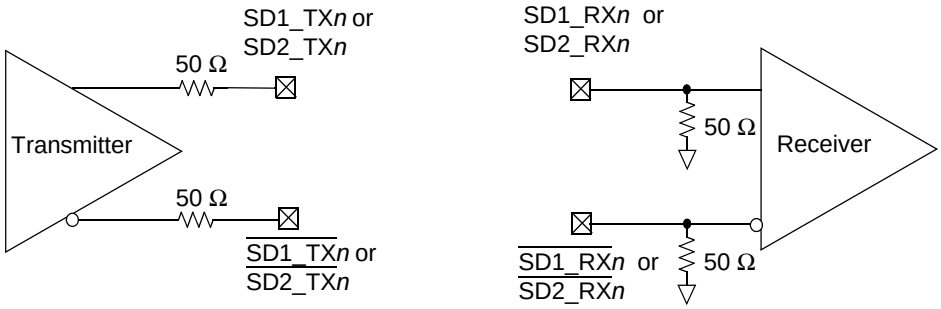


**Figure 54. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 16, "PCI Express"

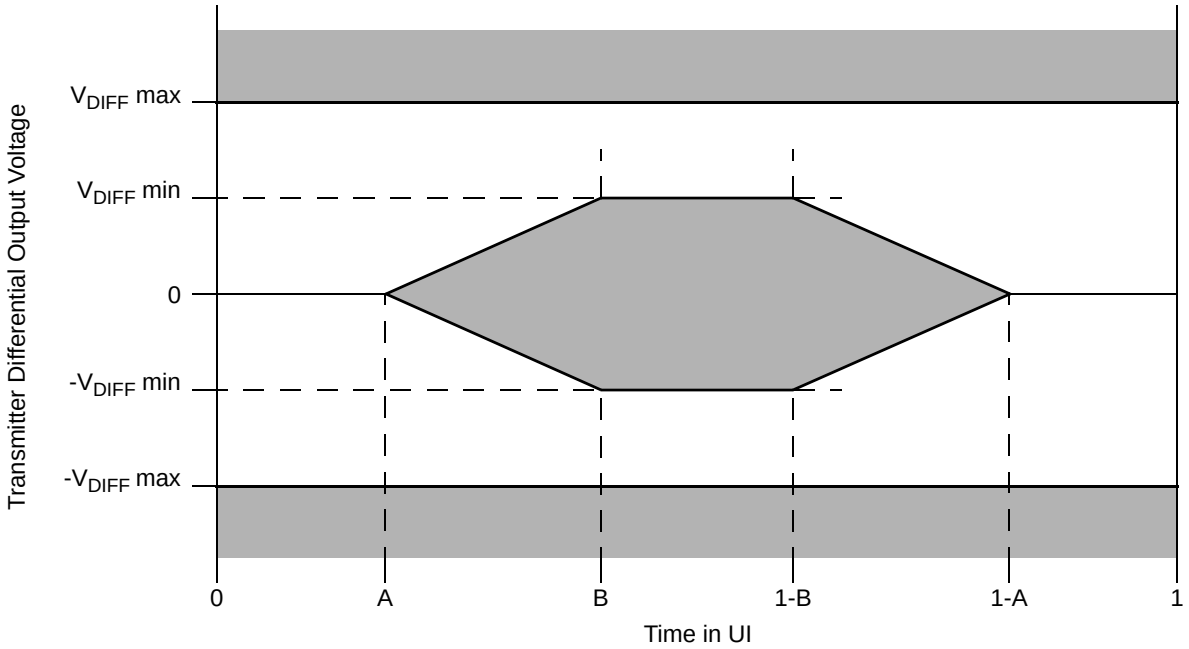


**Figure 58. Transmitter Output Compliance Mask**

**Table 71. Transmitter Differential Output Eye Diagram Parameters**

| Transmitter Type | $V_{DIFF}$min (mV) | $V_{DIFF}$max (mV) | A (UI) | B (UI) |
|---|---|---|---|---|
| 1.25 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 1.25 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 2.5 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 2.5 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 3.125 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 3.125 GBaud long range | 400 | 800 | 0.175 | 0.39 |

## 17.6 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25-Ω resistive for common mode.

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| N/C | No Connection | A16, A20, B16, B17, B19, B20, C17, C18, C19, D28, R31, T17, V23, W23, Y22, Y23, Y24, AA24, AB24, AC24, AC26, AC27, AC29, AD31, AE29, AJ25, AK28, AL31, AM21 | — | — | 17 |

**Note:**

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kO pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, “CCB/SYSCLK PLL Ratio.”
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 19.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore be described as an I/O for boundary scan.
10. If this pin is configured for local bus controller usage, recommend a weak pull-up resistor (2-10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and so on.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the VDD/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive diode.
15. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
16. This pin is only an output in FIFO mode when used as Rx Flow Control.
17. Do not connect.
18. These are test signals for factory use only and must be pulled up (100 Ω - 1 KΩ) to OVDD for normal machine operation.
19. Independent supplies derived from board VDD.
20. Recommend a pull-up resistor (~1 KΩ) be placed on this pin to OVDD.
21. The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA1\_DACK}}$[0:1], EC5_MDC, $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY_P0/QUIESCE, MSRCID[2:4], MDVAL, ASLEEP.
22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
23. This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.
24. TSEC2_TXD[1] is used as cfg_dram_type. IT MUST BE VALID AT POWER-UP, EVEN BEFORE HRESET ASSERTION.

**Table 82. DDR Clock Ratio (continued)**

| Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals | DDR:DDRCLK Ratio |
|---|---|
| 101 | 12:1 |
| 110 | 14:1 |
| 111 | Synchronous mode |

## 19.5 Frequency Options

### 19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

**Table 83. Frequency Options for Platform Frequency**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 33.33 | 41.66 | 50 | 66.66 | 83 | 100 | 111 | 133.33 |
| | Platform /CCB Frequency (MHz) | | | | | | | |
| **4** | | | | | | 400 | 444 | 533 |
| **5** | | | | | 415 | 500 | 555 | |
| 6 | | | | 400 | 498 | 600 | | |
| **8** | | | 400 | 533 | | | | |
| **10** | | 417 | 500 | | | | | |
| **12** | 400 | 500 | 600 | | | | | |

### 19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, “I/O Port Selection,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, “Link Width,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the “PCI Express link width”

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[ e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ ln\frac{I_H}{I_L} \right]$$

Where:

$I_{fw}$ = Forward current
$I_s$ = Saturation current
$V_d$ = Voltage at diode
$V_f$ = Voltage forward biased
$V_H$ = Diode voltage while $I_H$ is flowing
$V_L$ = Diode voltage while $I_L$ is flowing
$I_H$ = Larger diode bias current
$I_L$ = Smaller diode bias current
q = Charge of electron ($1.6 \times 10^{-19}$ C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant ($1.38 \times 10^{-23}$ Joules/K)
T = Temperature (Kelvins)

The ratio of $I_H$ to $I_L$ is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 85. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|
| $R_N$ | 45 Target | 18 Target (full strength mode)<br>36 Target (half strength mode) | $Z_0$ | Ω |
| $R_P$ | 45 Target | 18 Target (full strength mode)<br>36 Target (half strength mode) | $Z_0$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

## 21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

### 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

**Table 87. Part Numbering Nomenclature—Rev 2.1**

| MPC | *nnnn* | *e* | *t* | *l* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|---|

| Product Code[1] | Part Identifier | Security Engine | Temperature | Power | Package Sphere Type[2] | Processor Frequency/ DDR Data Rate[3] | Silicon Revision |
|---|---|---|---|---|---|---|---|
| MPC<br>PPC | 8572 | E = Included | Blank = 0 to 105°C<br>C = –40 to 105°C | Blank = Standard<br>L = Low | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA | AVN = 150- MHz processor; 800 MT/s DDR data rate<br><br>AUL = 1333-MHz processor; 667 MT/s DDR data rate<br><br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br><br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included |
| | | Blank = Not included | | | | | D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included |

**Notes:**

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

**Table 88. Part Numbering Nomenclature—Rev 1.1.1**

| MPC | *nnnn* | *e* | *t* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|

| Product Code[1] | Part Identifier | Security Engine | Temperature | Package Sphere Type[2] | Processor Frequency/ DDR Data Rate[3] | Silicon Revision |
|---|---|---|---|---|---|---|
| MPC<br>PPC | 8572 | E = Included | Blank=0 to 105°C<br>C= –40 to 105°C | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA | AVN = 1500-MHz processor; 800 MT/s DDR data rate<br>AUL = 1333-MHz process or; 667 MT/s DDR datarate<br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included |
| | | Blank = Not included | | | | B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included |

**Notes:**

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.