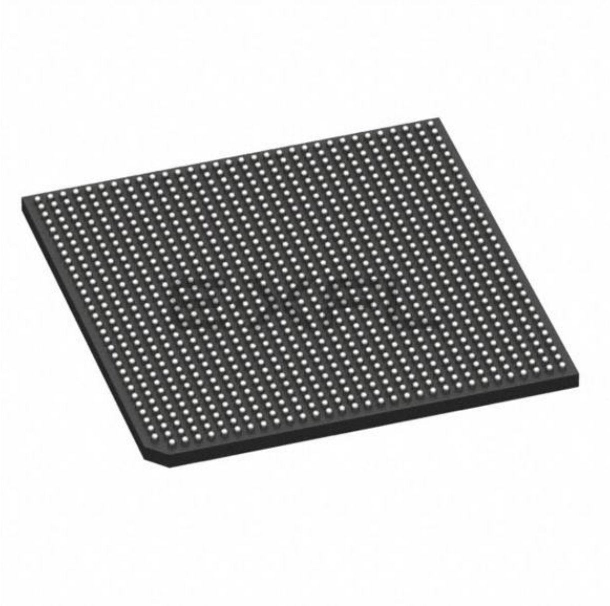

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572ecvtaulb

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
  - Shared by both cores.
  - Flexible configuration and individually configurable per core.
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and Flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be Flash cleared separately.
  - Per-way allocation of cache region to a given processor.
  - SRAM features include the following:
    - 1, 2, 4, or 8 ways can be configured as SRAM.
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
  - Twelve local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.

- Regular expression (regex) pattern matching
  - Built-in case insensitivity, wildcard support, no pattern explosion
  - Cross-packet pattern detection
  - Fast pattern database compilation and fast incremental updates
  - 16000 patterns, each up to 128 bytes in length
  - Patterns can be split into 256 sets, each of which can contain 16 subsets
- Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
  - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
  - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
  - 8192 stateful rules
- Deflate engine
  - Supports decompression of DEFLATE compression format including zlib and gzip
  - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)

• Two Table Lookup Units (TLU)
  - Hardware-based lookup engine offloads table searches from e500 cores
  - Longest prefix match, exact match, chained hash, and flat data table formats
  - Up to 32 tables, with each table up to 16M entries
  - 32-, 64-, 96-, or 128-bit keys

• Two I^{2}C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^{2}C mode support
  - On-chip digital filtering rejects spikes on the bus

• Boot sequencer
  - Optionally loads configuration data from serial ROM at reset the I^{2}C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^{2}C addressing mode
  - Data integrity checked with preamble signature and CRC

• DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D

• Enhanced local bus controller (eLBC)

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5, 6

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:

1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 8.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

Figure 14 shows the MII receive AC timing diagram.

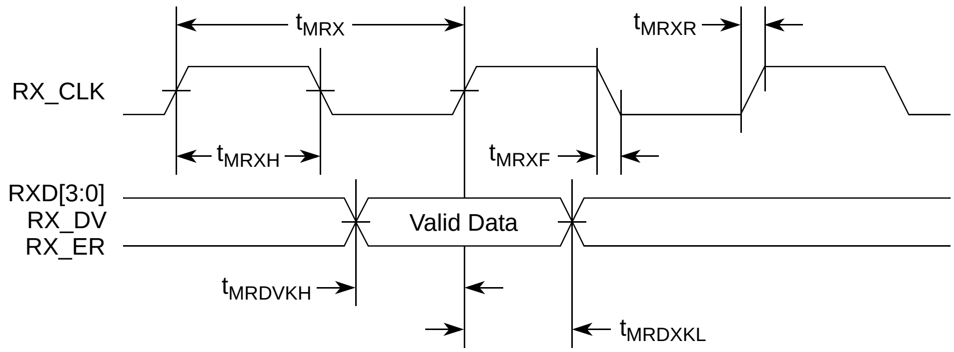

Figure 14. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

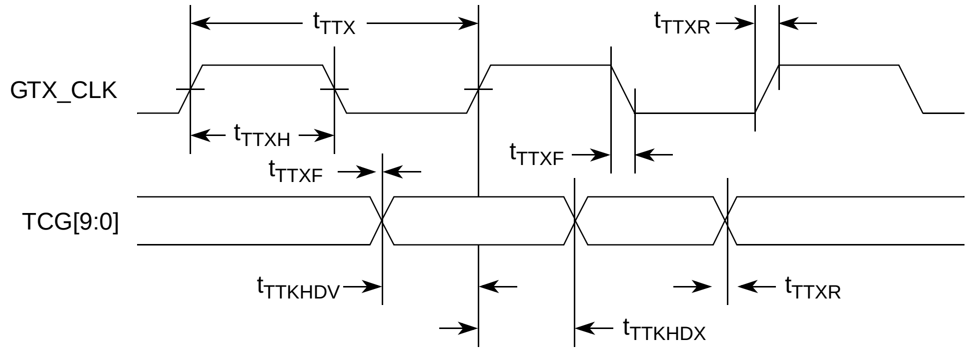

Figure 15. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition [3]	Symbol [1]	Min	Typ	Max	Unit
Clock period for TBI Receive Clock 0, 1	t_{TRX}	—	16.0	—	ns
Skew for TBI Receive Clock 0, 1	t_{SKTRX}	7.5	—	8.5	ns
Duty cycle for TBI Receive Clock 0, 1	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1	t_{TRDXKH}	1.5	—	—	ns
Clock rise time (20%-80%) for TBI Receive Clock 0, 1	t_{TRXR} [2]	0.7	—	2.4	ns
Clock fall time (80%-20%) for TBI Receive Clock 0, 1	t_{TRXF} [2]	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. The signals "TBI Receive Clock 0" and "TBI Receive Clock 1" refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

Figure 30 through Figure 35 show the local bus signals.

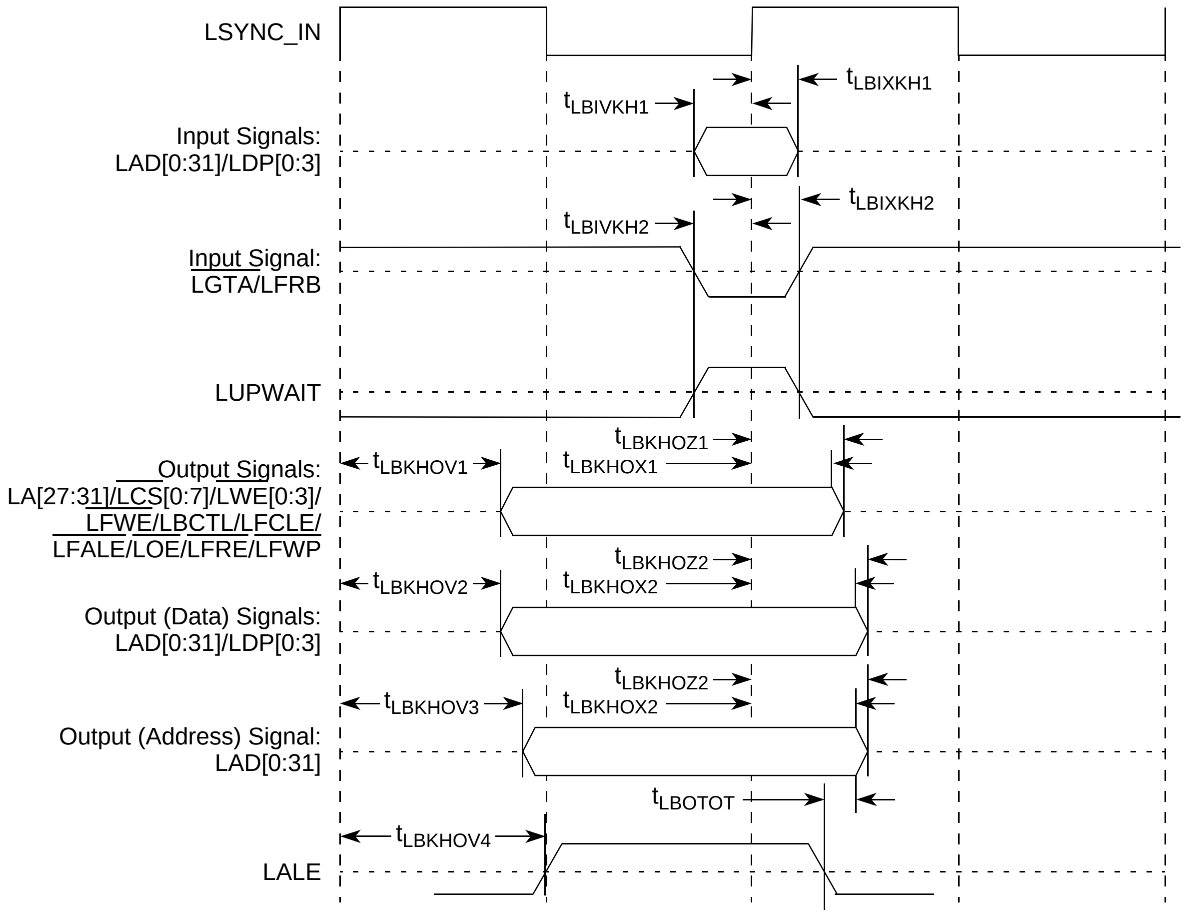

Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

Table 52 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC with PLL disabled.

Table 52. Local Bus General Timing Parameters—PLL Bypassed

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.0	ns	—
Input setup to local bus clock (except LGTA/LUPWAIT)	$t_{LBIVKH1}$	5.8	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.7	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	$t_{LBIXKH1}$	-1.3	—	ns	4, 5

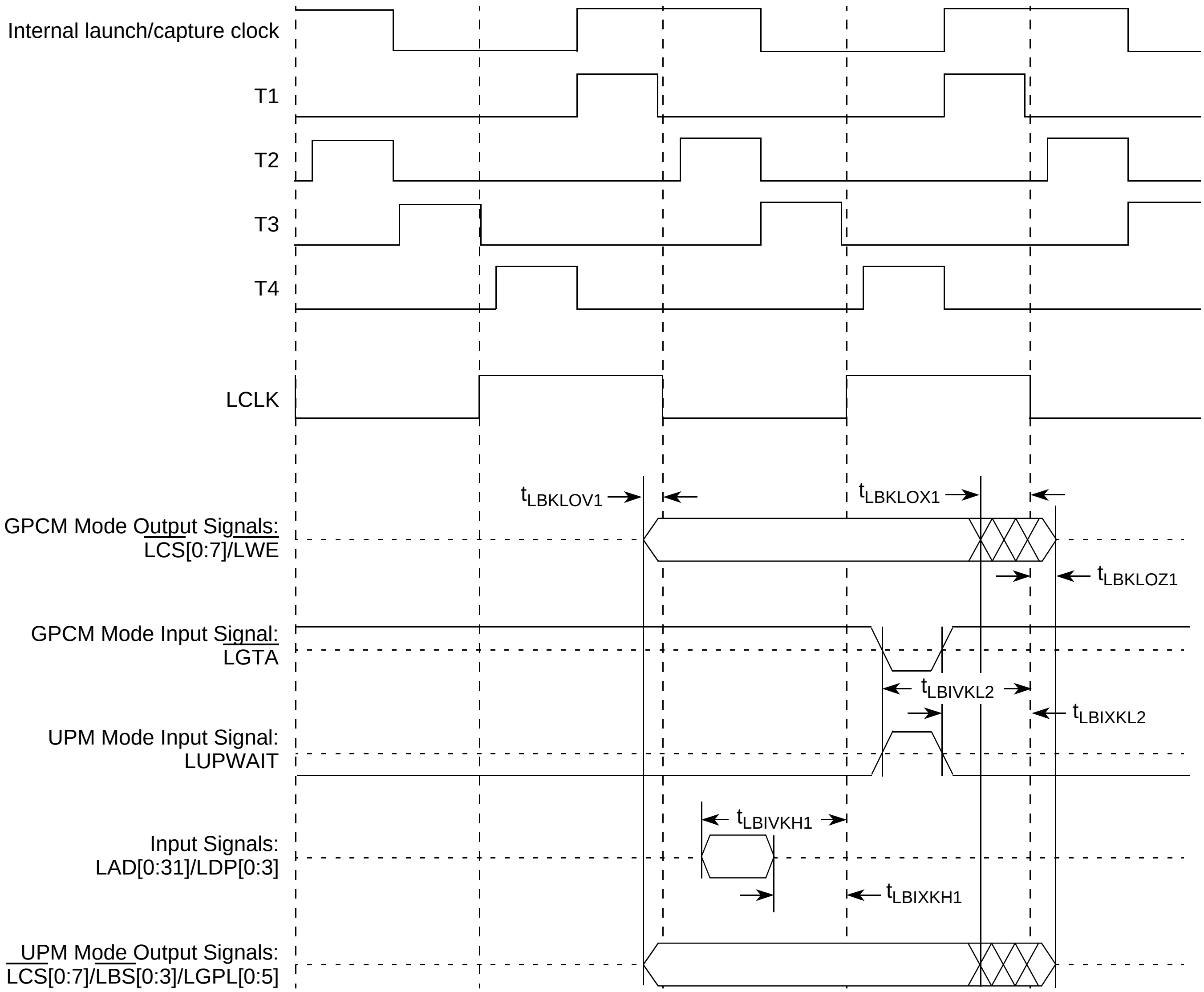

Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

$\overline{\text{SD1\_REF\_CLK}}$ for PCI Express and Serial RapidIO, or SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 44 shows a receiver reference diagram of the SerDes reference clocks. Characteristics are as follows:

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has on-chip 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

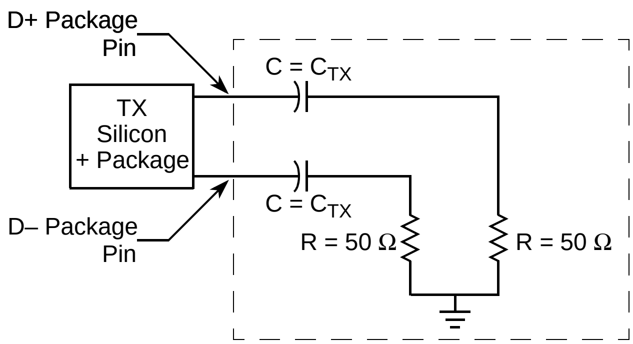

Figure 57. Compliance Test/Measurement Load

17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

17.5 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 65. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 69. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 70. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 58 with the parameters specified in Figure 71 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{D1\_MCAS}}$	Column Address Strobe	AC9	O	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	Row Address Strobe	AB12	O	GV_{DD}	—
D1_MCKE[0:3]	Clock Enable	M8, L9, T9, N8	O	GV_{DD}	11
$\overline{\text{D1\_MCS}}$[0:3]	Chip Select	AB9, AF10, AB11, AE11	O	GV_{DD}	—
D1_MCK[0:5]	Clock	V7, E13, AH11, Y9, F14, AG10	O	GV_{DD}	—
$\overline{\text{D1\_MCK}}$[0:5]	Clock Complements	Y10, E12, AH12, AA11, F13, AG11	O	GV_{DD}	—
D1_MODT[0:3]	On Die Termination	AD10, AF12, AC10, AE12	O	GV_{DD}	—
D1_MDIC[0:1]	Driver Impedance Calibration	E15, G14	I/O	GV_{DD}	25
DDR SDRAM Memory Interface 2					
D2_MDQ[0:63]	Data	A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7	I/O	GV_{DD}	—
D2_MECC[0:7]	Error Correcting Code	J5, H7, L7, N6, H4, H6, M4, M5	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N1	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	W2	O	GV_{DD}	—
D2_MDM[0:8]	Data Mask	A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5	O	GV_{DD}	—
D2_MDQS[0:8]	Data Strobe	B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS}}$[0:8]	Data Strobe	C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6	I/O	GV_{DD}	—
D2_MA[0:15]	Address	W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	O	BV_{DD}	5, 9
LGPL1/LFALE	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	O	BV_{DD}	5, 9
LGPL2/LOE/LFRE	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O	BV_{DD}	5, 8, 9
LGPL3/LFWP	UPM General Purpose Line 3 / Flash Write Protect	K16	O	BV_{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE /LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV_{DD}	—
LGPL5	UPM General Purpose Line 5 / Amux	B26	O	BV_{DD}	5, 9
LCLK[0:2]	Local Bus Clock	F17, F16, A23	O	BV_{DD}	—
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV_{DD}	—
LSYNC_OUT	Local Bus DLL Synchronization	A21	O	BV_{DD}	—
DMA					
DMA1_DACK[0:1]	DMA Acknowledge	W25, U30	O	OV_{DD}	21
DMA2_DACK[0]	DMA Acknowledge	AA26	O	OV_{DD}	5, 9
DMA1_DREQ[0:1]	DMA Request	Y29, V27	I	OV_{DD}	—
DMA2_DREQ[0]	DMA Request	V29	I	OV_{DD}	—
DMA1_DDONE[0:1]	DMA Done	Y28, V30	O	OV_{DD}	5, 9
DMA2_DDONE[0]	DMA Done	AA28	O	OV_{DD}	5, 9
DMA2_DREQ[2]	DMA Request	M23	I	BV_{DD}	—
Programmable Interrupt Controller					
UDE0	Unconditional Debug Event Processor 0	AC25	I	OV_{DD}	—
UDE1	Unconditional Debug Event Processor 1	AA25	I	OV_{DD}	—
MCP0	Machine Check Processor 0	M28	I	OV_{DD}	—
MCP1	Machine Check Processor 1	L28	I	OV_{DD}	—
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{IRQ\_OUT}$	Interrupt Output	U24	O	OV_{DD}	2, 4
1588					
TSEC_1588_CLK	Clock In	AM22	I	LV_{DD}	—
TSEC_1588_TRIG_IN	Trigger In	AM23	I	LV_{DD}	—
TSEC_1588_TRIG_OUT	Trigger Out	AA23	O	LV_{DD}	5, 9
TSEC_1588_CLK_OUT	Clock Out	AC23	O	LV_{DD}	5, 9
TSEC_1588_PULSE_OUT1	Pulse Out1	AA22	O	LV_{DD}	5, 9
TSEC_1588_PULSE_OUT2	Pulse Out2	AB23	O	LV_{DD}	5, 9
Ethernet Management Interface 1					
EC1_MDC	Management Data Clock	AL30	O	LV_{DD}	5, 9
EC1_MDIO	Management Data In/Out	AM25	I/O	LV_{DD}	—
Ethernet Management Interface 3					
EC3_MDC	Management Data Clock	AF19	O	TV_{DD}	5, 9
EC3_MDIO	Management Data In/Out	AF18	I/O	TV_{DD}	—
Ethernet Management Interface 5					
EC5_MDC	Management Data Clock	AF14	O	TV_{DD}	21
EC5_MDIO	Management Data In/Out	AF15	I/O	TV_{DD}	—
Gigabit Ethernet Reference Clock					
EC_GTX_CLK125	Reference Clock	AM24	I	LV_{DD}	32
Three-Speed Ethernet Controller 1					
TSEC1_RXD[7:0]/FIFO1_RXD[7:0]	Receive Data	AM28, AL28, AM26, AK23, AM27, AK26, AL29, AM30	I	LV_{DD}	1
TSEC1_TXD[7:0]/FIFO1_TXD[7:0]	Transmit Data	AC20, AD20, AE22, AB22, AC22, AD21, AB21, AE21	O	LV_{DD}	1, 5, 9
TSEC1_COL/FIFO1_TX_FC	Collision Detect/Flow Control	AJ23	I	LV_{DD}	1
TSEC1_CRS/FIFO1_RX_FC	Carrier Sense/Flow Control	AM31	I/O	LV_{DD}	1, 16
TSEC1_GTX_CLK	Transmit Clock Out	AK27	O	LV_{DD}	
TSEC1_RX_CLK/FIFO1_RX_CLK	Receive Clock	AL25	I	LV_{DD}	1

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
N/C	No Connection	A16, A20, B16, B17, B19, B20, C17, C18, C19, D28, R31, T17, V23, W23, Y22, Y23, Y24, AA24, AB24, AC24, AC26, AC27, AC29, AD31, AE29, AJ25, AK28, AL31, AM21	—	—	17

Note:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kO pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, “CCB/SYSCLK PLL Ratio.”
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 19.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore be described as an I/O for boundary scan.
10. If this pin is configured for local bus controller usage, recommend a weak pull-up resistor (2-10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and so on.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the VDD/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive diode.
15. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
16. This pin is only an output in FIFO mode when used as Rx Flow Control.
17. Do not connect.
18. These are test signals for factory use only and must be pulled up (100 Ω - 1 KΩ) to OVDD for normal machine operation.
19. Independent supplies derived from board VDD.
20. Recommend a pull-up resistor (~1 KΩ) be placed on this pin to OVDD.
21. The following pins must NOT be pulled down during power-on reset: DMA1_DACK[0:1], EC5_MDC, HRESET_REQ, TRIG_OUT/READY_P0/QUIESCE, MSRCID[2:4], MDVAL, ASLEEP.
22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
23. This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.
24. TSEC2_TXD[1] is used as cfg_dram_type. IT MUST BE VALID AT POWER-UP, EVEN BEFORE HRESET ASSERTION.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

25. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
26. These pins should be connected to XVDD_SRDS1.
27. These pins should be pulled to ground (XGND_SRDS1) through a 300-Ω (±10%) resistor.
28. These pins should be left floating.
29. These pins should be pulled up to TVDD through a 2–10 KΩ resistor.
30. These pins have other manufacturing or debug test functions. It is recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
31. DDRCLK input is only required when the MPC8572E DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* Rev.0, Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
32. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
33. These pins should be pulled to ground (GND).
34. These pins are sampled at POR for General Purpose configuration use by software. Their value has no impact on the functionality of the hardware.

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of $\overline{\text{LWE}}$[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

Table 81. e500 Core1 to CCB Clock Ratio

Binary Value of $\overline{\text{LWE}}$[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	Binary Value of $\overline{\text{LWE}}$[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Table 82. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1