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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572ecvtauld

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision

- Three PCI Express controllers
 - PCI Express 1.0a compatible
 - Supports x8, x4, x2, and x1 link widths (see following bullet for specific width configuration options)
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Full 64-bit decode with 36-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - Single x8/x4/x2/x1 PCI Express
 - Dual x4/x2/x1 PCI Express
 - Single x4/x2/x1 PCI Express and dual x2/x1 PCI Express
 - Single 1x/4x Serial RapidIO and single x4/x2/x1 PCI Express
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, that automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™ compatible, JTAG boundary scan
- 1023 FC-PBGA package

Figure 1 shows the MPC8572E block diagram.

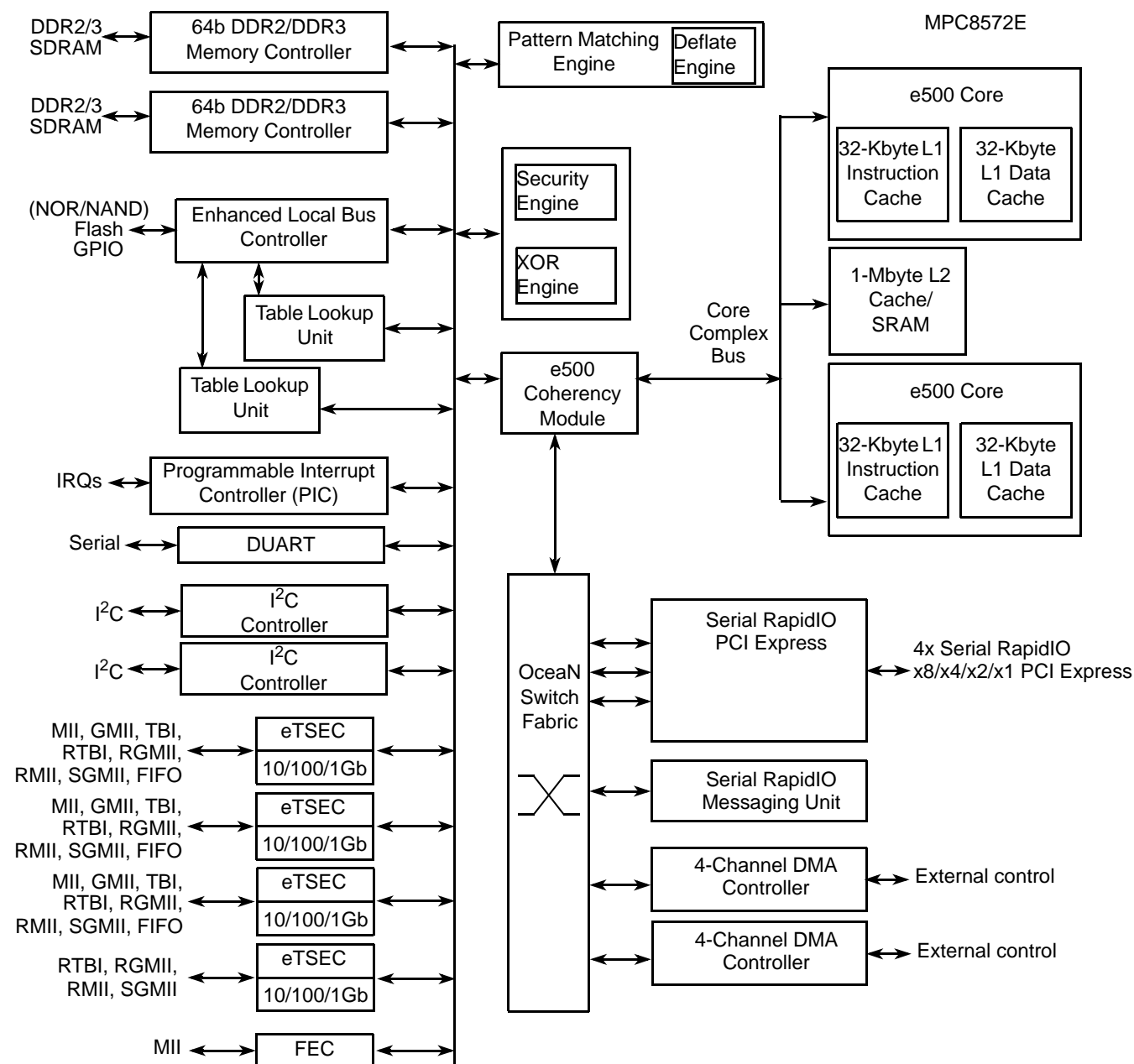


Figure 1. MPC8572E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KH}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency \leq platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency \leq platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

[Table 9](#) describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of \overline{HRESET}	100	—	μs	2
Minimum assertion time for \overline{SRESET}	3	—	SYSCLKs	1

Table 14 provides the current draw characteristics for MV_{REFn} .

Table 14. Current Draw Characteristics for MV_{REFn}

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for MV_{REFn}	DDR2 SDRAM	$I_{MV_{REFn}}$	—	1500	μA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for MV_{REFn} must be able to supply up to 1500 μA or 1250 μA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≥ 667 MHz	V_{ILAC}	—	$MV_{REFn} - 0.20$	V	—
	≤ 533 MHz		—	$MV_{REFn} - 0.25$		
AC input high voltage	≥ 667 MHz	V_{IHAC}	$MV_{REFn} + 0.20$	—	V	—
	≤ 533 MHz		$MV_{REFn} + 0.25$	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V \pm 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REFn} - 0.175$	V	—
AC input high voltage	V_{IHAC}	$MV_{REFn} + 0.175$	—	V	—

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and SD2_TX[n]) as depicted in Figure 23.

Table 38. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	XV_{DD_SRDS2}	1.045	1.1	1.155	V	—
Output high voltage	V_{OH}	—	—	$XV_{DD_SRDS2-Typ}/2 + V_{ODI-max} /2$	mV	1
Output low voltage	V_{OL}	$XV_{DD_SRDS2-Typ}/2 - V_{ODI-max} /2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage ^{2, 3, 5}	$ V_{ODI} $	359	550	791	mV	Equalization setting: 1.0x
		329	505	725		Equalization setting: 1.09x
		299	458	659		Equalization setting: 1.2x
		270	414	594		Equalization setting: 1.33x
		239	367	527		Equalization setting: 1.5x
		210	322	462		Equalization setting: 1.71x
		180	275	395		Equalization setting: 2.0x
Output offset voltage	V_{OS}	473	550	628	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta V_{ODI} $	—	—	25	mV	—

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.4	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	6.67	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4

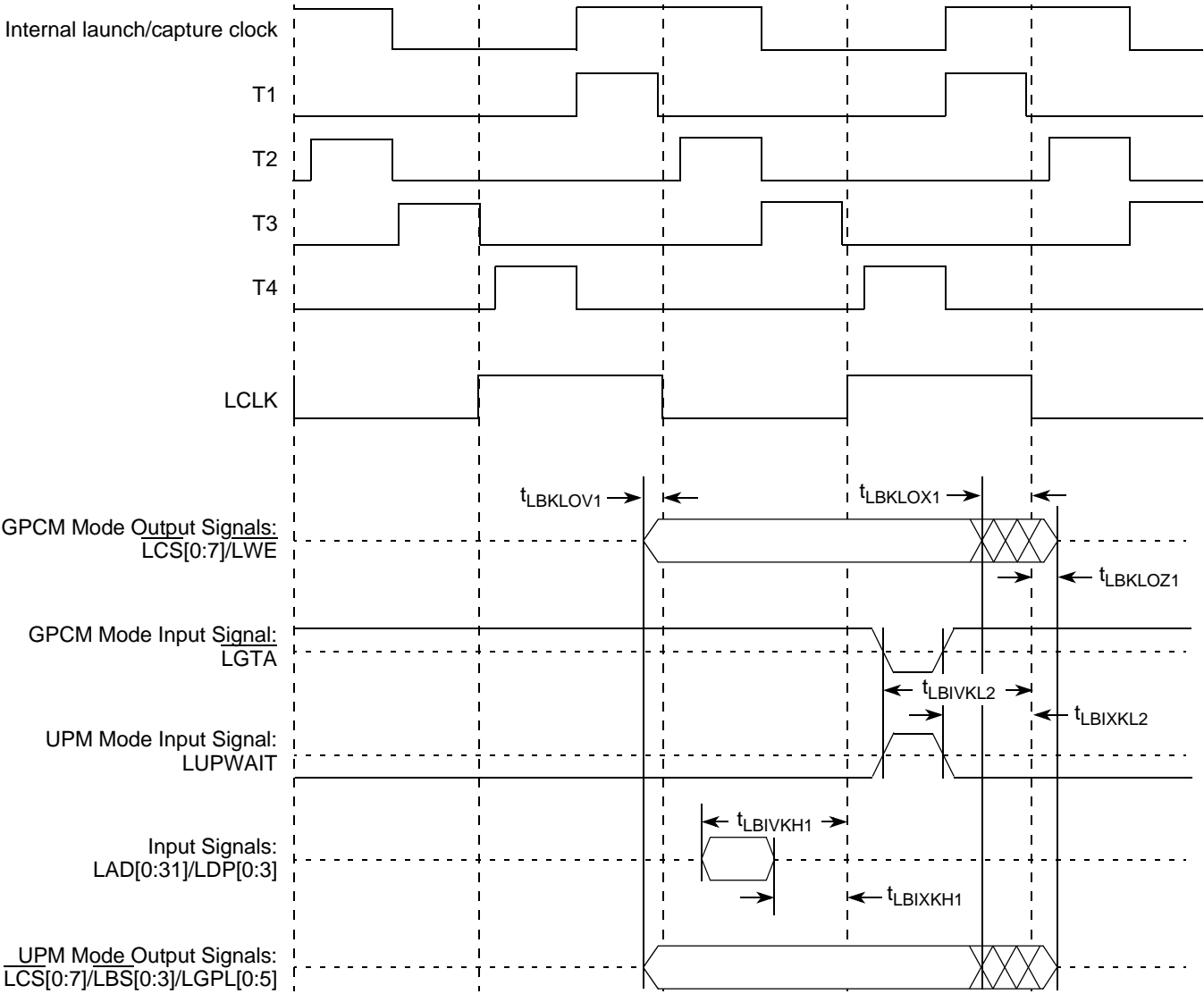


Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) ¹ (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	3	19		5, 6
TDO	t_{JTKLOZ}	3	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive $50\text{-}\Omega$ load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.

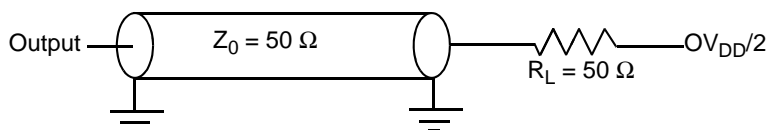

Figure 36. AC Test Load for the JTAG Interface

Figure 37 provides the JTAG clock input timing diagram.

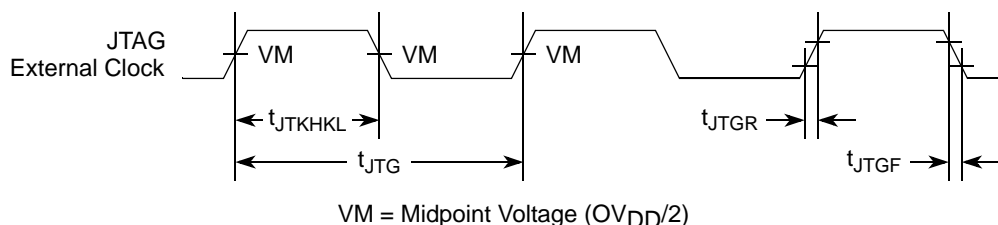

Figure 37. JTAG Clock Input Timing Diagram

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.

Table 58 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 1.8 \text{ V DC}$.

Table 58. GPIO DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	1.71	1.89	V
High-level input voltage	V_{IH}	$0.65 \times BV_{DD}$	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	$0.35 \times BV_{DD}$	V
Input current ($BV_{IN}^1 = 0 \text{ V}$ or $BV_{IN} = BV_{DD}$)	I_{IN}	TBD	TBD	μA
High-level output voltage ($I_{OH} = -100 \mu\text{A}$)	V_{OH}	$BV_{DD} - 0.2$	—	V
High-level output voltage ($I_{OH} = -2 \text{ mA}$)	V_{OH}	$BV_{DD} - 0.45$	—	V
Low-level output voltage ($I_{OL} = 100 \mu\text{A}$)	V_{OL}	—	0.2	V
Low-level output voltage ($I_{OL} = 2 \text{ mA}$)	V_{OL}	—	0.45	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications¹

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	2

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.

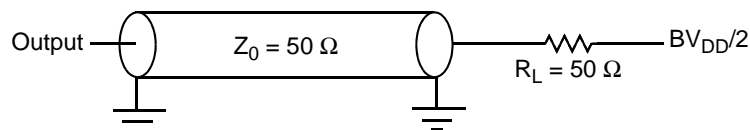


Figure 42. GPIO AC Test Load

15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND_SRDS_n (xc0revss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

NOTE

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = V_{RXD+} + V_{RXD-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)} \text{ of } V_{RX-D+} + V_{RX-D-} /2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance ($50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 69. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 70. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in [Figure 58](#) with the parameters specified in [Figure 71](#) when measured at the output pins of the device and the device is driving a $100\ \Omega$ +/-5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

18.2 Mechanical Dimensions of the MPC8572E FC-PBGA

Figure 61 shows the mechanical dimensions of the MPC8572E FC-PBGA package with full lid.

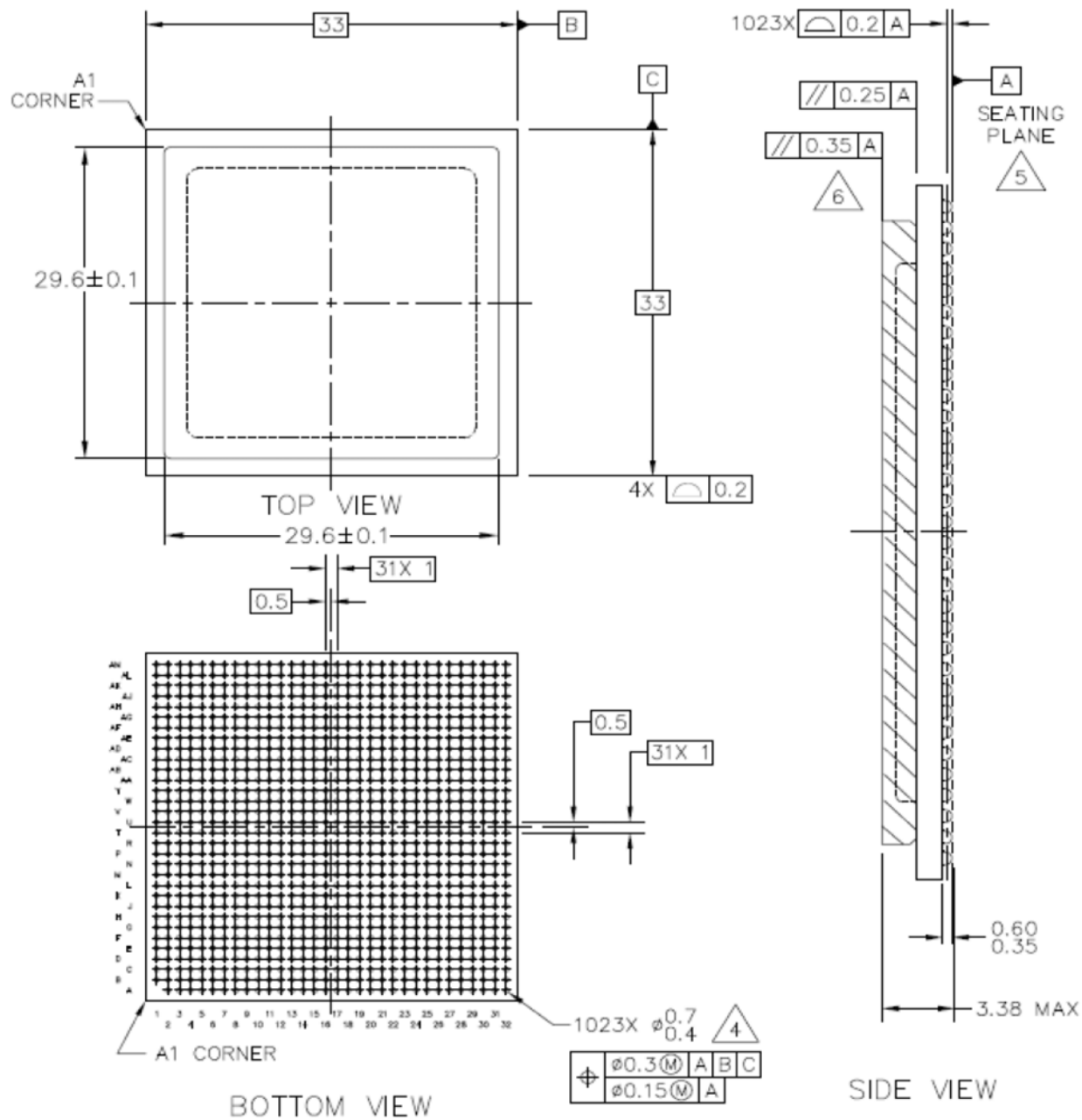


Figure 61. Mechanical Dimensions of the MPC8572E FC-PBGA with Full Lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

Table 77. MPC8572E Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1067 MHz		1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Notes:

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) [Section 19.3, “e500 Core PLL Ratio,”](#) and [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
- The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. [Table 78](#) provides the clocking specifications for the memory bus.

Table 79. CCB Clock Ratio

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	8:1
100	10:1
101	12:1
110	Reserved
111	Reserved

19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

[Table 80](#) describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ at power up, as shown in [Table 80](#).

Table 80. e500 Core0 to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

Table 82. DDR Clock Ratio (continued)

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
101	12:1
110	14:1
111	Synchronous mode

19.5 Frequency Options

19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

Table 83. Frequency Options for Platform Frequency

CCB to SYSCLK Ratio	SYSCLK (MHz)							
	33.33	41.66	50	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)							
4						400	444	533
5					415	500	555	
6				400	498	600		
8			400	533				
10		417	500					
12	400	500	600					

19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, “I/O Port Selection,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, “Link Width,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the “PCI Express link width”

Table 87. Part Numbering Nomenclature—Rev 2.1

MPC	nnnn	e	t	l	pp	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = -40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 150-MHz processor; 800 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included
		Blank = Not included				AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included

Notes:

- ¹ MPC stands for “Qualified.”
PPC stands for “Prototype”
- ² See [Section 18, “Package Description,”](#) for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 88. Part Numbering Nomenclature—Rev 1.1.1

MPC	nnnn	e	t	pp	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Package Sphere Type ²	Processor Frequency/DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank=0 to 105°C C= −40 to 105°C	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz process or; 667 MT/s DDR datarate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included
		Blank = Not included			B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included	

Notes:

- ¹ MPC stands for “Qualified.”
PPC stands for “Prototype”
- ² See [Section 18, “Package Description,”](#) for more information on the available package types.