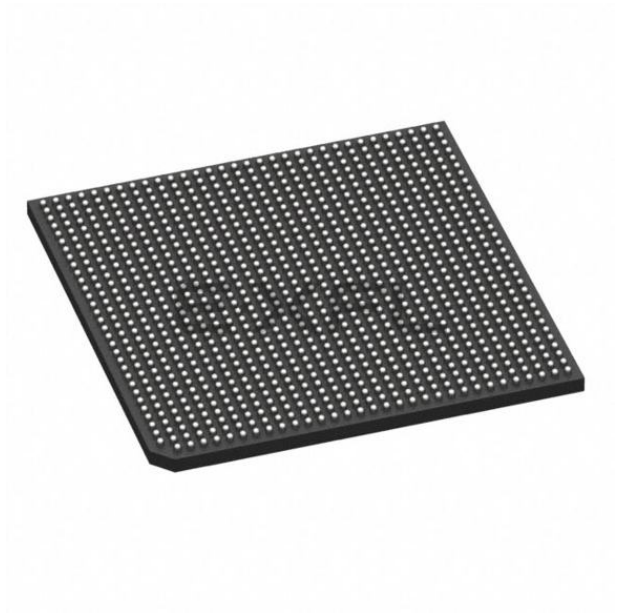

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.333GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 1023-BFBGA, FCBGA |
| Supplier Device Package | 1023-FCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572ecvtaule |

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- 10/100 Fast Ethernet controller (FEC) management interface
  - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
  - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
  - Four DMA channels per controller
  - All channels accessible by the local masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
  - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins ($\overline{\text{DMA2\_DREQ}}$[2]) is made available

**Table 9. RESET Initialization Timing Specifications (continued)**

| | | | | |
|---|---|---|---|---|
| PLL config input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | µs | — |
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 1 |
| Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 1 |

**Notes:**
1. SYSCLK is the primary clock input for the MPC8572E.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

**Table 10. PLL Lock Times**

| Parameter/Condition | Symbol | Min | Typical | Max |
|---|---|---|---|---|
| PLL lock times | — | 100 | µs | — |
| Local bus PLL | — | 50 | µs | — |

# 6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required $GV_{DD}$(typ) voltage is 1.8Vor 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

## 6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

**Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | $MV_{REF}n$ | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}n - 0.04$ | $MV_{REF}n + 0.04$ | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n + 0.125$ | $GV_{DD} + 0.3$ | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}n - 0.125$ | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | µA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |

Table 14 provides the current draw characteristics for $MV_{REF}n$.

**Table 14. Current Draw Characteristics for $MV_{REF}$ *n***

| Parameter / Condition | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Current draw for $MV_{REF}n$ | DDR2 SDRAM | $I_{MVREF}n$ | — | 1500 | µA | 1 |
| | DDR3 SDRAM | | | 1250 | | |

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

## 6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

### 6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

**Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%

| Parameter | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| AC input low voltage | >=667 MHz | $V_{ILAC}$ | — | $MV_{REF}n$ – 0.20 | V | — |
| | <= 533 MHz | | — | $MV_{REF}n$ – 0.25 | | |
| AC input high voltage | >=667 MHz | $V_{IHAC}$ | $MV_{REF}n$ + 0.20 | — | V | — |
| — | <= 533 MHz | | $MV_{REF}n$ + 0.25 | — | | |

**Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{ILAC}$ | — | $MV_{REF}n$ – 0.175 | V | — |
| AC input high voltage | $V_{IHAC}$ | $MV_{REF}n$ + 0.175 | — | V | — |

Figure 6 provides the AC test load for the DDR2 and DDR3 Controller bus.

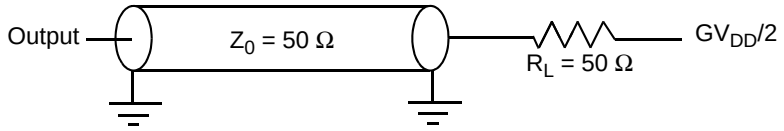
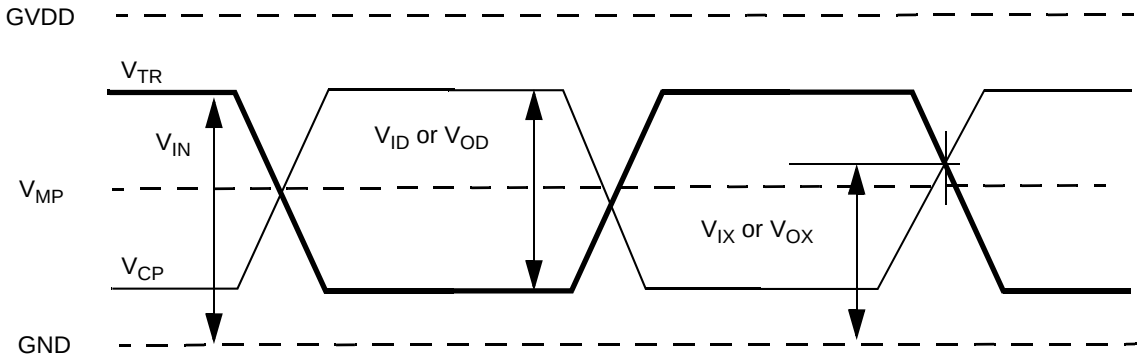



**Figure 6. DDR2 and DDR3 Controller bus AC Test Load**

## 6.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E.




**NOTE**

VID specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 19 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR2 mode.

**Table 19. DDR2 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| DC Input Signal Voltage | $V_{IN}$ | –0.3 | $GV_{DD}$ + 0.3 | V | — |
| DC Differential Input Voltage | $V_{ID}$ | — | — | mV | — |
| AC Differential Input Voltage | $V_{IDAC}$ | — | — | mV | — |
| DC Differential Output Voltage | $V_{OH}$ | — | — | mV | — |
| AC Differential Output Voltage | $V_{OHAC}$ | JEDEC: 0.5 | JEDEC: $GV_{DD}$ + 0.6 | V | — |
| AC Differential Cross-point Voltage | $V_{IXAC}$ | — | — | mV | — |
| Input Midpoint Voltage | $V_{MP}$ | — | — | mV | — |

## 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

**Table 22. DUART AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | $f_{CCB}$/1,048,576 | baud | 1, 2 |
| Maximum baud rate | $f_{CCB}$/16 | baud | 1, 2, 3 |
| Oversample rate | 16 | — | 1, 4 |

**Notes:**
1. Guaranteed by design
2. $f_{CCB}$ refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the $8^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each $16^{th}$ sample.

# 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V .

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 8.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

**Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | µA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | µA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1 and 2.
2 $TV_{DD}$ supports eTSECs 3 and 4 or FEC.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

## 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

**Table 25. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period[1] | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |

Figure 11 shows the GMII receive AC timing diagram.

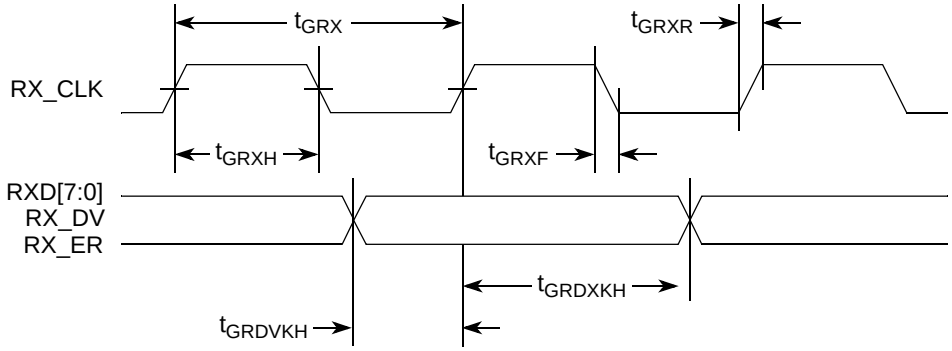



**Figure 11. GMII Receive AC Timing Diagram**

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

**Table 29. MII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$[2] | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%-80%) | $t_{MTXR}$[2] | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%-20%) | $t_{MTXF}$[2] | 1.0 | — | 4.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

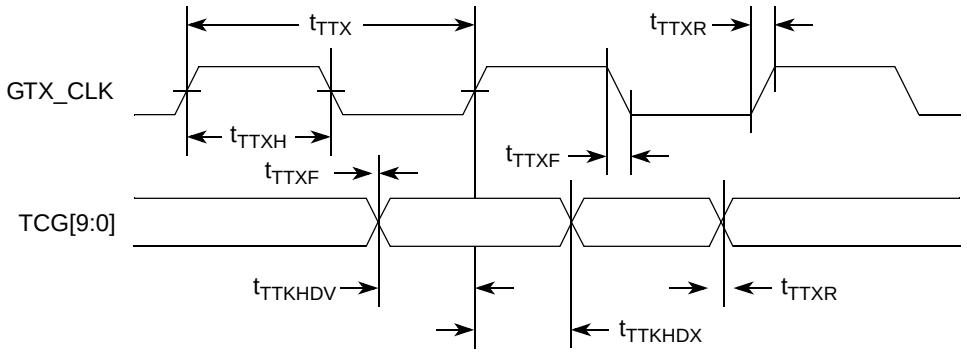



**Figure 15. TBI Transmit AC Timing Diagram**

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

**Table 32. TBI Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition [3] | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock period for TBI Receive Clock 0, 1 | $t_{TRX}$ | — | 16.0 | — | ns |
| Skew for TBI Receive Clock 0, 1 | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| Duty cycle for TBI Receive Clock 0, 1 | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDVKH}$ | 2.5 | — | — | ns |
| RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDXKH}$ | 1.5 | — | — | ns |
| Clock rise time (20%-80%) for TBI Receive Clock 0, 1 | $t_{TRXR}$ [2] | 0.7 | — | 2.4 | ns |
| Clock fall time (80%-20%) for TBI Receive Clock 0, 1 | $t_{TRXF}$ [2] | 0.7 | — | 2.4 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

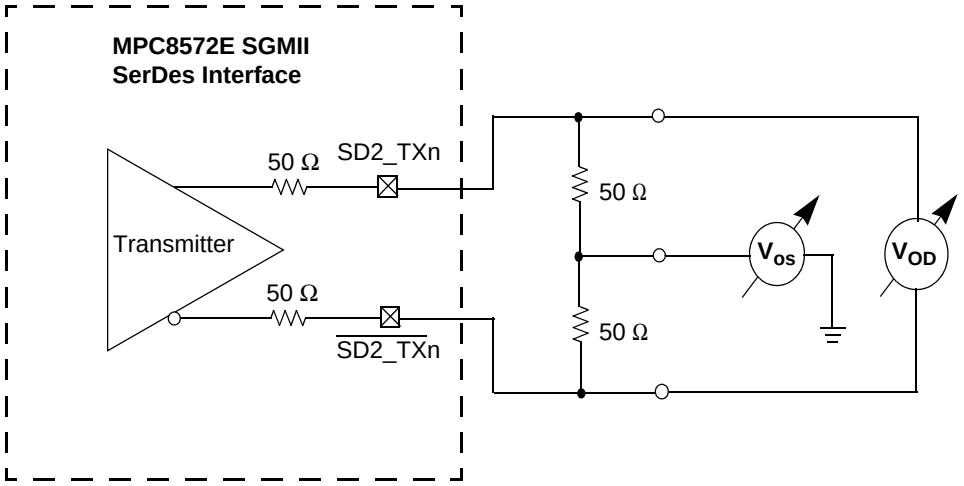



**Figure 23. SGMII Transmitter DC Measurement Circuit**

Table 39 lists the SGMII DC receiver electrical characteristics.

**Table 39. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX\_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM\_ACp-p}$ | | — | 100 | mV | 5 |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | | $Z_{RX\_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of MPC8572E's SerDes 2 Control Register.
5. $V_{CM\_ACp-p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

### 8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

#### 8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

**Table 40. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $XV_{DD\_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| $V_{OD}$ fall time (80%-20%) | tfall | 50 | — | 120 | ps | — |
| $V_{OD}$ rise time (20%-80%) | $t_{rise}$ | 50 | — | 120 | ps | — |

**Notes:**
1. Each UI is 800 ps ± 100 ppm.

#### 8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

**Table 41. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $XV_{DD\_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal Jitter Tolerance | JSIN | 0.1 | — | — | UI p-p | 1 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC Coupling Capacitor | $C_{TX}$ | 5 | — | 200 | nF | 3 |

**Notes:**
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

**Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | $t_{T1588OV}$ | 0.5 | — | 3.0 | ns | — |
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | $2*t_{T1588CLK\_MAX}$ | — | — | ns | 2 |

**Note:**

1. When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of $t_{T1588CLK}$ is defined in terms of $T_{TX\_CLK}$, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the $T_{TX\_CLK}$ is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.
2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

## 9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

**Table 43. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=3.3 V)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $LV_{DD}/TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | $OV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ =Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($LV_{DD}/TV_{DD}$ = Max, $V_{IN}$ [3] = 2.1 V) | $I_{IH}$ | — | 40 | µA | — |

**Table 43. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=3.3 V) (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input low current ($LV_{DD}/TV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | µA | — |

**Note:**
1. EC1_MDC and EC1_MDIO operate on $LV_{DD}$.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on $TV_{DD}$.
3. Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbol referenced in Table 1.

**Table 44. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=2.5 V)**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}/TV_{DD}$ | 2.37 | 2.63 | V | 1,2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.70 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | µA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | µA | 3 |

**Note:**

1 EC1_MDC and EC1_MDIO operate on $LV_{DD}$.
2 EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on $TV_{DD}$.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

## 9.2 MII Management AC Electrical Specifications

Table 45 provides the MII management AC timing specifications.There are three sets of Ethernet management signals (EC1_MDC and EC1_MDIO, EC3_MDC and EC3_MDIO, EC5_MDC and EC5_MDIO). These are not explicitly shown in the table or in the figure following.

**Table 45. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| ECn_MDC frequency | $f_{MDC}$ | 0.9 | 2.5 | 9.3 | MHz | 2, 3 |
| ECn_MDC period | $t_{MDC}$ | 107.5 | — | 1120 | ns | — |
| ECn_MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| ECn_MDC to ECn_MDIO delay | $t_{MDKHDX}$ | 10 | — | $16*t_{plb\_clk}$ | ns | 5 |

**Table 50. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC)—PLL Enabled (continued)**

At recommended operating conditions with $BV_{DD}$ of 2.5 V ± 5% (continued)

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.4 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.4 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.4 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.8 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 1.8 V DC

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 1.8 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 2.4 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)—PLL Enabled (continued)**

At recommended operating conditions with $BV_{DD}$ of 1.8 V ± 5% (continued)

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.2 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 3.2 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 3.2 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 3.2 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 3.2 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.9 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.9 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.

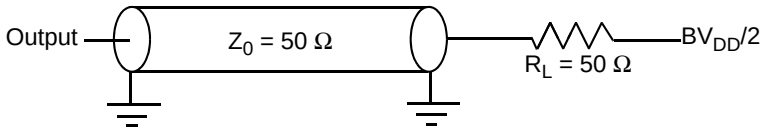



**Figure 29. Local Bus AC Test Load**

# 14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

## 14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 56. GPIO DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 57. GPIO DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 2.5V | $BV_{DD}$ | 2.37 | 2.63 | V |
| High-level input voltage | $V_{IH}$ | 1.70 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.7 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IH}$ | — | 10 | μA |
| | $I_{IL}$ | | –15 | |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | $BV_{DD}$ + 0.3 | V |
| Low-level output voltage ($BV_{DD}$ min, $I_{OL}$ = 1 mA) | $V_{OL}$ | GND – 0.3 | 0.4 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

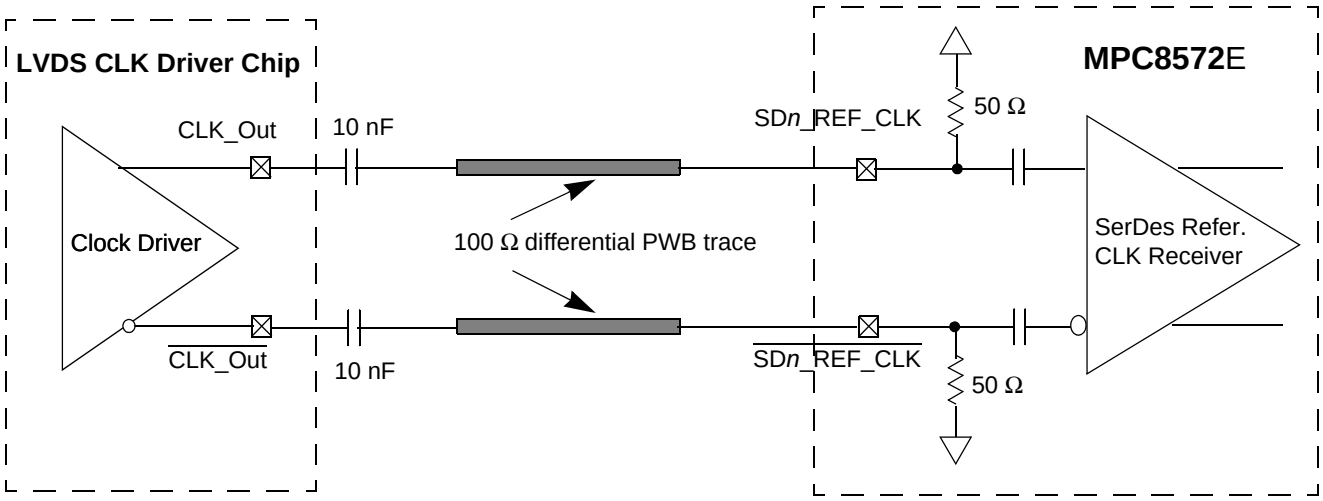



**Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Consult

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

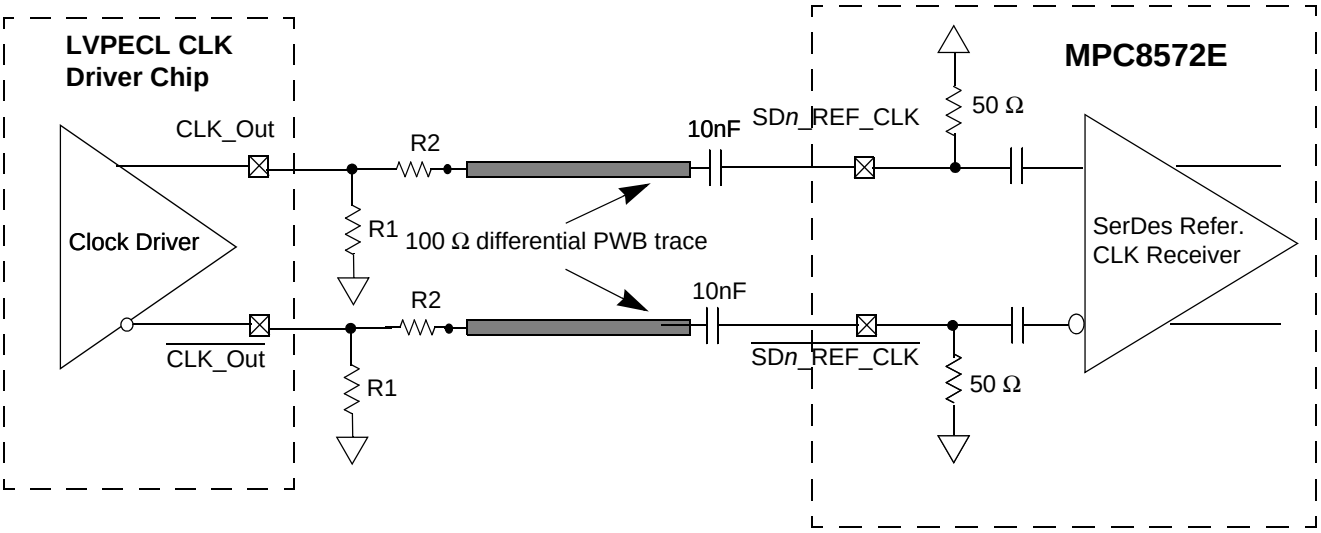



**Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

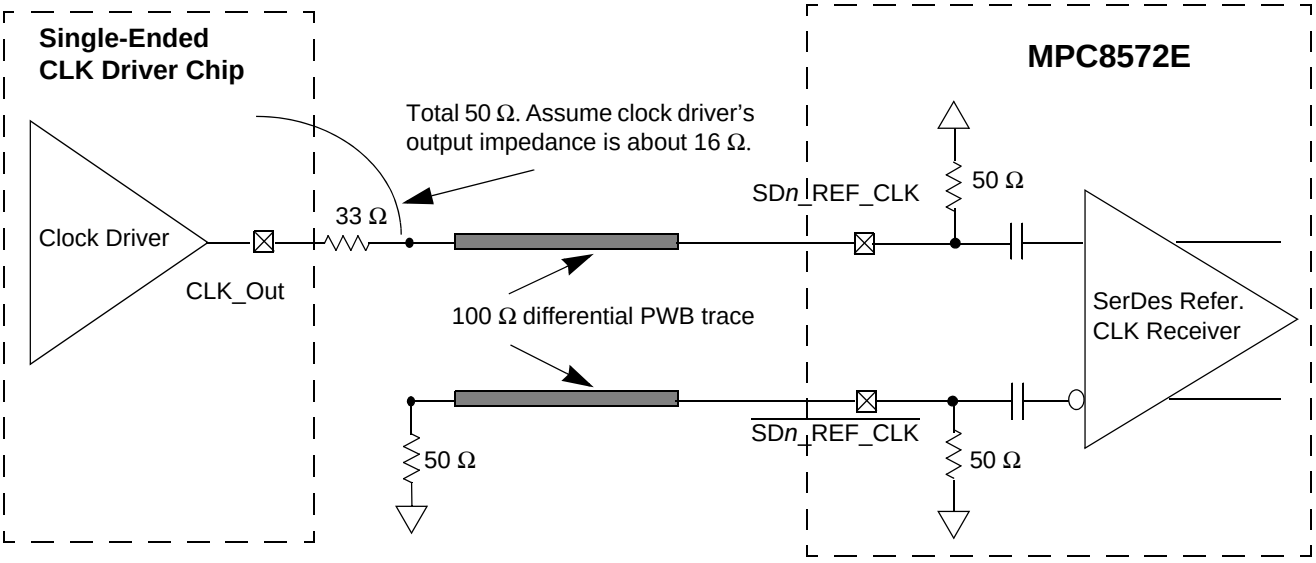



**Figure 51. Single-Ended Connection (Reference Only)**

## 15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

## 17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

## 17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

**Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10(8) | — | ns | 8 ns applies only to serial RapidIO with 125-MHz reference clock |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 80 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –40 | — | 40 | ps | — |

## 17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC3_GTX_CLK | Transmit Clock Out | AE17 | O | $TV_{DD}$ | |
| TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK | Receive Clock | AF17 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV | Receive Data Valid | AG14 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER | Receive Error | AH15 | I | $TV_{DD}$ | 1 |
| TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK | Transmit Clock In | AF16 | I | $TV_{DD}$ | 1 |
| TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN | Transmit Enable | AJ18 | O | $TV_{DD}$ | 1, 22 |
| **Three-Speed Ethernet Controller 4** | | | | | |
| TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4] | Transmit Data | AD15, AC16, AC14, AB16 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4] | Receive Data | AE15, AF13, AE14, AH14 | I | $TV_{DD}$ | 1 |
| TSEC4_GTX_CLK | Transmit Clock Out | AB14 | O | $TV_{DD}$ | — |
| TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC | Receive Clock | AG13 | I | $TV_{DD}$ | 1 |
| TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC | Receive Data Valid | AD13 | I/O | $TV_{DD}$ | 1, 23 |
| TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER | Transmit Enable | AB15 | O | $TV_{DD}$ | 1, 22 |
| **DUART** | | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | Clear to Send | W30, Y27 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | Ready to Send | W31, Y30 | O | $OV_{DD}$ | 5, 9 |
| UART_SIN[0:1] | Receive Data | Y26, W29 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | Transmit Data | Y25, W26 | O | $OV_{DD}$ | 5, 9 |
| **$I^2C$ Interface** | | | | | |
| IIC1_SCL | Serial Clock | AC30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC1_SDA | Serial Data | AB30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SCL | Serial Clock | AD30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SDA | Serial Data | AD29 | I/O | $OV_{DD}$ | 4, 20 |
| **SerDes (x10) PCIe, SRIO** | | | | | |

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

## 21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio." The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

## 21.2 Power Supply Design

### 21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_PLAT, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_DDR, $AV_{DD}$_LBIU, $AV_{DD}$_SRDS1 and $AV_{DD}$_SRDS2 respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 62, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.