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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572elpxatld

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

- Three inbound windows plus a configuration window on PCI Express
 - Four inbound windows plus a default window on Serial RapidIO®
 - Four outbound windows plus default translation for PCI Express
 - Eight outbound windows plus default translation for Serial RapidIO with segmentation and sub-segmentation support
- Two 64-bit DDR2/DDR3 memory controllers
 - Programmable timing supporting DDR2 and DDR3 SDRAM
 - 64-bit data interface per controller
 - Four banks of memory supported, each up to 4 Gbytes, for a maximum of 16 Gbytes per controller
 - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
 - Full ECC support
 - Page mode support
 - Up to 32 simultaneous open pages for DDR2 or DDR3
 - Contiguous or discontiguous memory mapping
 - Cache line, page, bank, and super-bank interleaving between memory controllers
 - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
 - Sleep mode support for self-refresh SDRAM
 - On-die termination support when using DDR2 or DDR3
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access through JTAG port
 - 1.8-V SSTL_1.8 compatible I/O
 - Support 1.5-V operation for DDR3. The detail is TBD pending on official release of appropriate industry specifications.
 - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts per processor with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high resolution timers/counters per processor that can generate interrupts
 - Supports a variety of other internal interrupt sources

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- 10/100 Fast Ethernet controller (FEC) management interface
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
 - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
 - Four DMA channels per controller
 - All channels accessible by the local masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
 - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins (DMA2_DREQ[2]) is made available

- Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
 - Supports *RapidIO Interconnect Specification, Revision 1.2*
 - Both 1x and 4x LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto-detection of 1x- and 4x-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compliant message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox
 - Single inbound doorbell message structure
 - Facility to accept port-write messages

Table 9. RESET Initialization Timing Specifications (continued)

PLL config input setup time with stable SYSCLK before HRESET negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs	1

Notes:

1. SYSCLK is the primary clock input for the MPC8572E.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Symbol	Min	Typical	Max
PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—

6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required $GV_{DD}(\text{typ})$ voltage is 1.8V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REFn}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REFn} - 0.04$	$MV_{REFn} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REFn} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REFn} - 0.125$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

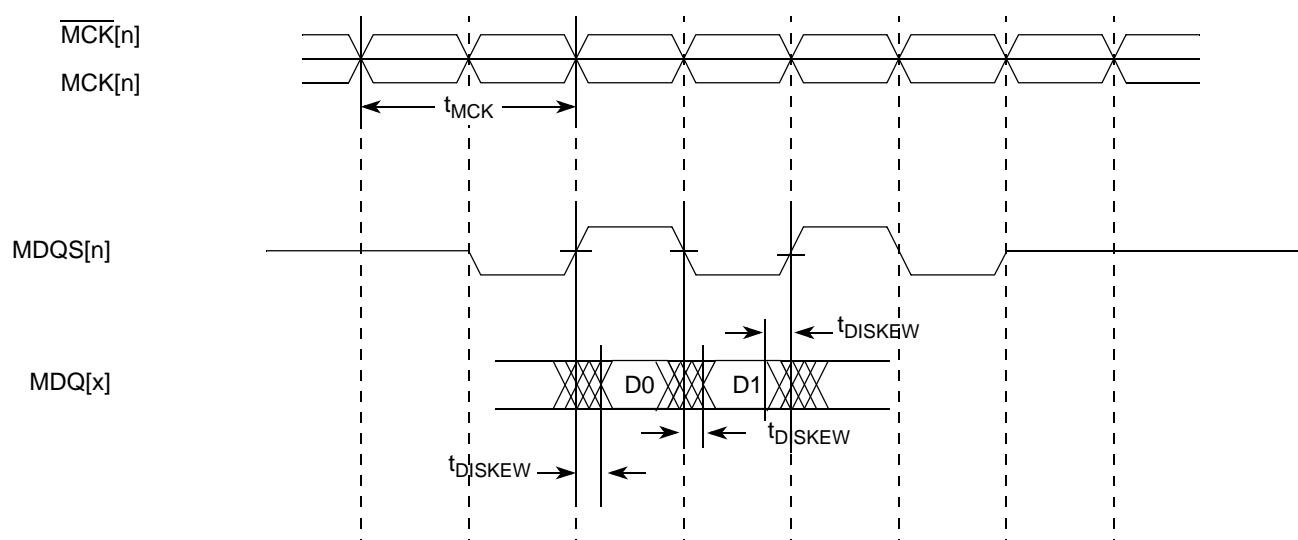
At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 MHz	—	–200	200	—	—
667 MHz	—	–240	240	—	—
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.


Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{MCS}[n]$ output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t_{DDKHCS}	1.95	—	ns	3
$\overline{MCS}[n]$ output hold with respect to MCK	$t_{DDKHCSX}$			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKMHM}			ns	4
800 MHz		−0.375	0.375		
≤ 667 MHz		−0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS} , t_{DDKLDS}			ps	5
800 MHz		375	—		
667 MHz		450	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX} , t_{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	—		

Figure 6 provides the AC test load for the DDR2 and DDR3 Controller bus.

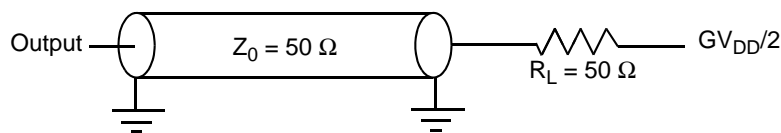
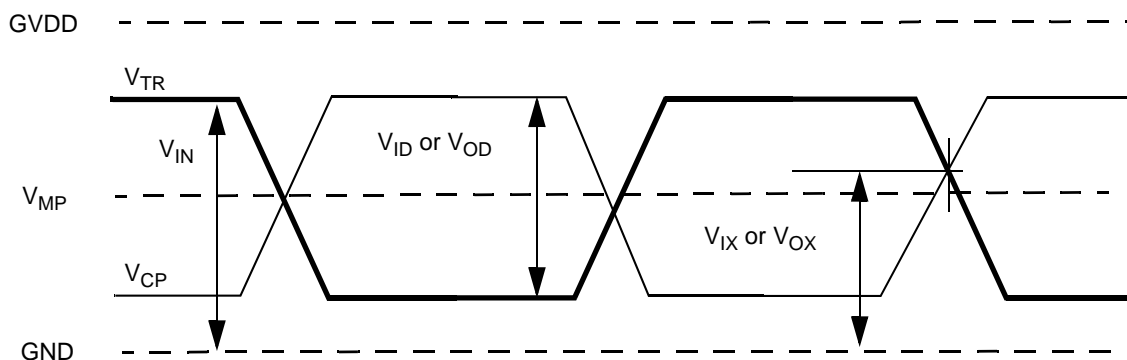


Figure 6. DDR2 and DDR3 Controller bus AC Test Load

6.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E.



NOTE

VID specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as \overline{MCK} or \overline{MDQS}) and V_{CP} is the complementary input signal (such as MCK or $MDQS$).

Table 19 provides the differential specifications for the MPC8572E differential signals $\overline{MDQS}/MDQS$ and \overline{MCK}/MCK when in DDR2 mode.

Table 19. DDR2 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V_{IN}	-0.3	$GV_{DD} + 0.3$	V	—
DC Differential Input Voltage	V_{ID}	—	—	mV	—
AC Differential Input Voltage	V_{IDAC}	—	—	mV	—
DC Differential Output Voltage	V_{OH}	—	—	mV	—
AC Differential Output Voltage	V_{OHAC}	JEDEC: 0.5	JEDEC: $GV_{DD} + 0.6$	V	—
AC Differential Cross-point Voltage	V_{IXAC}	—	—	mV	—
Input Midpoint Voltage	V_{MP}	—	—	mV	—

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB}/1,048,576$	baud	1, 2
Maximum baud rate	$f_{CCB}/16$	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:

1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

The electrical characteristics for SGMII is specified in [Section 8.3, “SGMII Interface Electrical Characteristics.”](#) The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and SD2_TX[n]) as depicted in Figure 23.

Table 38. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	XV_{DD_SRDS2}	1.045	1.1	1.155	V	—
Output high voltage	V_{OH}	—	—	$XV_{DD_SRDS2-Typ}/2 + V_{ODL-max} /2$	mV	1
Output low voltage	V_{OL}	$XV_{DD_SRDS2-Typ}/2 - V_{ODL-max} /2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage ^{2, 3, 5}	$ V_{OD} $	359	550	791	mV	Equalization setting: 1.0x
		329	505	725		Equalization setting: 1.09x
		299	458	659		Equalization setting: 1.2x
		270	414	594		Equalization setting: 1.33x
		239	367	527		Equalization setting: 1.5x
		210	322	462		Equalization setting: 1.71x
		180	275	395		Equalization setting: 2.0x
Output offset voltage	V_{OS}	473	550	628	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta V_{OD} $	—	—	25	mV	—

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with V_{DD}/TV_{DD} of $3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
ECn_MDIO to ECn_MDC setup time	t_{MDDVKH}	5	—	—	ns	—
ECn_MDIO to ECn_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
ECn_MDC rise time	t_{MDCR}	—	—	10	ns	4
ECn_MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and } t_{\text{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, } t_{MDKHDX}$ symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIIMCFG[MgmtClk] encoding selection). For example, if MIIMCFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3\text{ MHz}$. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
- The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
- Guaranteed by design.
- t_{plb_clk} is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.

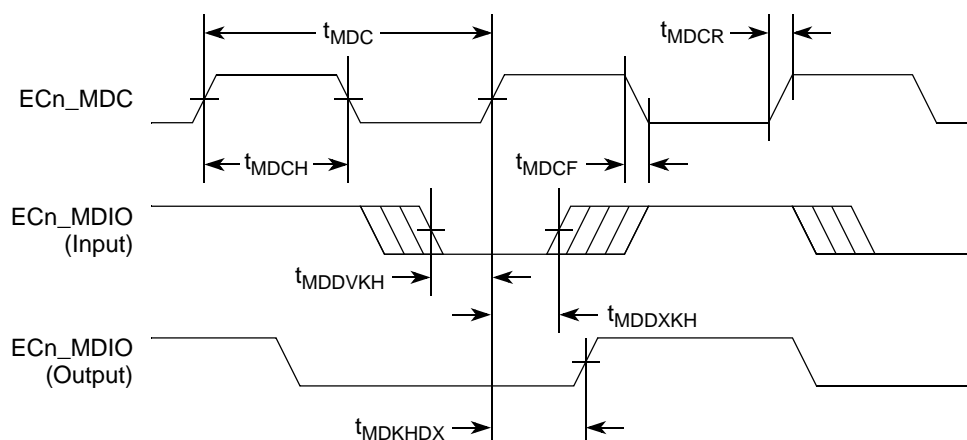


Figure 28. MII Management Interface Timing Diagram

Table 58 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 1.8 \text{ V DC}$.

Table 58. GPIO DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	1.71	1.89	V
High-level input voltage	V_{IH}	$0.65 \times BV_{DD}$	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	$0.35 \times BV_{DD}$	V
Input current ($BV_{IN}^1 = 0 \text{ V}$ or $BV_{IN} = BV_{DD}$)	I_{IN}	TBD	TBD	μA
High-level output voltage ($I_{OH} = -100 \mu\text{A}$)	V_{OH}	$BV_{DD} - 0.2$	—	V
High-level output voltage ($I_{OH} = -2 \text{ mA}$)	V_{OH}	$BV_{DD} - 0.45$	—	V
Low-level output voltage ($I_{OL} = 100 \mu\text{A}$)	V_{OL}	—	0.2	V
Low-level output voltage ($I_{OL} = 2 \text{ mA}$)	V_{OL}	—	0.45	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications¹

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	2

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.

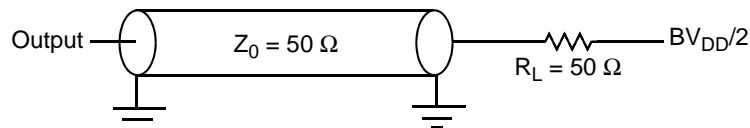


Figure 42. GPIO AC Test Load

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$L_{RX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 57](#) should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in [Figure 56](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see [Figure 57](#)). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS1	SerDes Transceiver Core Logic GND (xcorevss)	C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32	—	—	—
SGND_SRDS2	SerDes Transceiver Core Logic GND (xcorevss)	AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32	—	—	—
AGND_SRDS1	SerDes PLL GND	J31	—	—	—
AGND_SRDS2	SerDes PLL GND	AH31	—	—	—
OVDD	General I/O Supply	U31, V24, V28, Y31, AA27, AB25, AB29	—	OVDD	—
LVDD	TSEC 1&2 I/O Supply	AC18, AC21, AG21, AL27	—	LVDD	—
TVDD	TSEC 3&4 I/O Supply	AC15, AE16, AH18	—	TVDD	—
GVDD	SSTL_1.8 DDR Supply	B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2	—	GVDD	—
BVDD	Local Bus and GPIO Supply	A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20	—	BVDD	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω (±1%) to GND	—
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	O	AVDD_S RDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	I	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	I	100Ω (±1%) to GND	—
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	O	AVDD_S RDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	—	internal diode	14
No Connection Pins					

Table 78. Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, "CCB/SYSCLK PLL Ratio,"](#) [Section 19.3, "e500 Core PLL Ratio,"](#) and [Section 19.4, "DDR/DDRCLK PLL Ratio,"](#) for ratio settings.
- The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn_MCK}}[0:5]$ output clocks, running at half of the DDR data rate.
- In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to [Section 19.4, "DDR/DDRCLK PLL Ratio."](#) The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in [Table 80](#) and [Table 81](#);
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from [Table 79](#);
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from [Table 82](#). Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in [Table 79](#):

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA_DACK}}[0:1]$, EC5_MDC, $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY_P0/QUIESCE, MSRCID[2:4], MDVAL, and ASLEEP. The $\overline{\text{TEST_SEL}}$ pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $\text{OV}_{\text{DD}}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $\text{OV}_{\text{DD}}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

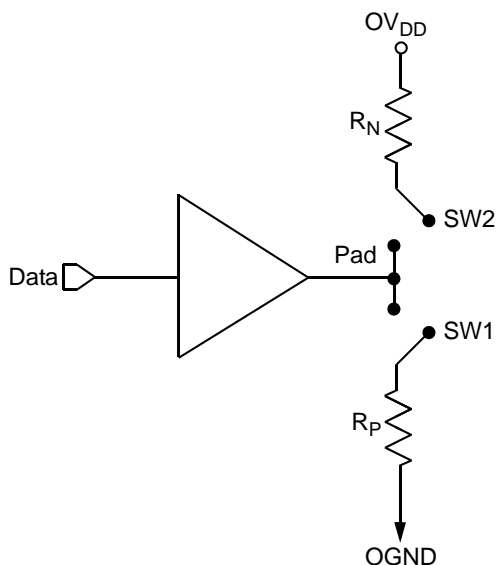


Figure 64. Driver Impedance Measurement

22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 22.1, “Part Numbers Fully Addressed by this Document.”](#)

22.1 Part Numbers Fully Addressed by this Document

[Table 86](#) through [Table 88](#) provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 86. Part Numbering Nomenclature—Rev 2.2.1

MPC	nnnn	e	t	l	pp	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = -40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA ⁴ VJ = Fully Pb-free FC-PBGA ⁵	AVN = 1500-MHz processor; 800 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included
		Blank = Not included				AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included

Notes:

- ¹ MPC stands for “Qualified.”
PPC stands for “Prototype”
- ² See [Section 18, “Package Description,”](#) for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- ⁴ The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.
- ⁵ The VJ part number is entirely lead-free. This includes the C4 die bumps.

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