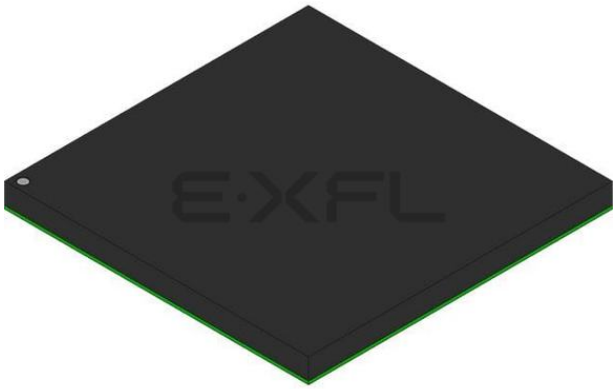

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572elpxavnd

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Range	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface	—	–0.3 to 1.65		—
Three-speed Ethernet I/O, FEC management interface, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2) TV_{DD} (for eTSEC3 and eTSEC4, FEC)	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 3.63 –0.3 to 2.75	V — —	2 2
DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus and GPIO I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 and DDR3 SDRAM interface reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus and GPIO signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 14 provides the current draw characteristics for $MV_{REF}n$.

Table 14. Current Draw Characteristics for MV_{REF} *n*

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	$I_{MVREF}n$	—	1500	µA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	>=667 MHz	V_{ILAC}	—	$MV_{REF}n$ – 0.20	V	—
	<= 533 MHz		—	$MV_{REF}n$ – 0.25		
AC input high voltage	>=667 MHz	V_{IHAC}	$MV_{REF}n$ + 0.20	—	V	—
—	<= 533 MHz		$MV_{REF}n$ + 0.25	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REF}n$ – 0.175	V	—
AC input high voltage	V_{IHAC}	$MV_{REF}n$ + 0.175	—	V	—

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 MHz	—	–200	200	—	—
667 MHz	—	–240	240	—	—
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW.This can be determined by the following equation: tDISKEW =+/–(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

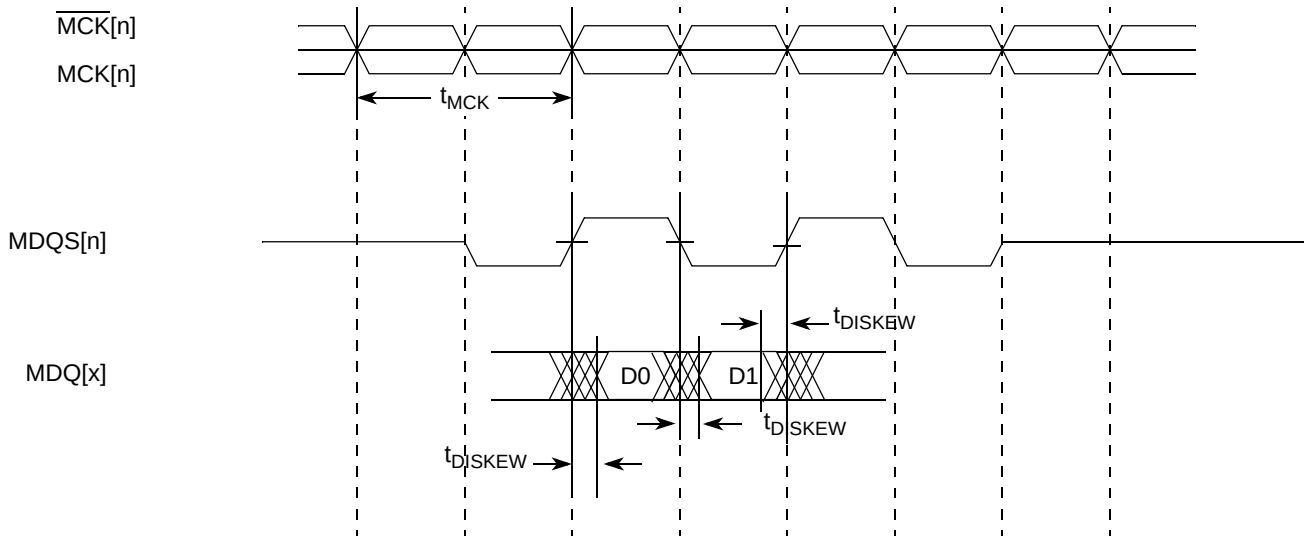

Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:
1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V .

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 8.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

Table 25. FIFO Mode Transmit AC Timing Specification (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Notes:

1. The minimum cycle period (or maximum frequency) of the TX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Table 26. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period[1]	t_{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Figure 7 and Figure 8 show the FIFO timing diagrams.

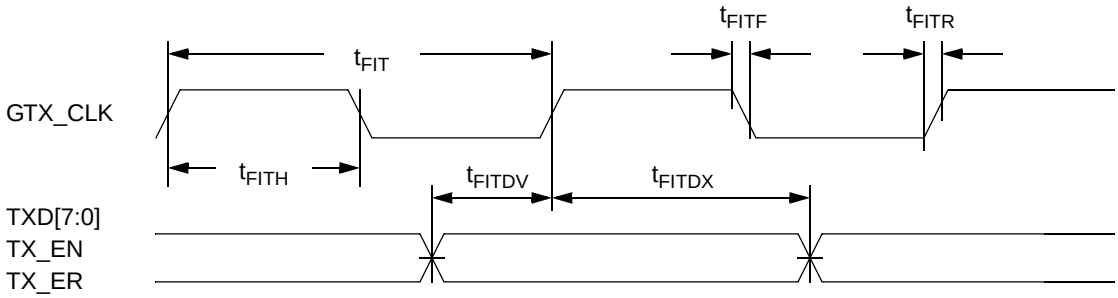

Figure 7. FIFO Transmit AC Timing Diagram

Figure 16 shows the TBI receive AC timing diagram.

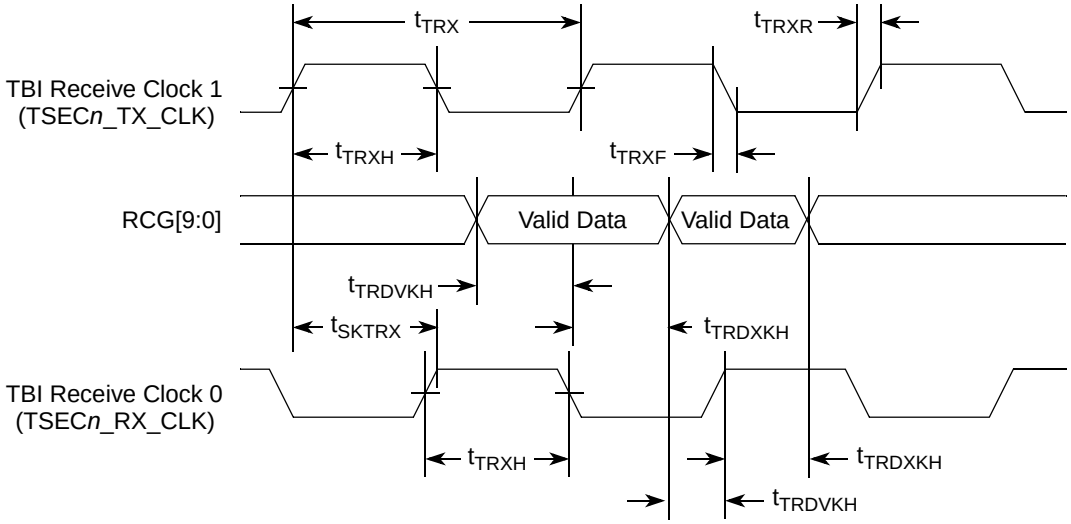

Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	—	—	ns

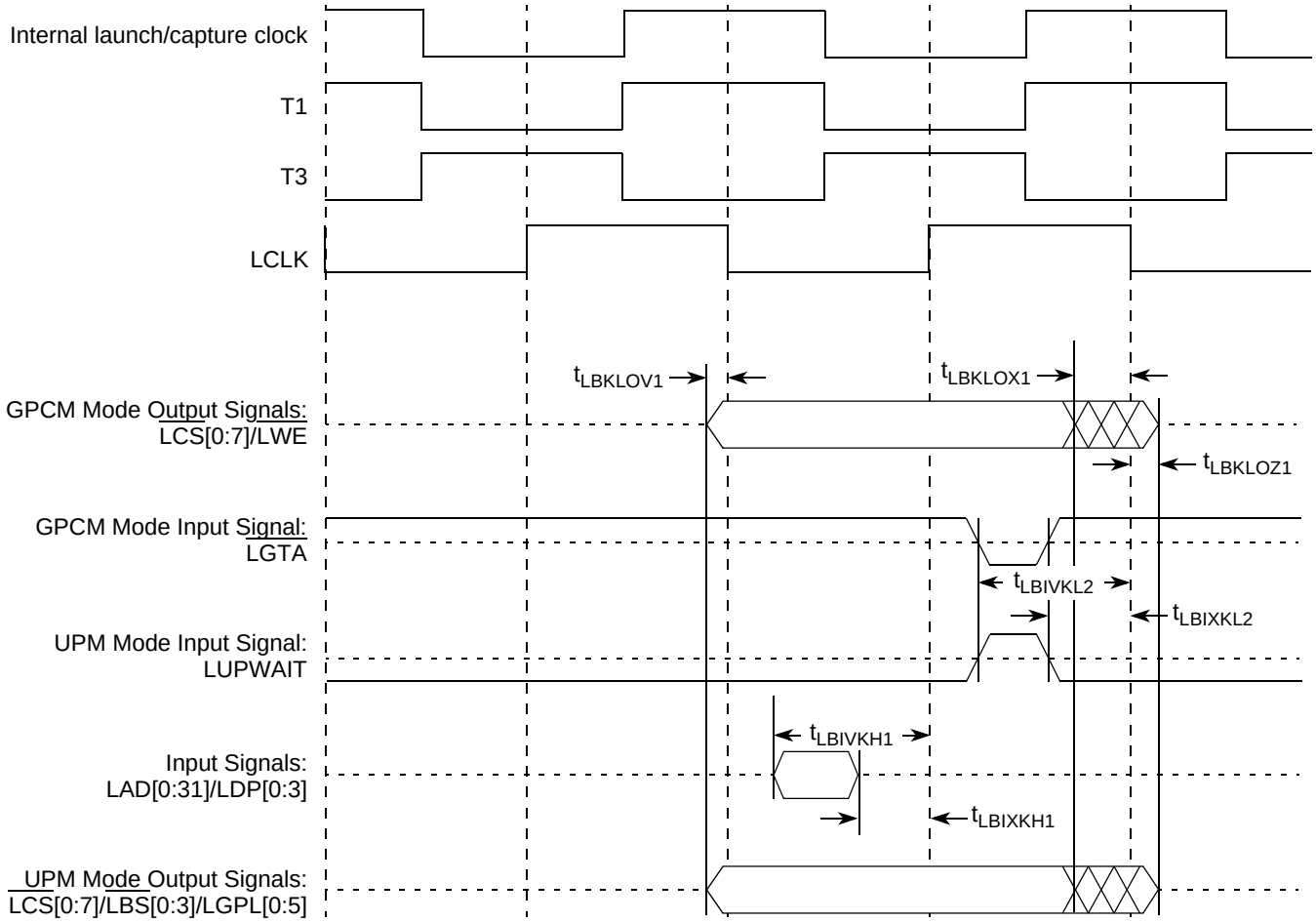

Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.

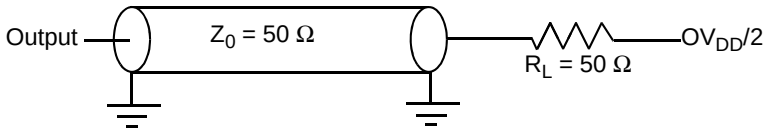

Figure 36. AC Test Load for the JTAG Interface

Figure 37 provides the JTAG clock input timing diagram.

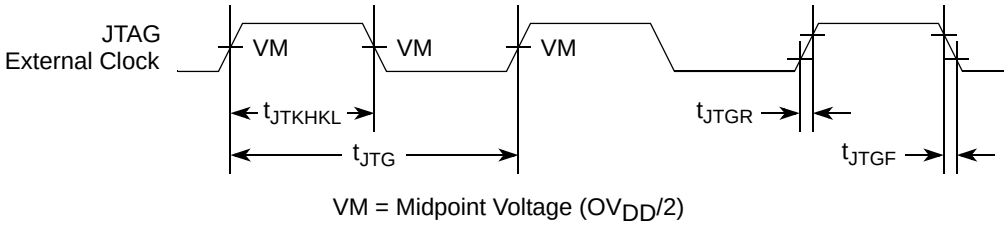

Figure 37. JTAG Clock Input Timing Diagram

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.

Table 54. I²C DC Electrical Characteristics (continued)

Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

Table 55 provides the AC timing parameters for the I²C interfaces.

Table 55. I²C AC Electrical Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 2).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz[4]
Low period of the SCL clock	t_{I2CL}	1.3	—	µs
High period of the SCL clock	t_{I2CH}	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs
Data setup time	t_{I2DVKH}	100	—	ns
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — —	µs
Data output delay time	t_{I2OVKL}	—	0.9[3]	µs
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

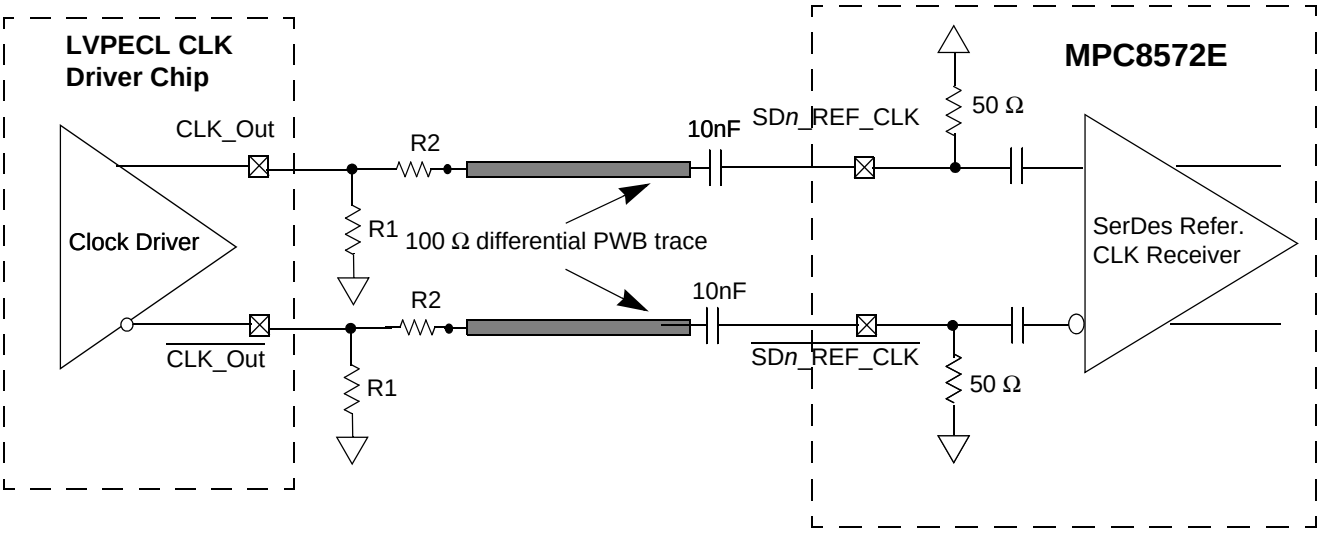

Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

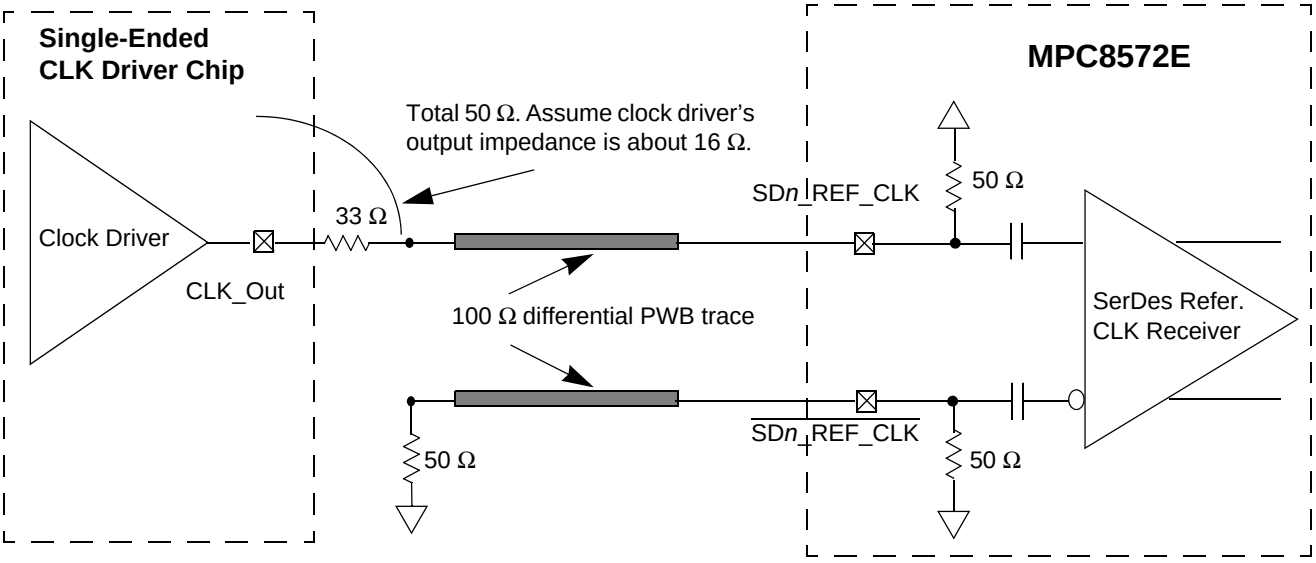

Figure 51. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

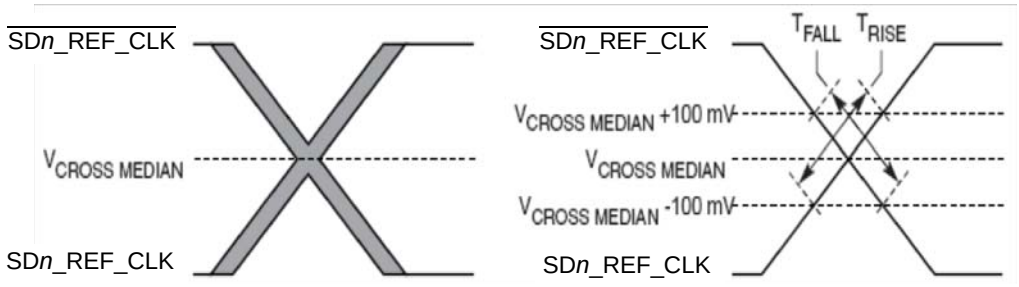

Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$"
- Section 16.2, "AC Requirements for PCI Express SerDes Reference Clocks"
- Section 17.2, "AC Requirements for Serial RapidIO SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$"

15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ are designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane's transmitter and receiver.

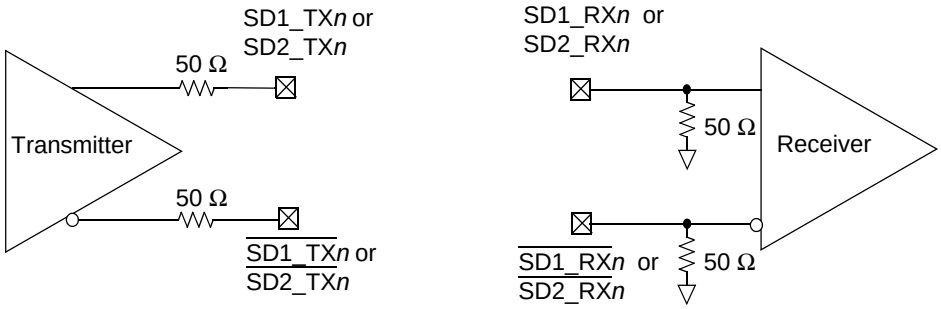

Figure 54. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 16, "PCI Express"

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

17.8.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

17.8.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

17.8.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 17.6, “Receiver Specifications,” and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 60 and Table 75. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 17.6, “Receiver Specifications,” is then added to the signal and the test load is replaced by the receiver being tested.

18 Package Description

This section describes package parameters, pin assignments, and dimensions.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0]	Receive Data Valid	AL24	I	LV_{DD}	1
TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1]	Receive Data Error	AM29	I	LV_{DD}	1
TSEC1_TX_CLK/FIFO1_TX_CLK	Transmit Clock In	AB20	I	LV_{DD}	1
TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0]	Transmit Enable	AJ24	O	LV_{DD}	1, 22
TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1]	Transmit Error	AK25	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 2					
TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8]	Receive Data	AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20	I	LV_{DD}	1
TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8]	Transmit Data	AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18	O	LV_{DD}	1, 5, 9, 24
TSEC2_COL/FIFO2_TX_FC	Collision Detect/Flow Control	AE19	I	LV_{DD}	1
TSEC2_CRS/FIFO2_RX_FC	Carrier Sense/Flow Control	AJ20	I/O	LV_{DD}	1, 16
TSEC2_GTX_CLK	Transmit Clock Out	AE18	O	LV_{DD}	—
TSEC2_RX_CLK/FIFO2_RX_CLK	Receive Clock	AL23	I	LV_{DD}	1
TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2]	Receive Data Valid	AJ22	I	LV_{DD}	1
TSEC2_RX_ER/FIFO2_RX_ER	Receive Data Error	AD19	I	LV_{DD}	1
TSEC2_TX_CLK/FIFO2_TX_CLK	Transmit Clock In	AC19	I	LV_{DD}	1
TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2]	Transmit Enable	AB19	O	LV_{DD}	1, 22
TSEC2_TX_ER/FIFO2_TX_ERR	Transmit Error	AB17	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 3					
TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0]	Transmit Data	AG18, AG17, AH17, AH19	O	TV_{DD}	1, 5, 9
TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0]	Receive Data	AG16, AK19, AD16, AJ19	I	TV_{DD}	1

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals					
GND	Ground	A18, A25, A29, C3, C6, C9, C12, C15, C20, C22, E5, E8, E11, E14, F3, G7, G10, G13, G16, H5, H21, J3, J9, J12, J18, K7, L5, L13, L15, L16, L21, M3, M9, M12, M14, M16, M18, N7, N13, N15, N17, N19, N21, N23, P5, P12, P14, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, R26, T7, T12, T14, T16, T18, T20, T22, T30, U5, U11, U13, U15, U16, U17, U19, U21, U23, U25, V3, V9, V12, V14, V16, V18, V20, V22, W7, W11, W13, W15, W17, W19, W21, W27, W32, Y5, Y12, Y14, Y16, Y18, Y20, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA30, AB7, AB26, AC5, AC11, AC13, AD3, AD9, AD14, AD17, AD22, AE7, AE13, AF5, AF11, AG3, AG9, AG15, AG19, AH7, AH13, AH22, AJ5, AJ11, AJ17, AK3, AK9, AK15, AK24, AL7, AL13, AL19, AL26	—	—	—
XGND_SRDS1	SerDes Transceiver Pad GND (xpadvss)	C23, C27, D23, D25, E23, E26, F23, F24, G23, G27, H23, H25, J23, J26, K23, K24, L27, M25	—	—	—
XGND_SRDS2	SerDes Transceiver Pad GND (xpadvss)	AD23, AD25, AE23, AE27, AF23, AF24, AG23, AG26, AH23, AH25, AJ27	—	—	—

Table 82. DDR Clock Ratio (continued)

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
101	12:1
110	14:1
111	Synchronous mode

19.5 Frequency Options

19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

Table 83. Frequency Options for Platform Frequency

CCB to SYSCLK Ratio	SYSCLK (MHz)							
	33.33	41.66	50	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)							
4						400	444	533
5					415	500	555	
6				400	498	600		
8			400	533				
10		417	500					
12	400	500	600					

19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, “I/O Port Selection,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, “Link Width,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the “PCI Express link width”

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

Table 90. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
6	06/2014	• Updated Table 76, “MPC8572E Pinout Listing,” TDO signal is not driven during HRSET* assertion. • In Table 86, “Part Numbering Nomenclature—Rev 2.2.1,“ added full Pb-free part code.
5	01/2011	• Editorial changes throughout • Updated Table 4, “MPC8572E Power Dissipation,” to include low power product. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” defined PPC as “Prototype” and changed table headings to say “Package Sphere Type”. • Added Table 86, “Part Numbering Nomenclature—Rev 2.2.1.”
4	06/2010	• In Section 18.3, “Pinout Listings,” updated Table 76 showing GPINOUT power rail as BVDD. • Updated Section 14.1, “GPIO DC Electrical Characteristics.”
3	03/2010	• In Section 2.1, “Overall DC Electrical Characteristics,” changed GPIO power from OVDD to BVDD. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” added Table 87 for Rev 2.1 silicon. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” updated Table 88 for Rev 1.1.1 silicon.
2	06/2009	• In Section 3, “Power Characteristics,” updated CCB Max to 533MHz for 1200MHz core device in Table 5, “MPC8572EL Power Dissipation.” • In Section 4.4, “DDR Clock Timing,” changed DDRCLK Max to 100MHz. This change was announced in Product Bulletin #13572. • Clarified restrictions in Section 4.5, “Platform to eTSEC FIFO Restrictions.” • In Table 9, “RESET Initialization Timing Specifications,” added note 2. • Added Section 14, “GPIO.” • In Section 18.1, “Package Parameters for the MPC8572E FC-PBGA,” updated material composition to 63% Sn, 37% Pb. • In Section 18.2, “Mechanical Dimensions of the MPC8572E FC-PBGA, updated Figure 61 to correct the package thickness and top view. • In Section 19.1, “Clock Ranges,” updated CCB Max to 533MHz for 1200MHz core device in Table 77, “MPC8572E Processor Core Clocking Specifications.” • In Section 19.5.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces,” changed minimum CCB clock frequency for proper PCI Express operation. • Added LPBSE to description of LGPL4/LGTA/LUPWAIT/LPBSE/LFRB signal in Table 76, “MPC8572E Pinout Listing.” • Corrected supply voltage for GPIO pins in Table 76, “MPC8572E Pinout Listing.” • Applied note to SD1_PLL_TPA in Table 76, “MPC8572E Pinout Listing.” • Updated note regarding MDIC in Table 76, “MPC8572E Pinout Listing.” • Added note for LAD pins in Table 76, “MPC8572E Pinout Listing.” • Updated Table 88, “,Part Numbering Nomenclature—Rev 1.1.1” with Rev 2.0 and Rev 2.1 part number information. Added note indicating that silicon version 2.0 is available for prototype purposes only and will not be available as a qualified device.
1	08/2008	• In Section 22.1, “Part Numbers Fully Addressed by this Document,” added SVR information in, Table 88 “Part Numbering Nomenclature—Rev 1.1.1,” for devices without Security Engine feature.
0	07/2008	• Initial release.