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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

| | |
|---------------------------------|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.2GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 1023-BFBGA, FCBGA |
| Supplier Device Package | 1023-FCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572epxatld |

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

Table 8. DDRCLK AC Timing Specifications (continued)

 At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---------------------|--------|-----|---------|---------|------|---------|
| DDRCLK jitter | — | — | — | +/- 150 | ps | 4, 5, 6 |

Notes:

- Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
- Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The DDRCLK driver’s closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock (CCB) frequency} / 4.2$$

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock (CCB) frequency} / 3.2$$

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

[Table 9](#) describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

| Parameter/Condition | Min | Max | Unit | Notes |
|---|-----|-----|---------------|-------|
| Required assertion time of $\overline{\text{HRESET}}$ | 100 | — | μs | 2 |
| Minimum assertion time for $\overline{\text{SRESET}}$ | 3 | — | SYCLKs | 1 |

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with $G_{V_{DD}}$ of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|---------------------|---------------------|-------------------------------|-------------------------------|------|-------|
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQS preamble start | t_{DDKHMP} | | | ns | 6 |
| 800 MHz | | $-0.5 \times t_{MCK} - 0.375$ | $-0.5 \times t_{MCK} + 0.375$ | | |
| ≤ 667 MHz | | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | | |
| MDQS epilogue end | t_{DDKHME} | | | ns | 6 |
| 800 MHz | | -0.375 | 0.375 | | |
| ≤ 667 MHz | t_{DDKHME} | -0.6 | 0.6 | ns | 6 |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the $MCK[n]$ clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the $TIMING_CFG_2$ register. This typically be set to the same delay as in $DDR_SDRAM_CLK_CNTL[CLK_ADJUST]$. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of $MCK[n]$ at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

| Parameter | Value | Unit | Notes |
|-------------------|---------------------|------|---------|
| Minimum baud rate | $f_{CCB}/1,048,576$ | baud | 1, 2 |
| Maximum baud rate | $f_{CCB}/16$ | baud | 1, 2, 3 |
| Oversample rate | 16 | — | 1, 4 |

Notes:

1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

The electrical characteristics for SGMII is specified in [Section 8.3, “SGMII Interface Electrical Characteristics.”](#) The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in [Table 24](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------------------|------|-----------------------|---------------|---------|
| Supply voltage 3.3 V | V_{DD} V_{DD} | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($V_{DD}/V_{DD} = \text{Min}$, $I_{OH} = -4.0 \text{ mA}$) | V_{OH} | 2.40 | $V_{DD}/V_{DD} + 0.3$ | V | — |
| Output low voltage ($V_{DD}/V_{DD} = \text{Min}$, $I_{OL} = 4.0 \text{ mA}$) | V_{OL} | GND | 0.50 | V | — |
| Input high voltage | V_{IH} | 2.0 | $V_{DD}/V_{DD} + 0.3$ | V | — |
| Input low voltage | V_{IL} | -0.3 | 0.90 | V | — |
| Input high current ($V_{IN} = V_{DD}$, $V_{IN} = V_{DD}$) | I_{IH} | — | 40 | μA | 1, 2, 3 |
| Input low current ($V_{IN} = \text{GND}$) | I_{IL} | -600 | — | μA | 3 |

Notes:

¹ V_{DD} supports eTSECs 1 and 2.

² V_{DD} supports eTSECs 3 and 4 or FEC.

³ The symbol V_{IN} , in this case, represents the V_{IN} and V_{IN} symbols referenced in [Table 1](#).

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

| Parameters | Symbol | Min | Max | Unit | Notes |
|--|-----------------|-----------|-----------------------|------|-------|
| Supply voltage 2.5 V | V_{DD}/V_{DD} | 2.37 | 2.63 | V | 1, 2 |
| Output high voltage ($V_{DD}/V_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$) | V_{OH} | 2.00 | $V_{DD}/V_{DD} + 0.3$ | V | — |
| Output low voltage ($V_{DD}/V_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$) | V_{OL} | GND - 0.3 | 0.40 | V | — |
| Input high voltage | V_{IH} | 1.70 | $V_{DD}/V_{DD} + 0.3$ | V | — |
| Input low voltage | V_{IL} | -0.3 | 0.70 | V | — |

Figure 16 shows the TBI receive AC timing diagram.

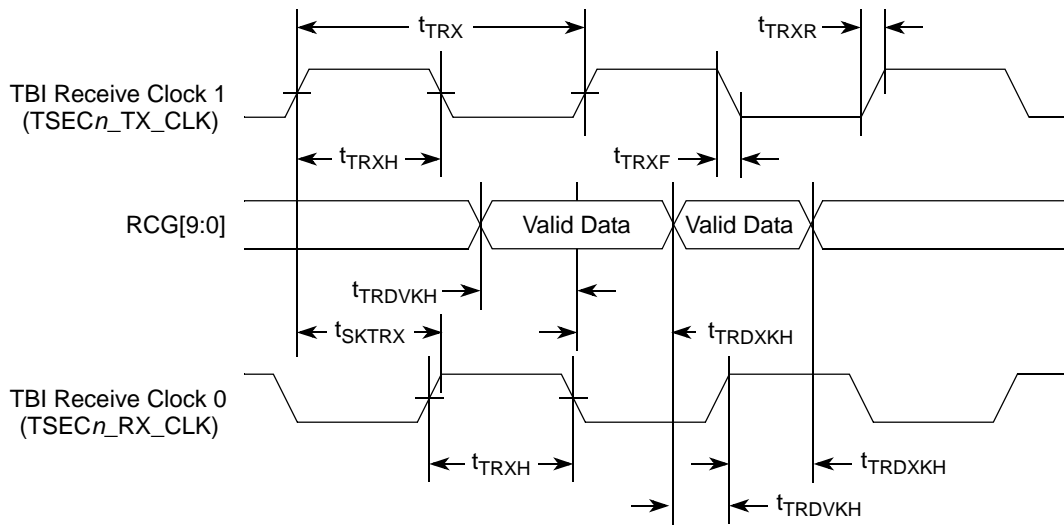


Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC_n pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|--------------------------------------|-----|-----|-----|------|
| RX_CLK clock period | t _{TRRX} | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | t _{TRRH} /t _{TRRX} | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | t _{TRRJ} | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | t _{TRRR} | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | t _{TRRF} | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | t _{TRRDVKH} | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | t _{TRRDVKH} | 1.0 | — | — | ns |

Figure 17 shows the TBI receive the timing diagram.

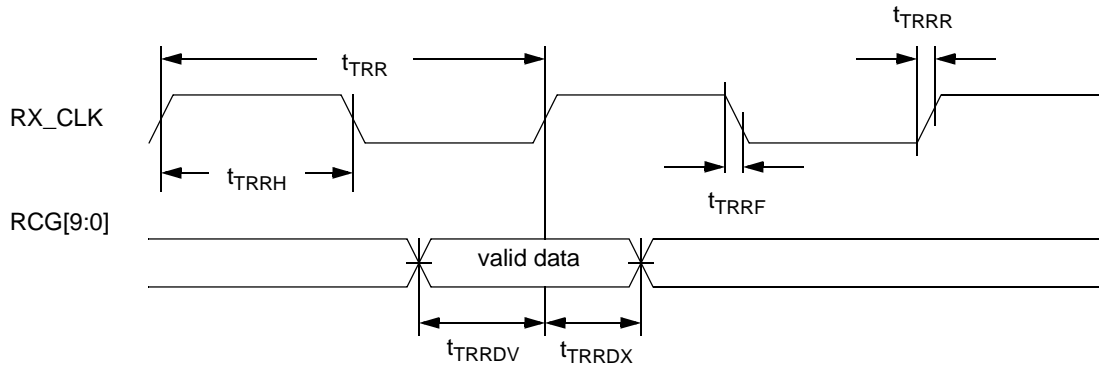


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of $2.5\text{ V} \pm 5\%$.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|--|---------------------|------|-----|------|------|
| Data to clock output skew (at transmitter) | t_{SKRGT} | -500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) ² | t_{SKRGT} | 1.0 | — | 2.8 | ns |
| Clock period ³ | t_{RGT} | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX ^{3, 4} | t_{RGTH}/t_{RGT} | 40 | 50 | 60 | % |
| Rise time (20%–80%) | t_{RGTR} | — | — | 0.75 | ns |
| Fall time (20%–80%) | t_{RGTF} | — | — | 0.75 | ns |

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to $400\text{ ns} \pm 40\text{ ns}$ and $40\text{ ns} \pm 4\text{ ns}$, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

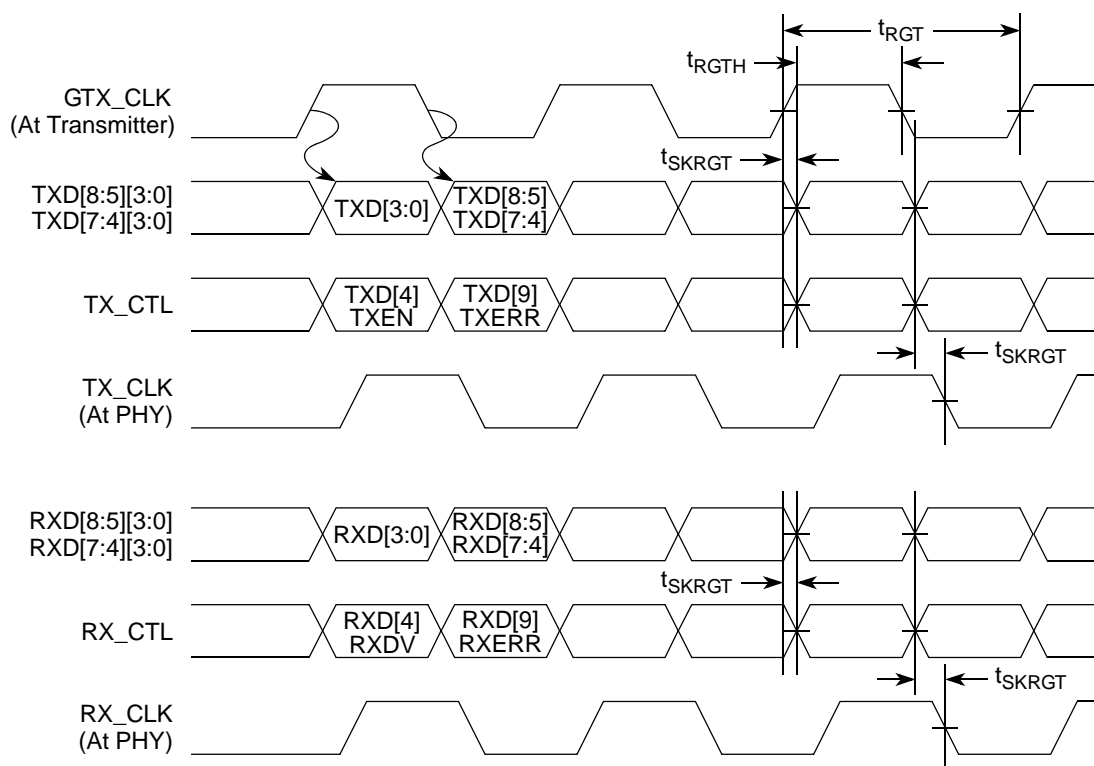


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMI AC Timing Specifications

This section describes the RMI transmit and receive AC timing specifications.

8.2.7.1 RMI Transmit AC Timing Specifications

Table 35 shows the RMI transmit AC timing specifications.

Table 35. RMI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|----------------------------------|---------------------|------|------|------|------|
| TSECn_TX_CLK clock period | t _{RMT} | 15.0 | 20.0 | 25.0 | ns |
| TSECn_TX_CLK duty cycle | t _{RMTH} | 35 | 50 | 65 | % |
| TSECn_TX_CLK peak-to-peak jitter | t _{RMTJ} | — | — | 250 | ps |
| Rise time TSECn_TX_CLK (20%–80%) | t _{RMTR} | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | t _{RMTF} | 1.0 | — | 2.0 | ns |

6. Differential Waveform

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the non-inverting signal (SDn_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to [Figure 52](#) as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

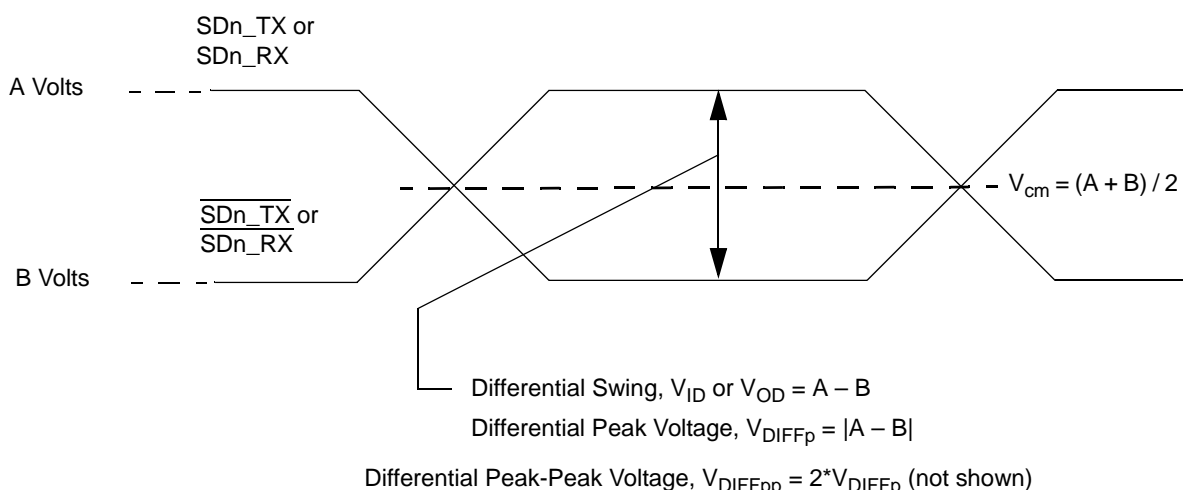


Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and \overline{TD} , has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

- To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{SDn_REF_CLK}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

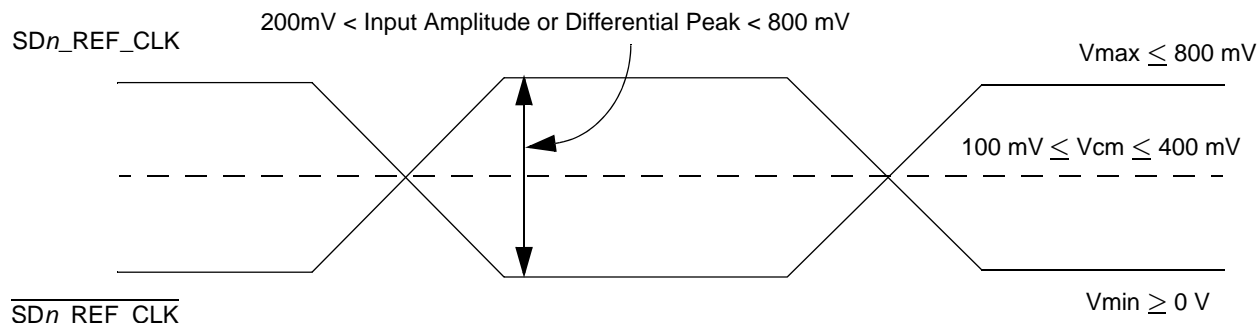


Figure 45. Differential Reference Clock Input DC Requirements (External DC-Coupled)

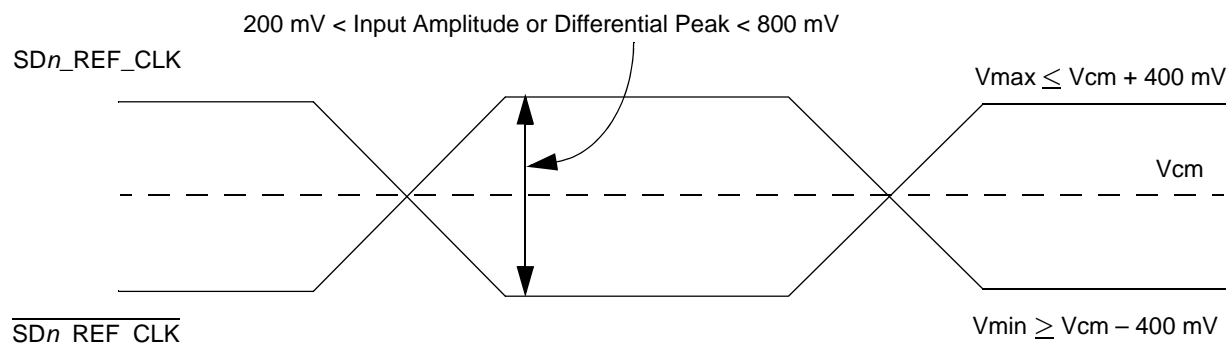


Figure 46. Differential Reference Clock Input DC Requirements (External AC-Coupled)

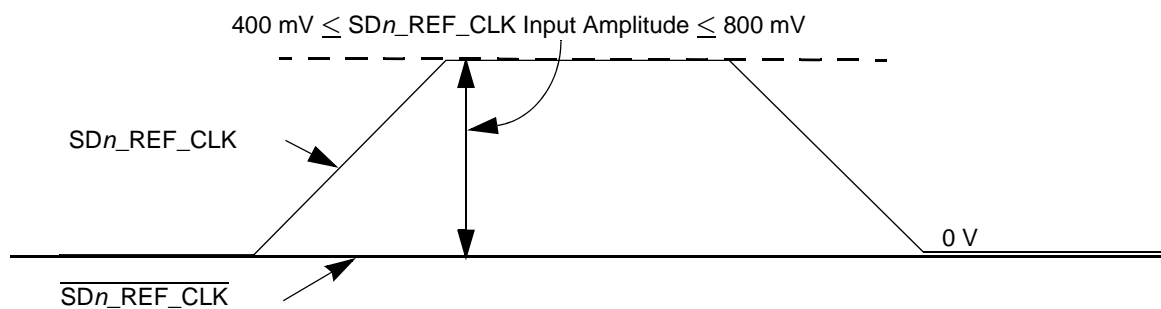


Figure 47. Single-Ended Reference Clock Input DC Requirements

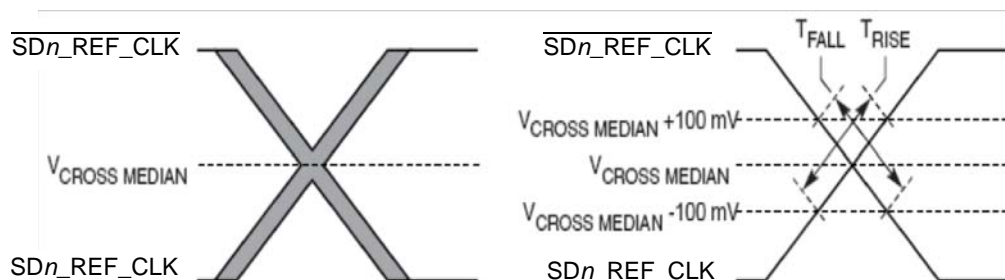


Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- [Section 8.3.2, “AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK”](#)
- [Section 16.2, “AC Requirements for PCI Express SerDes Reference Clocks”](#)
- [Section 17.2, “AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK”](#)

15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/SD1_REF_CLK are designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/SD2_REF_CLK are not to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane’s transmitter and receiver.

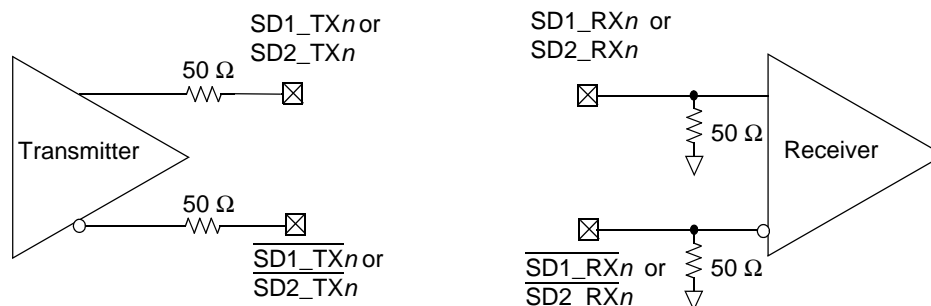


Figure 54. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- [Section 8.3, “SGMII Interface Electrical Characteristics”](#)
- [Section 16, “PCI Express”](#)

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)

| Characteristic | Symbol | Range | | Unit | Notes |
|----------------------|----------|-------|------|------|--|
| | | Min | Max | | |
| Multiple Output skew | S_{MO} | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | +/- 100 ppm |

Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud

| Characteristic | Symbol | Range | | Unit | Notes |
|-----------------------------|--------------|-------|------|--------|--|
| | | Min | Max | | |
| Output Voltage, | V_O | -0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | V_{DIFFPP} | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | J_D | — | 0.17 | UI p-p | — |
| Total Jitter | J_T | — | 0.35 | UI p-p | — |
| Multiple output skew | S_{MO} | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/- 100 ppm |

Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud

| Characteristic | Symbol | Range | | Unit | Notes |
|-----------------------------|--------------|-------|------|--------|--|
| | | Min | Max | | |
| Output Voltage, | V_O | -0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | V_{DIFFPP} | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | J_D | — | 0.17 | UI p-p | — |
| Total Jitter | J_T | — | 0.35 | UI p-p | — |
| Multiple output skew | S_{MO} | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | +/- 100 ppm |

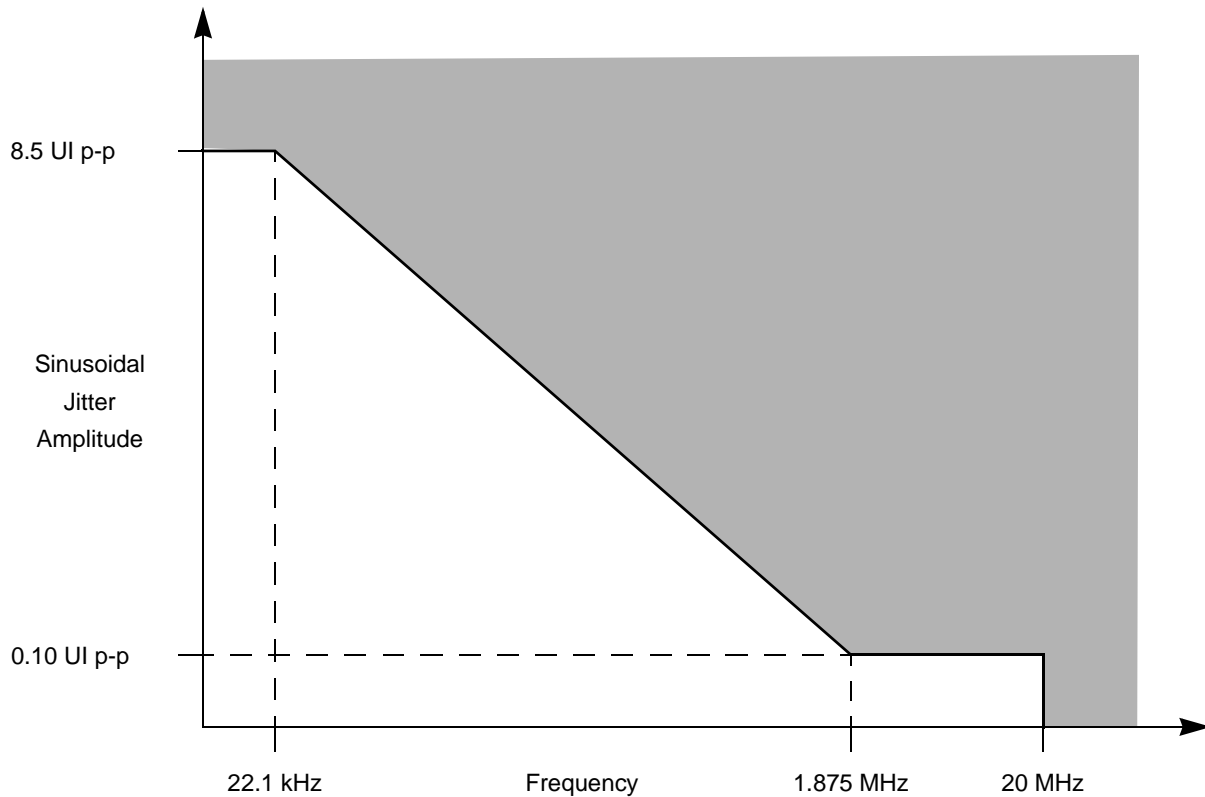


Figure 59. Single Frequency Sinusoidal Jitter Limits

17.7 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 72, Table 73, and Table 74) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 60 with the parameters specified in Table 75. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\text{-}\Omega \pm 5\%$ differential resistive load.

Table 76. MPC8572E Pinout Listing (continued)

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|--------------------------------|-----------------------------|--------------------|----------|------------------|-----------|
| MSRCID[0:1] | Memory Debug Source Port ID | U27, T29 | O | OV _{DD} | 5, 9, 30 |
| MSRCID[2:4] | Memory Debug Source Port ID | U28, W24, W28 | O | OV _{DD} | 21 |
| MDVAL | Memory Debug Data Valid | V26 | O | OV _{DD} | 2, 21 |
| CLK_OUT | Clock Out | U32 | O | OV _{DD} | 11 |
| Clock | | | | | |
| RTC | Real Time Clock | V25 | I | OV _{DD} | — |
| SYSCLK | System Clock | Y32 | I | OV _{DD} | — |
| DDRCLK | DDR Clock | AA29 | I | OV _{DD} | 31 |
| JTAG | | | | | |
| TCK | Test Clock | T28 | I | OV _{DD} | |
| TDI | Test Data In | T27 | I | OV _{DD} | 12 |
| TDO | Test Data Out | T26 | O | OV _{DD} | — |
| TMS | Test Mode Select | U26 | I | OV _{DD} | 12 |
| $\overline{\text{TRST}}$ | Test Reset | AA32 | I | OV _{DD} | 12 |
| DFT | | | | | |
| L1_TSTCLK | L1 Test Clock | V32 | I | OV _{DD} | 18 |
| L2_TSTCLK | L2 Test Clock | V31 | I | OV _{DD} | 18 |
| $\overline{\text{LSSD_MODE}}$ | LSSD Mode | N24 | I | OV _{DD} | 18 |
| $\overline{\text{TEST_SEL}}$ | Test Select 0 | K28 | I | OV _{DD} | 18 |
| Power Management | | | | | |
| ASLEEP | Asleep | P28 | O | OV _{DD} | 9, 15, 21 |

Table 78. Memory Bus Clocking Specifications

| Characteristic | Min | Max | Unit | Notes |
|----------------------------|-----|-----|------|------------|
| Memory bus clock frequency | 200 | 400 | MHz | 1, 2, 3, 4 |

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, "CCB/SYSCLK PLL Ratio,"](#) [Section 19.3, "e500 Core PLL Ratio,"](#) and [Section 19.4, "DDR/DDRCLK PLL Ratio,"](#) for ratio settings.
- The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn_MCK}}[0:5]$ output clocks, running at half of the DDR data rate.
- In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to [Section 19.4, "DDR/DDRCLK PLL Ratio."](#) The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in [Table 80](#) and [Table 81](#);
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from [Table 79](#);
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from [Table 82](#). Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in [Table 79](#):

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 19.2, “CCB/SYSCLK PLL Ratio.”](#) The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 19.3, “e500 Core PLL Ratio.”](#)
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

21.2 Power Supply Design

21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CORE0} , AV_{DD_CORE1} , AV_{DD_DDR} , AV_{DD_LBIU} , AV_{DD_SRDS1} and AV_{DD_SRDS2} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 62](#), one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.

Figure 62 shows the PLL power supply filter circuits.

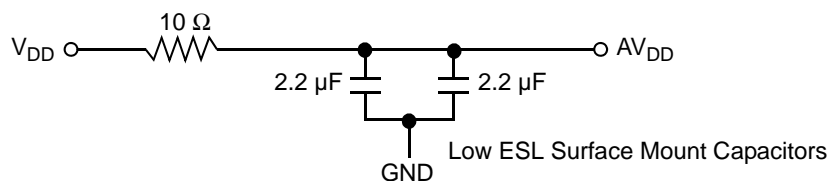
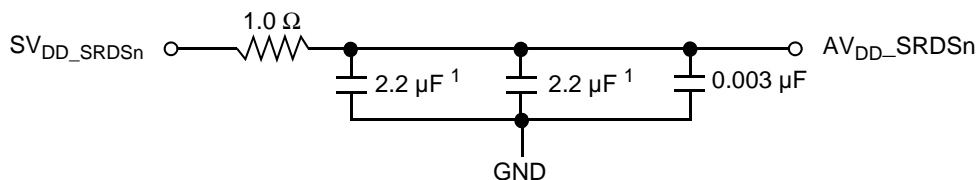


Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD_SRDSn} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD_SRDSn} ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

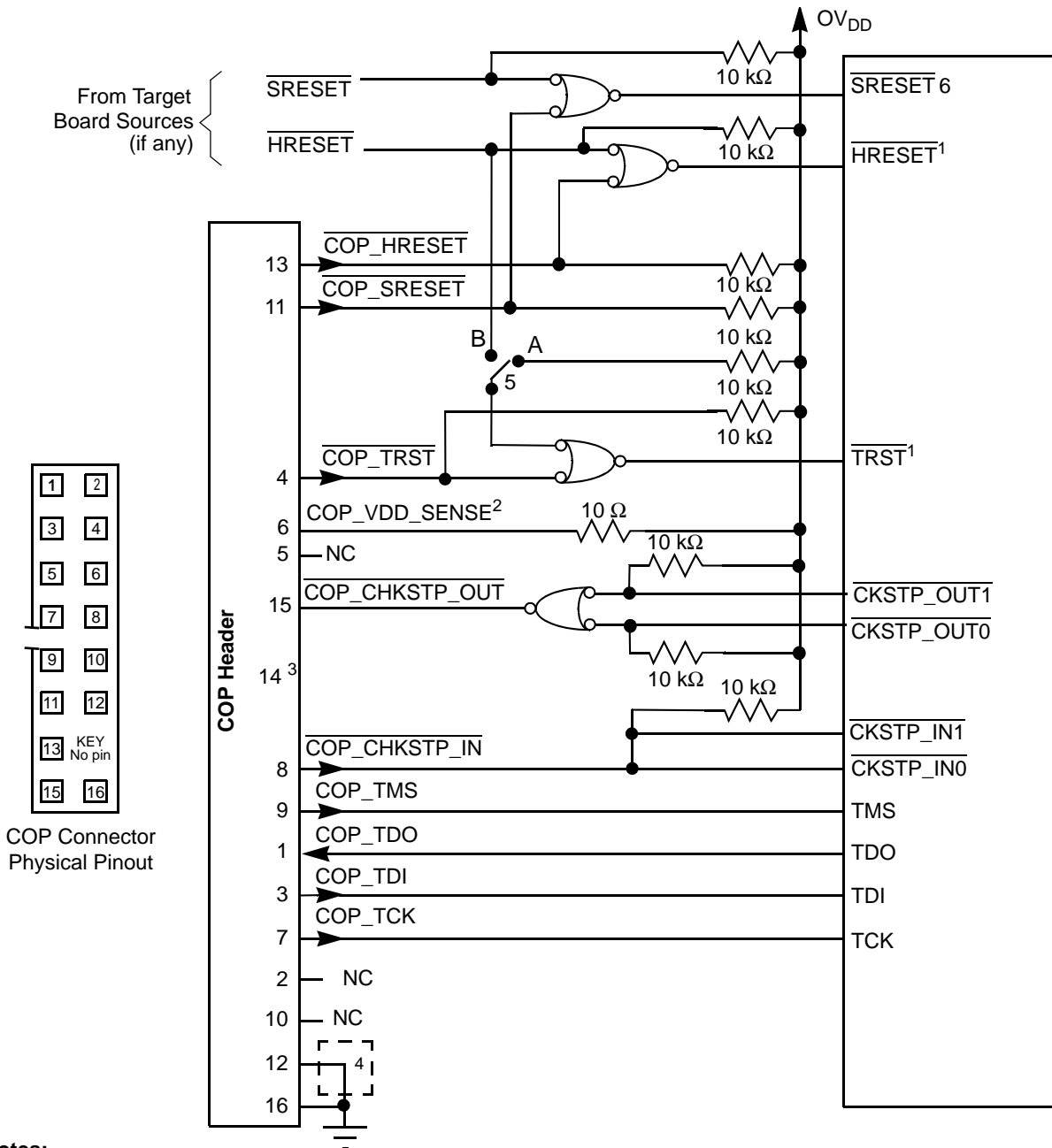
AV_{DD_SRDSn} should be a filtered version of SV_{DD_SRDSn} .

NOTE

Signals on the SerDes interface are fed from the XV_{DD_SRDSn} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 cores.

21.10.3 SerDes 2 Interface (SGMII) Entirely Unused

If the high-speed SerDes 2 interface (SGMII) is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2_TX}}[3:0]$
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2_RX}}[3:0]$
- SD2_REF_CLK
- $\overline{\text{SD2_REF_CLK}}$

The POR configuration pin `cfg_srds_sgmii_en` on $\overline{\text{UART_RTS}}[1]$ can be used to power down SerDes 2 block for power saving. Note that both SVDD_SRDS2 and XVDD_SRDS2 must remain powered.

21.10.4 SerDes 2 Interface (SGMII) Partly Unused

If only part of the high speed SerDes 2 interface (SGMII) pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2_TX}}[3:0]$
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2_RX}}[3:0]$

22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 22.1, “Part Numbers Fully Addressed by this Document.”](#)

22.1 Part Numbers Fully Addressed by this Document

[Table 86](#) through [Table 88](#) provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 86. Part Numbering Nomenclature—Rev 2.2.1

| MPC | nnnn | e | t | l | pp | ffm | r |
|---------------------------|-----------------|----------------------|--|-----------------------------|--|--|--|
| Product Code ¹ | Part Identifier | Security Engine | Temperature | Power | Package Sphere Type ² | Processor Frequency/DDR Data Rate ³ | Silicon Revision |
| MPC PPC | 8572 | E = Included | Blank = 0 to 105°C C = -40 to 105°C | Blank = Standard L = Low | PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA ⁴ VJ = Fully Pb-free FC-PBGA ⁵ | AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate | E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included |
| | | Blank = Not included | | | | | |

Notes:

- ¹ MPC stands for “Qualified.”
PPC stands for “Prototype”
- ² See [Section 18, “Package Description,”](#) for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- ⁴ The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.
- ⁵ The VJ part number is entirely lead-free. This includes the C4 die bumps.