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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572epxaulb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Table 4	MPC8572F	Power	Dissir	nation ¹
		I OWEI	Diagih	Jation

Notes:

¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.

 $^2~$ Typical-65 is based on V_DD = 1.1 V, T_j = 65 °C, running Dhrystone.

³ Typical-105 is based on V_{DD} = 1.1 V, T_i = 105 °C, running Dhrystone.

⁴ Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Table 5. MPC8572EL Power Dissipation ¹

Notes:

¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.

² Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.

³ Typical-105 is based on V_{DD} = 1.1 V, T_i = 105 °C, running Dhrystone.

 4 Maximum is based on V_{DD} = 1.1 V, T_i = 105 °C, running a smoke test.

DDR2 and DDR3 SDRAM Controller

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Output low current ($V_{OUT} = 0.280 V$)	I _{OL}	13.4		mA	_

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm GV}_{\rm DD}$ at all times.

- 2. $MV_{REF}n$ is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to MV_{REF}*n*. This rail should track variations in the DC level of MV_{REF}*n*.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV _{DD}	1.425	1.575	V	1
I/O reference voltage	MV _{REF} n	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
Input high voltage	V _{IH}	$MV_{REF}n + 0.100$	GV _{DD}	V	—
Input low voltage	V _{IL}	GND	MV _{REF} <i>n</i> – 0.100	V	—
Output leakage current	I _{OZ}	-50	50	μA	3

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm GV}_{\rm DD}$ at all times.

2. $MV_{REF}n$ is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.

3. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Мах	Unit
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.175 V.



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Figure 16 shows the TBI receive AC timing diagram.



Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
RX_CLK clock period	t _{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH} /t _{TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}	_	_	250	ps
Rise time RX_CLK (20%-80%)	t _{TRRR}	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXKH}	1.0		_	ns



Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol ¹	Min	Мах	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-1.3	_	ns	4, 5
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t _{LBOTOT}	1.5	_	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	_	-0.3	ns	
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	_	-0.1	ns	4
Local bus clock to address valid for LAD	t _{LBKLOV3}	—	0.0	ns	4
Local bus clock to LALE assertion	t _{LBKLOV4}	—	0.0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-3.3	—	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-3.3	_	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}	_	0.2	ns	7

Notes:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
- 3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
- 5. Input timings are measured at the pin.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).



Local Bus Controller (eLBC)



Figure 31. Local Bus Signals (PLL Bypass Mode)



Local Bus Controller (eLBC)



Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)



11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

Table 53. JTAG	AC Timina	Specifications	(Independent	t of SYSCLK)	1
	/ · · · · · · · · · · · · · · · · · · ·	opeenieanene	(

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	_	ns	—
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	6
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0		ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25		ns	4
Valid times: Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	30 30		ns	5



At recommended operating conditions with OV_{DD} of 3.3 V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 2).

Parameter	Symbol ¹	Min	Мах	Unit
Capacitive load for each bus line	Cb	—	400	pF

Notes:

NXP Semiconductors

- 1. The symbols used for timing specifications herein follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the t_{I2C} clock reference (K) going to the t_{I2C} clock reference (K) going to the t_{I2C} timing (I2) for the time that the data with respect to the t_{I2C} symbolizes I²C timing (I2) for the time that the data with respect to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the t_{I2C} clock reference (K) going to the t_{I2C} clock reference (K) going to the t_{I2C} timing (I2) for the time that the data with respect to the t_{I2C} clock reference (K) going to the t_{I2C} clock reference (K) going to the t_{I2C} timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.}
- 2. As a transmitter, the MPC8572E provides a delay time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8572E acts as the I2C bus master while transmitting, the MPC8572E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8572E would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8572E as transmitter, application note AN2919 referred to in note 4 below is recommended.
- 3. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*.

Figure 40 provides the AC test load for the I^2C .



Figure 40. I²C AC Test Load

Figure 41 shows the AC timing diagram for the I^2C bus.



Figure 41. I²C Bus AC Timing Diagram



6. Differential Waveform

- 1. The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the non-inverting signal (SDn_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
- 2. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.



Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and



High-Speed Serial Interfaces (HSSI)

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.



Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)





Table 63. Differential Receiver (RX)	Input	Specifications	(continued)
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Symbol	Parameter	Min	Nominal	Max	Units	Comments
L _{RX-SKEW}	Total Skew		_	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 57 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 56). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes see Figure 57). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.



Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)

Characteristic	Symbol	Ra	nge	Unit	Notes		
Characteristic	Gymbol	Min	Мах	Onic	notes		
Multiple Output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link		
Unit Interval	UI	400	400	ps	+/- 100 ppm		

Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notos	
Gharacteristic	Symbol	Min	Мах	Unit	NOLES	
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair	
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	—	
Deterministic Jitter	J _D	_	0.17	UI p-p	—	
Total Jitter	J _T	—	0.35	UI p-p	_	
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit Interval	UI	320	320	ps	+/– 100 ppm	

Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notes	
Unaracteristic	Gymbol	Min	Мах	Onic	Notes	
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair	
Differential Output Voltage	V _{DIFFPP}	800	1600	mV p-p	—	
Deterministic Jitter	J _D	—	0.17	UI p-p	—	
Total Jitter	J _T	—	0.35	UI p-p	—	
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit Interval	UI	800	800	ps	+/- 100 ppm	



Package Description

Table 76. MPC8572E Pinout Listing (continue	d)
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Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	0	GV _{DD}	_
D2_MWE	Write Enable	AA2	0	GV _{DD}	_
D2_MCAS	Column Address Strobe	AD1	0	GV _{DD}	_
D2_MRAS	Row Address Strobe	AA1	0	GV _{DD}	_
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	0	GV _{DD}	11
D2_MCS[0:3]	Chip Select	AB1, AG2, AC1, AH2	0	GV _{DD}	_
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	0	GV _{DD}	—
D2_MCK[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	0	GV _{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	0	GV _{DD}	_
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV _{DD}	25
	Local Bus Contro	ller Interface			
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV _{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV _{DD}	_
LA[27]	Burst Address	J21	0	BV _{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	0	BV _{DD}	5, 7, 9
LCS[0:4]	Chip Selects	B23, E16, D20, B25, A22	0	BV _{DD}	10
LCS[5]/DMA2_DREQ[1]	Chip Selects / DMA Request	D19	I/O	BV _{DD}	1, 10
LCS[6]/DMA2_DACK[1]	Chip Selects / DMA Ack	E19	0	BV _{DD}	1, 10
LCS[7]/DMA2_DDONE[1]	Chip Selects / DMA Done	C21	0	BV _{DD}	1, 10
LWE[0]/LBS[0]/LFWE	Write Enable / Byte Select	D17	0	BV _{DD}	5, 9
LWE[1]/LBS[1]	Write Enable / Byte Select	F15	0	BV _{DD}	5, 9
LWE[2]/LBS[2]	Write Enable / Byte Select	B24	0	BV _{DD}	5, 9
LWE[3]/LBS[3]	Write Enable / Byte Select	D18	0	BV _{DD}	5, 9
LALE	Address Latch Enable	F19	0	BV _{DD}	5, 8, 9
LBCTL	Buffer Control	L18	0	BV _{DD}	5, 8, 9



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS1	SerDes Transceiver Core Logic GND (xcorevss)	C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32	_	_	_
SGND_SRDS2	SerDes Transceiver Core Logic GND (xcorevss)	AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32	_	_	_
AGND_SRDS1	SerDes PLL GND	J31		—	
AGND_SRDS2	SerDes PLL GND	AH31	_	—	_
OVDD	General I/O Supply	U31, V24, V28, Y31, AA27, AB25, AB29	_	OVDD	_
LVDD	TSEC 1&2 I/O Supply	AC18, AC21, AG21, AL27	_	LVDD	_
TVDD	TSEC 3&4 I/O Supply	AC15, AE16, AH18		TVDD	
GVDD	SSTL_1.8 DDR Supply	B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2		GVDD	
BVDD	Local Bus and GPIO Supply	A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20	—	BVDD	—



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω (±1%) to GND	_
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω (±1%) to GND	_
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	0	AVDD_S RDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	Ι	$\begin{array}{c} 200\Omega \\ (\pm1\%) \text{ to} \\ \text{GND} \end{array}$	_
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	Ι	100Ω (±1%) to GND	_
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	0	AVDD_S RDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	_	internal diode	14
No Connection Pins					

Table 76. MPC8572E Pinout Listing (continued)



Clocking

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

	Maximum Processor Core Frequency									
Characteristic	1067 MHz		1200 MHz		1333 MHz		1500 MHz		Unit	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Table 77. MPC8572E Processor Core Clocking Specifications

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.

2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.



Clocking

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio	
000	4:1	
001	5:1	
010	6:1	
011	8:1	
100	10:1	
101	12:1	
110	Reserved	
111	Reserved	

Table 79. CCB Clock Ratio

19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

Table 80 describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/LOE/LFRE at power up, as shown in Table 80.

Binary Value of LBCT <u>L, LALE,</u> LGPL2/LOE/LFRE Signals	e500 Core0:CCB Clock Ratio	Binary Value of LBCT <u>L, LALE,</u> LGPL2/LOE/LFRE Signals	e500 Core0:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

Table 80. e500 Core0 to CCB Clock Ratio



in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

 $\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$

See Section 20.4, "1x/4x LP-Serial Signal Descriptions," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, $1023 \ 33 \times 33 \ FC-PBGA$.

The package uses a 29.6×29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer (1s)	R_{\ThetaJA}	15	°C/W	1, 2
Junction to ambient, natural convection	Four-layer (2s2p)	R_{\ThetaJA}	11	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer (1s)	$R_{\Theta JMA}$	11	°C/W	1, 3
Junction to ambient (ar 200 ft./min.)	Four-layer (2s2p)	R _{ØJMA} 8		°C/W	1, 3
Junction to board	—	$R_{\Theta J B}$	4	°C/W	4
Junction to case	_	R_{\ThetaJC}	0.5	°C/W	5

Table 84. Package Thermal Characteristics

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance

- 2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
- 3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461TM). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:

MPC8572E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 7

NXP Semiconductors



22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 22.1, "Part Numbers Fully Addressed by this Document."

22.1 Part Numbers Fully Addressed by this Document

Table 86 through Table 88 provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

MPC	nnnn	е	t	1	рр	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/ DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included Blank = 0 C C = -40 to Blank = Not included	Blank = 0 to 105°C Blank = C = -40 to 105°C Standa L = Lov	Blank = Standard L = Low	ank = PX = andard = Low FC-PBGA VT = Pb-free, FC-PBGA ⁴ VJ = Fully Pb-free FC-PBGA ⁵	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included
							E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included

Notes:

- ¹ MPC stands for "Qualified."
- PPC stands for "Prototype"
- ² See Section 18, "Package Description," for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 4. The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.
- 5. The VJ part number is entirely lead-free. This includes the C4 die bumps.