# E·XFL



#### Welcome to E-XFL.COM

#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572epxavne

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
  - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1<sup>TM</sup> virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision



- Three PCI Express controllers
  - PCI Express 1.0a compatible
  - Supports x8, x4, x2, and x1 link widths (see following bullet for specific width configuration options)
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Full 64-bit decode with 36-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
  - Single x8/x4/x2/x1 PCI Express
  - Dual x4/x2/x1 PCI Express
  - Single x4/x2/x1 PCI Express and dual x2/x1 PCI Express
  - Single 1x/4x Serial RapidIO and single x4/x2/x1 PCI Express
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, that automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the eight counters
  - Supports duration and quantity threshold counting
  - Permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1<sup>™</sup> compatible, JTAG boundary scan
- 1023 FC-PBGA package



Electrical Characteristics

### 2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

	Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage		V <sub>DD</sub>	1.1 V ± 55 mV	V	—
PLL supply voltage		AV <sub>DD</sub>	1.1 V ± 55 mV	V	1
Core power supply for	or SerDes transceivers	SV <sub>DD</sub>	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceivers			1.1 V ± 55 mV	V	—
DDR SDRAM	DDR2 SDRAM Interface	GV <sub>DD</sub>	1.8 V ± 90 mV	V	—
Supply voltage	DDR3 SDRAM Interface	1.5 V ±			_
Three-speed Etherne	et I/O voltage	LV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV		4
DUART, system cont	trol and power management, $I^2C$ , and JTAG I/O voltage	OV <sub>DD</sub>	3.3 V ± 165 mV	V	3
Local bus and GPIO	I/O voltage	BV <sub>DD</sub>	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV <sub>IN</sub>	GND to GV <sub>DD</sub>	V	2
	DDR2 and DDR3 SDRAM Interface reference	MV <sub>REF</sub> n	GV <sub>DD</sub> /2 ± 1%	V	—
Local bus and GPIO I/O voltage Input voltage DDR2 and DDR3 SDRAM Interface signals DDR2 and DDR3 SDRAM Interface reference Three-speed Ethernet signals		LV <sub>IN</sub> TV <sub>IN</sub>	GND to LV <sub>DD</sub> GND to TV <sub>DD</sub>	V	4
	Local bus and GPIO signals	BV <sub>IN</sub>	GND to BV <sub>DD</sub>	V	—
	Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, I <sup>2</sup> C, and JTAG signals	OV <sub>IN</sub>	GND to OV <sub>DD</sub>	V	3
Junction temperature	e range	TJ	0 to 105	°C	_

### **Table 2. Recommended Operating Conditions**

### Notes:

- 1. This voltage is the input to the filter discussed in Section 21.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AV<sub>DD</sub> pin, that may be reduced from V<sub>DD</sub> by the filter.
- 2. Caution: MV<sub>IN</sub> must not exceed GV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. **Caution:** OV<sub>IN</sub> must not exceed OV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV<sub>IN</sub> must not exceed L/TV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8572E.



### Figure 2. Overshoot/Undershoot Voltage for TV<sub>DD</sub>/BV<sub>DD</sub>/GV<sub>DD</sub>/LV<sub>DD</sub>/OV<sub>DD</sub>

The core voltage must always be provided at nominal 1.1 V. (See Table 2 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage.  $TV_{DD}$ ,  $BV_{DD}$ ,  $OV_{DD}$ , and  $LV_{DD}$  based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied  $MV_{REF}n$  signal (nominally set to  $GV_{DD}/2$ ) as is appropriate for the SSTL\_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.



## 4 Input Clocks

## 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

### Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with  $OV_{DD}$  of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f <sub>SYSCLK</sub>	33	—	133	MHz	1
SYSCLK cycle time	t <sub>SYSCLK</sub>	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t <sub>KHK</sub> /tsysclk	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

- 2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{CCB}$ , and minimum clock low time is  $2 \times t_{CCB}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.



**RESET** Initialization

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with  $OV_{DD}$  of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	_			+/- 150	ps	4, 5, 6

Notes:

- 1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
- 2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

## 4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

## 4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

## 5 **RESET** Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

### **Table 9. RESET Initialization Timing Specifications**

Parameter/Condition	Min	Мах	Unit	Notes
Required assertion time of HRESET	100	—	μs	2
Minimum assertion time for SRESET	3	—	SYSCLKs	1



described in Section 21.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC\_GTX\_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2\_REF\_CLK and SD2\_REF\_CLK pins.

## 8.3.1 DC Requirements for SGMII SD2\_REF\_CLK and SD2\_REF\_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

## 8.3.2 AC Requirements for SGMII SD2\_REF\_CLK and SD2\_REF\_CLK

Table 37 lists the SGMII SerDes reference clock AC requirements. Note that SD2\_REF\_CLK and SD2\_REF\_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t <sub>REF</sub>	REFCLK cycle time		10 (8)	_	ns	1
t <sub>REFCJ</sub>	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles		—	100	ps	_
t <sub>REFPJ</sub>	Phase jitter. Deviation in edge location with respect to mean edge location	-50		50	ps	

### Table 37. SD2\_REF\_CLK and SD2\_REF\_CLK AC Requirements

Note:

1.8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected through cfg\_srds\_sgmii\_refclk during POR.



#### **Ethernet Management Interface Electrical Characteristics**

### Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with  $LV_{DD}/TV_{DD}$  of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit	Notes
ECn_MDIO to ECn_MDC setup time	t <sub>MDDVKH</sub>	5	—	-	ns	_
ECn_MDIO to ECn_MDC hold time	t <sub>MDDXKH</sub>	0	—	-	ns	_
ECn_MDC rise time	t <sub>MDCR</sub>	-	—	10	ns	4
ECn_MDC fall time	t <sub>MDHF</sub>	—	—	10	ns	4

### Notes:

1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state)

(reference)(state) for inputs and  $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MDKHDX}$  symbolizes management data timing (MD) for the time  $t_{MDC}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{MDDVKH}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MDC}$  clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency ( $f_{CCB}$ ). The actual ECn\_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2\*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz,  $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3$  MHz. That is, for a system running at a particular platform frequency ( $f_{CCB}$ ), the ECn\_MDC output clock frequency can be programmed between maximum  $f_{MDC} = f_{CCB}/64$  and minimum  $f_{MDC} = f_{CCB}/448$ . Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
- 3. The maximum ECn\_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn\_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn\_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
- 4. Guaranteed by design.
- 5. t<sub>plb clk</sub> is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.



Figure 28. MII Management Interface Timing Diagram

## NP

#### Local Bus Controller (eLBC)

Table 50. Local Bus General Timing Parameters ( $BV_{DD} = 2.5 V DC$ )—PLL Enabled (continued)At recommended operating conditions with  $BV_{DD}$  of 2.5 V ± 5% (continued)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.4	ns	_
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.5	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.4	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>	—	2.6	ns	5

Note:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t<sub>(First two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one(1). Also, t<sub>LBKHOX</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 2.5-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at  $BV_{DD} = 1.8 \text{ V DC}$ 

Table 51. Local Bus General Timing Parameters ( $BV_{DD} = 1.8 V DC$ )—PLL Enabled At recommended operating conditions with  $BV_{DD}$  of 1.8 V ± 5%

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	6.67	12	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	2.4	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.9	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.1	—	ns	3, 4



Table 51. Local Bus General Timing Parameters (BV<sub>DD</sub> = 1.8 V DC)—PLL Enabled (continued)

At recommended operating conditions with  $\mathsf{BV}_{\mathsf{DD}}$  of 1.8 V ± 5% (continued)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.1	_	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t <sub>LBOTOT</sub>	1.2	_	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	_	3.2	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	_	3.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	_	3.2	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	_	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.9	_	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.9		ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.6	ns	5

Note:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t<sub>(First two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one(1). Also, t<sub>LBKHOX</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from BV<sub>DD</sub>/2 of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 1.8-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.



Figure 29. Local Bus AC Test Load



### Local Bus Controller (eLBC)

Figure 30 through Figure 35 show the local bus signals.



Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

Table 52 describes the general timing parameters of the local bus interface at  $BV_{DD} = 3.3 \text{ V DC}$  with PLL disabled.

### Table 52. Local Bus General Timing Parameters—PLL Bypassed

At recommended operating conditions with  $BV_{DD}$  of 3.3 V ± 5%

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	12		ns	2
Local bus duty cycle	t <sub>LBKH</sub> /t <sub>LBK</sub>	43	57	%	—
Internal launch/capture clock to LCLK delay	t <sub>LBKHKT</sub>	2.3	4.0	ns	
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	5.8	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKL2</sub>	5.7	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	-1.3	_	ns	4, 5



Local Bus Controller (eLBC)



Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)





Figure 39 provides the boundary-scan timing diagram.



Figure 39. Boundary-Scan Timing Diagram

## 13 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the I<sup>2</sup>C interfaces of the MPC8572E.

## **13.1** I<sup>2</sup>C DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the I<sup>2</sup>C interfaces.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V <sub>IH</sub>	$0.7 \times OV_{DD}$	OV <sub>DD</sub> + 0.3	V	—
Input low voltage level	V <sub>IL</sub>	-0.3	$0.3  imes OV_{DD}$	V	—
Low level output voltage	V <sub>OL</sub>	0	0.4	V	1
Pulse width of spikes which must be suppressed by the input filter	t <sub>I2KHKL</sub>	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1\times OV_{DD}$ and $0.9\times OV_{DD}(max)$	lı	-10	10	μA	3



High-Speed Serial Interfaces (HSSI)

SD1\_REF\_CLK for PCI Express and Serial RapidIO, or SD2\_REF\_CLK and SD2\_REF\_CLK for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

## **15.2.1 SerDes Reference Clock Receiver Characteristics**

Figure 44 shows a receiver reference diagram of the SerDes reference clocks. Characteristics are as follows:

- The supply voltage requirements for  $XV_{DD SRDS2}$  are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SDn\_REF\_CLK and SDn\_REF\_CLK are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SDn\_REF\_CLK or SDn\_REF\_CLK) has on-chip 50-Ω termination to SGND\_SRDSn (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND\_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*\_REF\_CLK and  $\overline{\text{SD}n_\text{REF}\text{-}\text{CLK}}$  inputs cannot drive 50  $\Omega$  to SGND\_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.



Serial RapidIO

# 17.1 <u>DC Requirements</u> for Serial RapidIO SD1\_REF\_CLK and SD1\_REF\_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

# 17.2 <u>AC Requirements</u> for Serial RapidIO SD1\_REF\_CLK and SD1\_REF\_CLK

Figure 64lists the AC requirements.

Table 64. SD <i>n</i> _	_REF_CL	K and SD <i>n</i> _	_REF_(	CLK AC	Requirements

Symbol	Parameter Description	Min	Typical	Мах	Units	Comments
t <sub>REF</sub>	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t <sub>REFCJ</sub>	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	_	—	80	ps	_
t <sub>REFPJ</sub>	Phase jitter. Deviation in edge location with respect to mean edge location	-40	-	40	ps	_

## 17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.



link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than  $10^{-12}$ . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be  $100 \Omega$  resistive +/- 5% differential to 2.5 GHz.

### 17.8.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

### 17.8.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100  $\Omega$  resistive +/- 5% differential to 2.5 GHz.

### 17.8.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 17.6, "Receiver Specifications," and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 60 and Table 75. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 17.6, "Receiver Specifications," is then added to the signal and the test load is replaced by the receiver being tested.

## **18 Package Description**

This section describes package parameters, pin assignments, and dimensions.



**Package Description** 

- 5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 6. Parallelism measurement shall exclude any effect of mark on top surface of package.

## 18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

### Table 76. MPC8572E Pinout Listing

Signal	Signal Name	Pin Type	Power Supply	Notes						
DDR SDRAM Memory Interface 1										
D1_MDQ[0:63]	Data	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17	I/O	GV <sub>DD</sub>						
D1_MECC[0:7]	Error Correcting Code	M10, M7, R8, T11, L12, L11, P9, R10	I/O	GV <sub>DD</sub>	—					
D1_MAPAR_ERR	Address Parity Error	P6	I	GV <sub>DD</sub>	_					
D1_MAPAR_OUT	Address Parity Out	W6	0	$GV_DD$	_					
D1_MDM[0:8]	Data Mask	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11	0	GV <sub>DD</sub>	_					
D1_MDQS[0:8]	Data Strobe	A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9	I/O	GV <sub>DD</sub>	_					
D1_MDQS[0:8]	Data Strobe	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	GV <sub>DD</sub>	_					
D1_MA[0:15]	Address	Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7	0	GV <sub>DD</sub>						
D1_MBA[0:2]	Bank Select	AA7, AA8, R7	0	$GV_DD$						
D1_MWE	Write Enable	AC12	0	$\text{GV}_{\text{DD}}$	_					



Clocking

## 19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

	Maximum Processor Core Frequency									
Characteristic	1067 MHz		1200 MHz		1333 MHz		1500 MHz		Unit	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

### Table 77. MPC8572E Processor Core Clocking Specifications

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.

2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.



### System Design Information

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

### 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.



System Design Information



Figure 65. COP Connector Physical Pinout