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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572evjatle

  - Regular expression (regex) pattern matching
    - Built-in case insensitivity, wildcard support, no pattern explosion
    - Cross-packet pattern detection
    - Fast pattern database compilation and fast incremental updates
    - 16000 patterns, each up to 128 bytes in length
    - Patterns can be split into 256 sets, each of which can contain 16 subsets
  - Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
    - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
    - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
    - 8192 stateful rules
  - Deflate engine
    - Supports decompression of DEFLATE compression format including zlib and gzip
    - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)
- Two Table Lookup Units (TLU)
  - Hardware-based lookup engine offloads table searches from e500 cores
  - Longest prefix match, exact match, chained hash, and flat data table formats
  - Up to 32 tables, with each table up to 16M entries
  - 32-, 64-, 96-, or 128-bit keys
- Two I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Enhanced local bus controller (eLBC)

Figure 1 shows the MPC8572E block diagram.

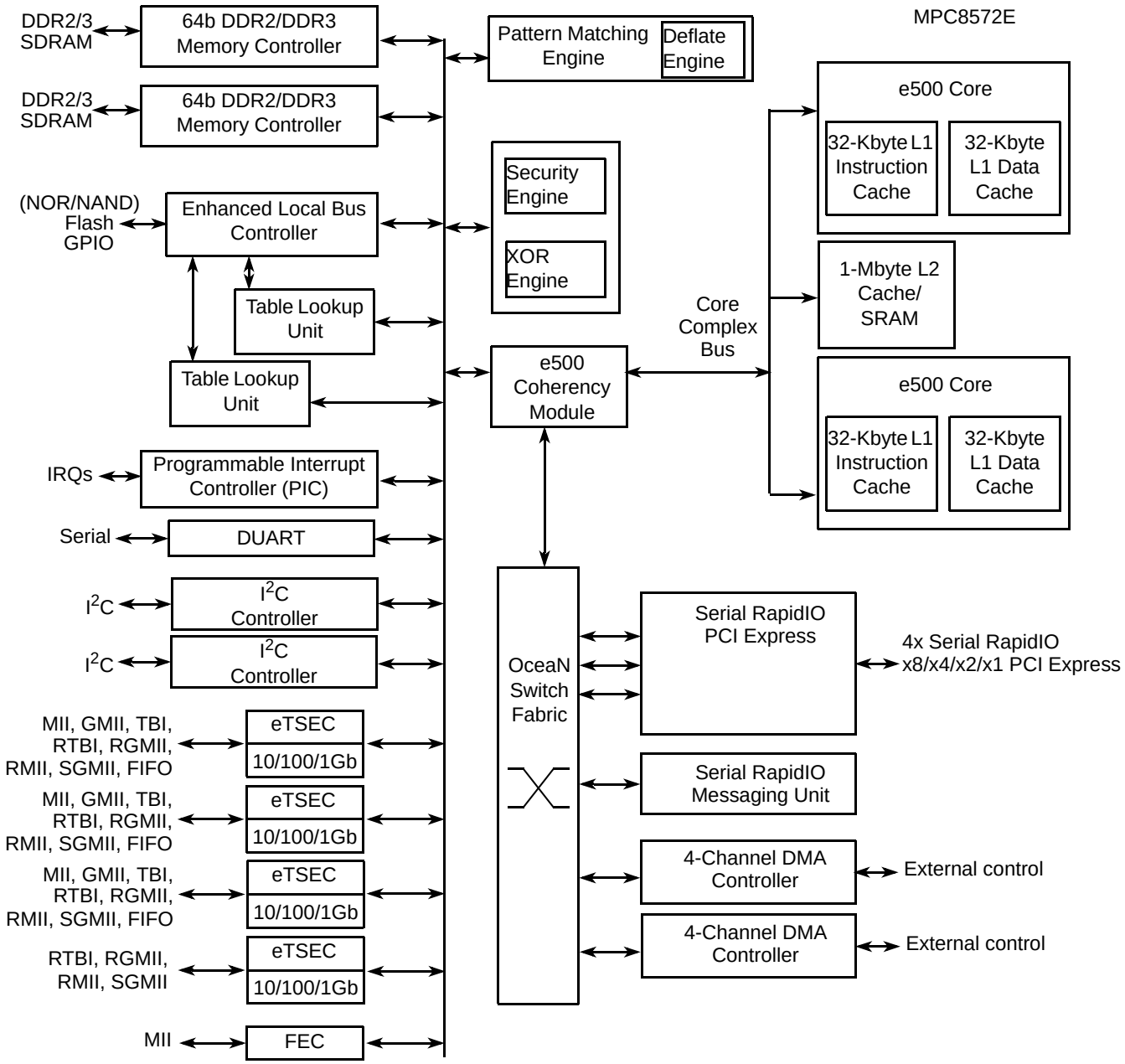

Figure 1. MPC8572E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

Table 4. MPC8572E Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

Table 5. MPC8572EL Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

Table 14 provides the current draw characteristics for $MV_{REF}n$.

Table 14. Current Draw Characteristics for MV_{REF} *n*

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	$I_{MVREF}n$	—	1500	µA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	>=667 MHz	V_{ILAC}	—	$MV_{REF}n$ – 0.20	V	—
	<= 533 MHz		—	$MV_{REF}n$ – 0.25		
AC input high voltage	>=667 MHz	V_{IHAC}	$MV_{REF}n$ + 0.20	—	V	—
—	<= 533 MHz		$MV_{REF}n$ + 0.25	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REF}n$ – 0.175	V	—
AC input high voltage	V_{IHAC}	$MV_{REF}n$ + 0.175	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6
800 MHz		$-0.5 \times t_{MCK} - 0.375$	$-0.5 \times t_{MCK} + 0.375$		
<= 667 MHz		$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$		
MDQS epilogue end	t_{DDKHME}			ns	6
800 MHz		–0.375	0.375		
<= 667 MHz	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR2 and DDR3 SDRAM Interface output timing for the MCK to MDQS skew measurement (tDDKHMH).

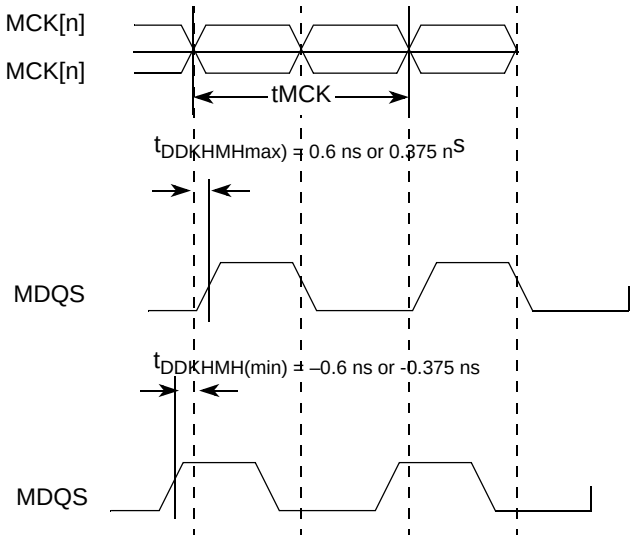

Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR2 and DDR3 SDRAM Interface output timing diagram.

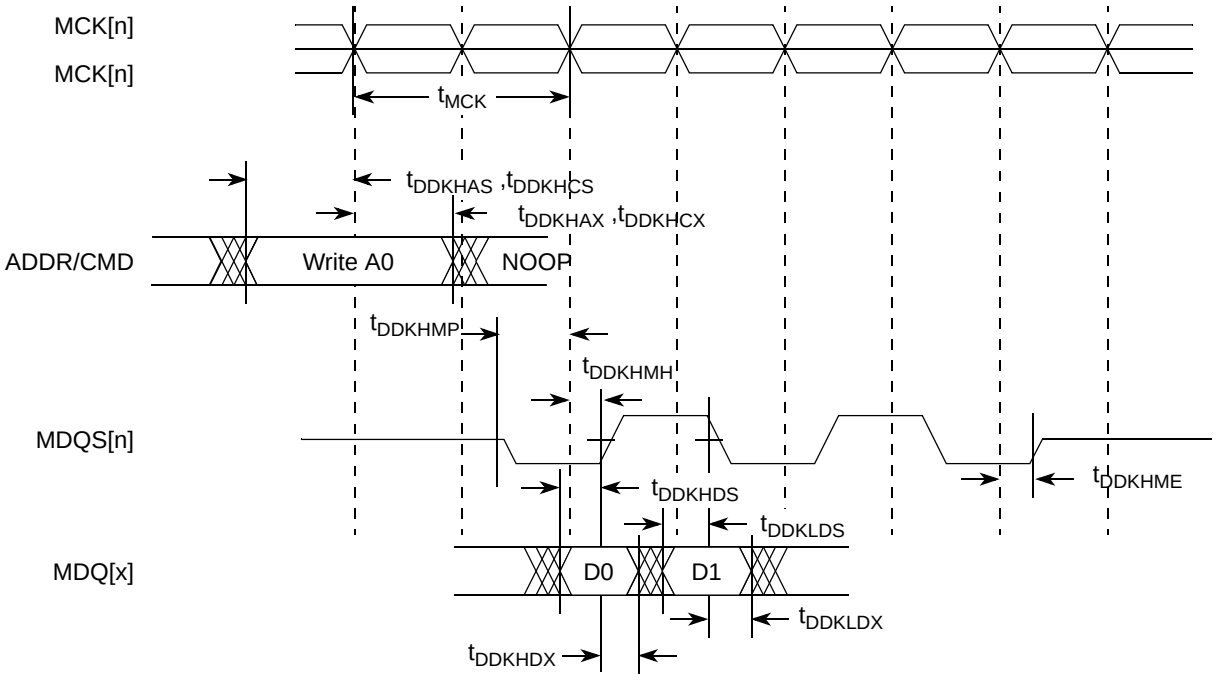

Figure 5. DDR2 and DDR3 SDRAM Interface Output Timing Diagram

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)

Parameters	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4 or FEC.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

Table 25. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period[1]	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%

described in Section 21.5, “Connection Recommendations,” as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ pins.

8.3.1 DC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, “High-Speed Serial Interfaces (HSSI).”

8.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

Table 37 lists the SGMII SerDes reference clock AC requirements. Note that SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 37. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Note:
1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected through cfg_srds_sgmii_refclk during POR.

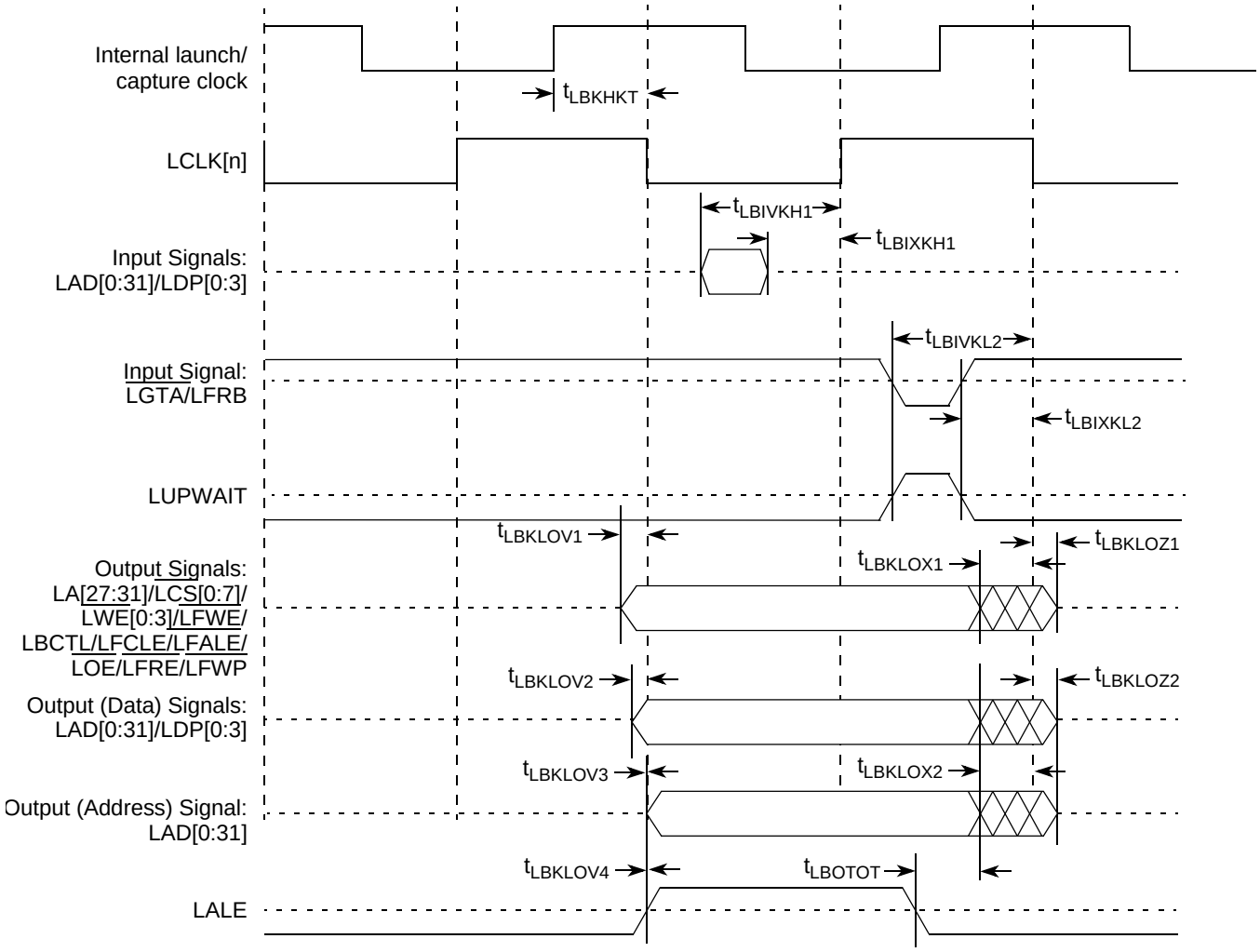

Figure 31. Local Bus Signals (PLL Bypass Mode)

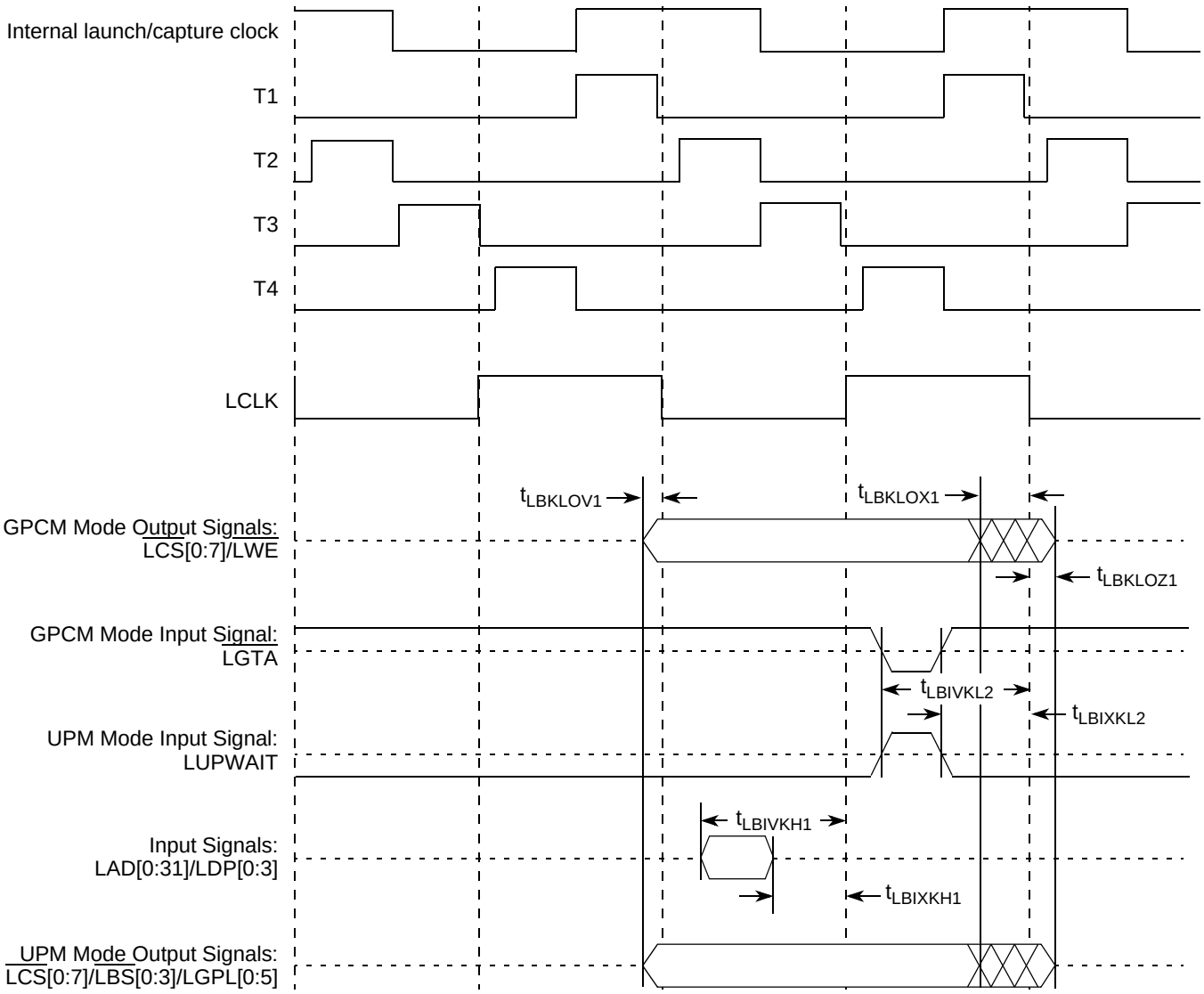

Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.

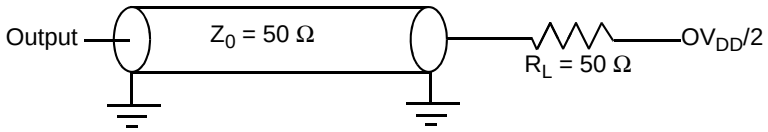

Figure 36. AC Test Load for the JTAG Interface

Figure 37 provides the JTAG clock input timing diagram.

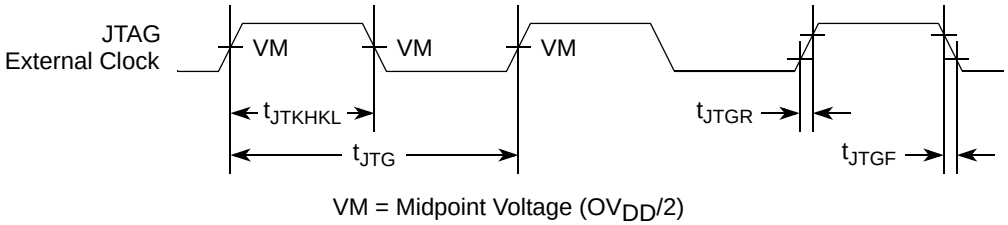

Figure 37. JTAG Clock Input Timing Diagram

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.

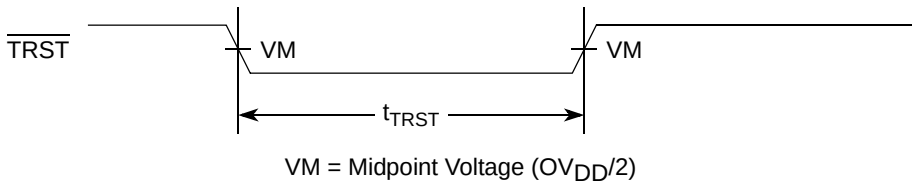

Figure 38. $\overline{\text{TRST}}$ Timing Diagram

Figure 39 provides the boundary-scan timing diagram.

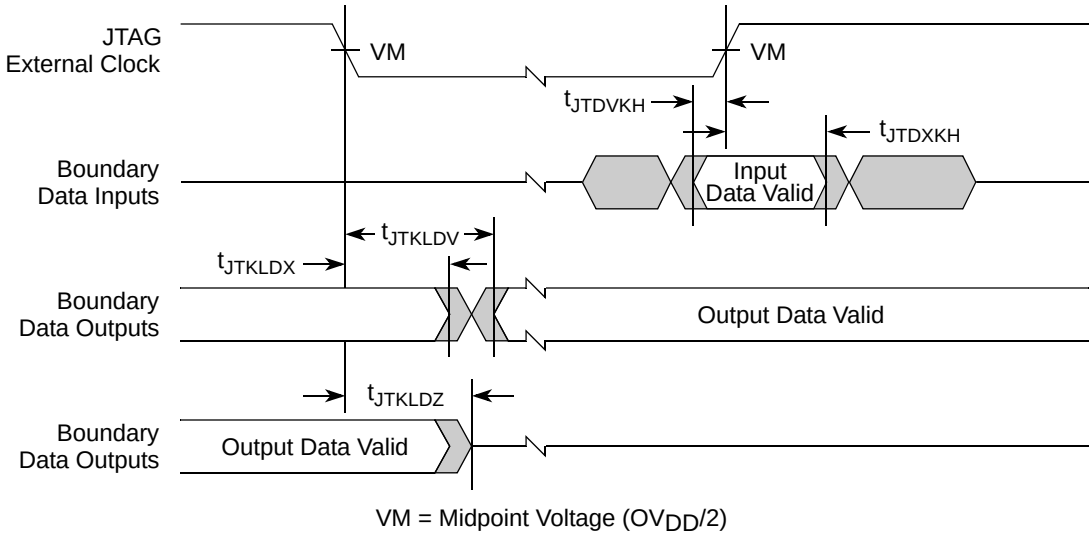

Figure 39. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8572E.

13.1 I²C DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the I²C interfaces.

Table 54. I²C DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3

is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

Table 60 describes some AC parameters common to SGMII, PCI Express and Serial RapidIO protocols.

Table 60. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200		mV	2
Differential Input Low Voltage	V_{IL}	—	-200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate (SDn_REF_CLK) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 52.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 53.

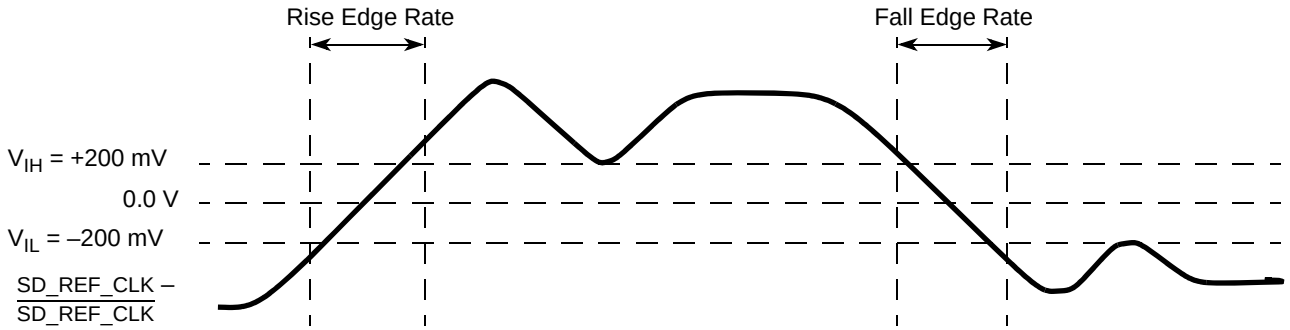

Figure 52. Differential Measurement Points for Rise and Fall Time

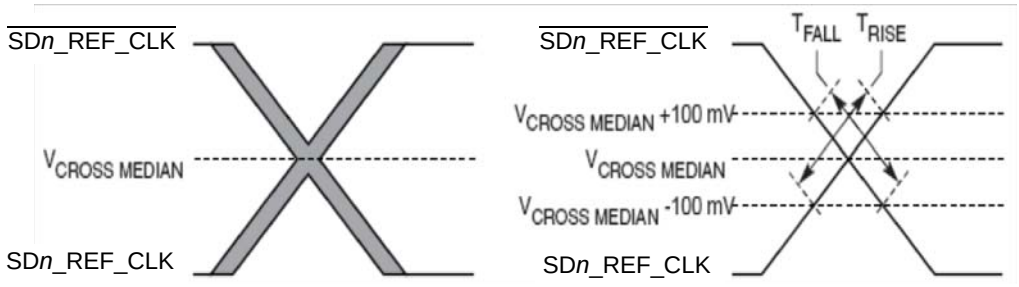

Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$"
- Section 16.2, "AC Requirements for PCI Express SerDes Reference Clocks"
- Section 17.2, "AC Requirements for Serial RapidIO SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$"

15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ are designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane's transmitter and receiver.

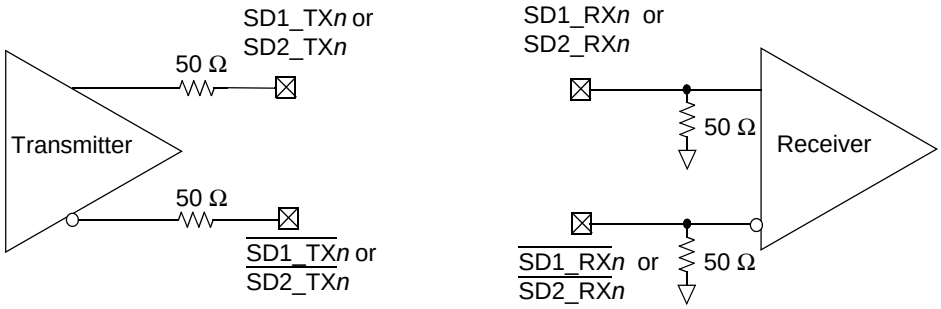

Figure 54. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 16, "PCI Express"

- Section 17, “Serial RapidIO”

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

16.2 AC Requirements for PCI Express SerDes Reference Clocks

Table 61 lists AC requirements.

Table 61. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:
1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

16.4.1 Differential Transmitter (TX) Output

Table 62 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 72. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 73. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	O	BV_{DD}	5, 9
LGPL1/$\overline{\text{LFALE}}$	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	O	BV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O	BV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose Line 3 / Flash Write Protect	K16	O	BV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV_{DD}	—
LGPL5	UPM General Purpose Line 5 / Amux	B26	O	BV_{DD}	5, 9
LCLK[0:2]	Local Bus Clock	F17, F16, A23	O	BV_{DD}	—
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV_{DD}	—
LSYNC_OUT	Local Bus DLL Synchronization	A21	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DACK}}$[0:1]	DMA Acknowledge	W25, U30	O	OV_{DD}	21
$\overline{\text{DMA2\_DACK}}$[0]	DMA Acknowledge	AA26	O	OV_{DD}	5, 9
$\overline{\text{DMA1\_DREQ}}$[0:1]	DMA Request	Y29, V27	I	OV_{DD}	—
$\overline{\text{DMA2\_DREQ}}$[0]	DMA Request	V29	I	OV_{DD}	—
$\overline{\text{DMA1\_DDONE}}$[0:1]	DMA Done	Y28, V30	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DDONE}}$[0]	DMA Done	AA28	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DREQ}}$[2]	DMA Request	M23	I	BV_{DD}	—
Programmable Interrupt Controller					
$\overline{\text{UDE0}}$	Unconditional Debug Event Processor 0	AC25	I	OV_{DD}	—
$\overline{\text{UDE1}}$	Unconditional Debug Event Processor 1	AA25	I	OV_{DD}	—
$\overline{\text{MCP0}}$	Machine Check Processor 0	M28	I	OV_{DD}	—
$\overline{\text{MCP1}}$	Machine Check Processor 1	L28	I	OV_{DD}	—
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV_{DD}	—

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

Figure 66. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

21.10.1 SerDes 1 Interface Entirely Unused

If the high-speed SerDes 1 interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX}}$[7:0]
- Reserved pins C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1:

- SD1_RX[7:0]
- $\overline{\text{SD1\_RX}}$[7:0]
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

Pins K32 and C29 must be tied to XV_{DD}_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.

The POR configuration pin cfg_srds1_en on TSEC2_TXD[5] can be used to power down SerDes 1 block for power saving. Note that both SVDD_SRDS1 and XVDD_SRDS1 must remain powered.

21.10.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes 1 interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX}}$[7:0]
- Reserved pins: C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1 if not used:

- SD1_RX[7:0]
- $\overline{\text{SD1\_RX}}$[7:0]

Pins K32 and C29 must be tied to XV_{DD}_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.

Table 87. Part Numbering Nomenclature—Rev 2.1

MPC	*nnnn*	*e*	*t*	*l*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = –40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 150- MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included
		Blank = Not included					D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 88. Part Numbering Nomenclature—Rev 1.1.1

MPC	*nnnn*	*e*	*t*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank=0 to 105°C C= –40 to 105°C	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz process or; 667 MT/s DDR datarate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included
		Blank = Not included				B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.