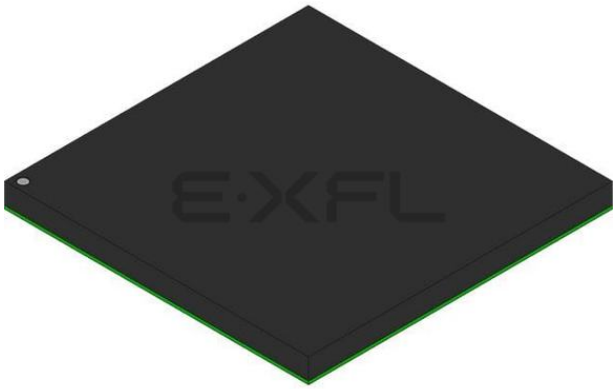

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572evtatld

- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing.
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
- Interrupt summary registers allow fast identification of interrupt source.

- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, SSL/TLS, SRTP, 802.16e, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 4096 bits
    - Elliptic curve cryptography with F_2m and F(p) modes and programmable field size up to 1023 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB, CBC and OFB-64 modes for both DES and 3DES
  - AESU—Advanced Encryption Standard unit
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, CTR, CCM, GCM, CMAC, OFB-128, CFB-128, and LRW modes
    - 128-, 192-, and 256-bit key lengths
  - AFEU—ARC four execution unit
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - MDEU—message digest execution unit
    - SHA-1 with 160-bit message digest
    - SHA-2 (SHA-256, SHA-384, SHA-512)
    - MD5 with 128-bit message digest
    - HMAC with all algorithms
  - KEU—Kasumi execution unit
    - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
    - Also supports A5/3 and GEA-3 algorithms
  - RNG—random number generator
  - XOR engine for parity checking in RAID storage applications
  - CRC execution unit
    - CRC-32 and CRC-32C
- Pattern Matching Engine with DEFLATE decompression

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- 10/100 Fast Ethernet controller (FEC) management interface
  - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
  - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
  - Four DMA channels per controller
  - All channels accessible by the local masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
  - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins ($\overline{\text{DMA2\_DREQ}}$[2]) is made available

Table 14 provides the current draw characteristics for $MV_{REF}n$.

Table 14. Current Draw Characteristics for MV_{REF} *n*

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	$I_{MVREF}n$	—	1500	µA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	>=667 MHz	V_{ILAC}	—	$MV_{REF}n$ – 0.20	V	—
	<= 533 MHz		—	$MV_{REF}n$ – 0.25		
AC input high voltage	>=667 MHz	V_{IHAC}	$MV_{REF}n$ + 0.20	—	V	—
—	<= 533 MHz		$MV_{REF}n$ + 0.25	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REF}n$ – 0.175	V	—
AC input high voltage	V_{IHAC}	$MV_{REF}n$ + 0.175	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t_{DDKHCS}	1.95	—	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
<= 667 MHz		–0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		375	—		
667 MHz		450	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	—		

Figure 15 shows the TBI transmit AC timing diagram.

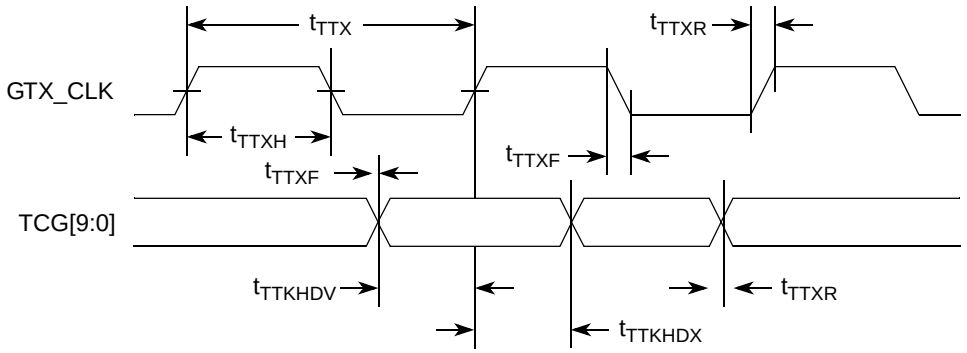

Figure 15. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition [3]	Symbol [1]	Min	Typ	Max	Unit
Clock period for TBI Receive Clock 0, 1	t_{TRX}	—	16.0	—	ns
Skew for TBI Receive Clock 0, 1	t_{SKTRX}	7.5	—	8.5	ns
Duty cycle for TBI Receive Clock 0, 1	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1	t_{TRDXKH}	1.5	—	—	ns
Clock rise time (20%-80%) for TBI Receive Clock 0, 1	t_{TRXR} [2]	0.7	—	2.4	ns
Clock fall time (80%-20%) for TBI Receive Clock 0, 1	t_{TRXF} [2]	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Notes:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

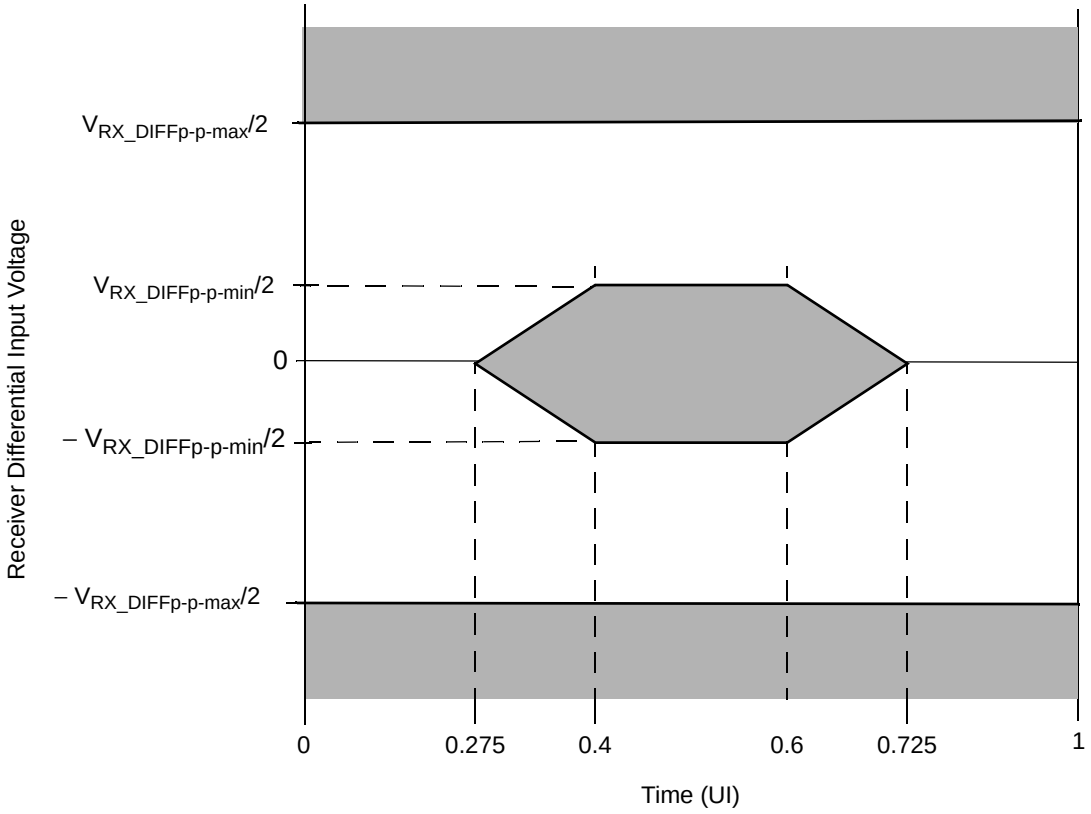

Figure 24. SGMII Receiver Input Compliance Mask

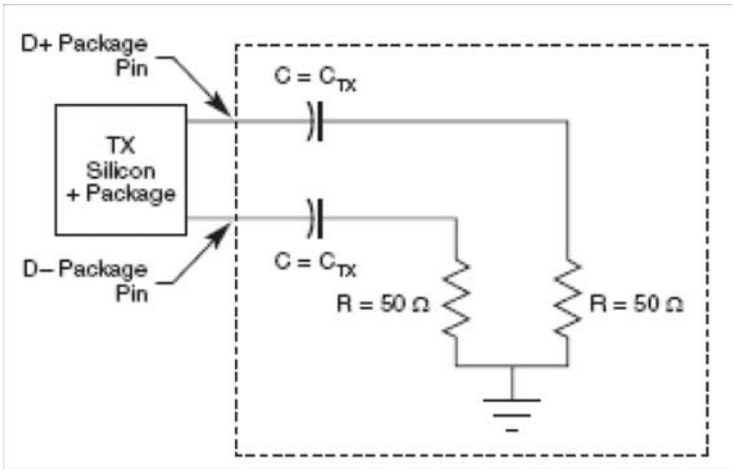

Figure 25. SGMII AC Test/Measurement Load

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=3.3 V) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV_{DD}/TV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	µA	—

Note:
1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbol referenced in Table 1.

Table 44. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=2.5 V)

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:

1 EC1_MDC and EC1_MDIO operate on LV_{DD}.
2 EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

9.2 MII Management AC Electrical Specifications

Table 45 provides the MII management AC timing specifications.There are three sets of Ethernet management signals (EC1_MDC and EC1_MDIO, EC3_MDC and EC3_MDIO, EC5_MDC and EC5_MDIO). These are not explicitly shown in the table or in the figure following.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
ECn_MDC frequency	f_{MDC}	0.9	2.5	9.3	MHz	2, 3
ECn_MDC period	t_{MDC}	107.5	—	1120	ns	—
ECn_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
ECn_MDC to ECn_MDIO delay	t_{MDKHDX}	10	—	$16*t_{plb\_clk}$	ns	5

Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-1.3	—	ns	4, 5
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	–0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	–0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0.0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.3	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.3	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

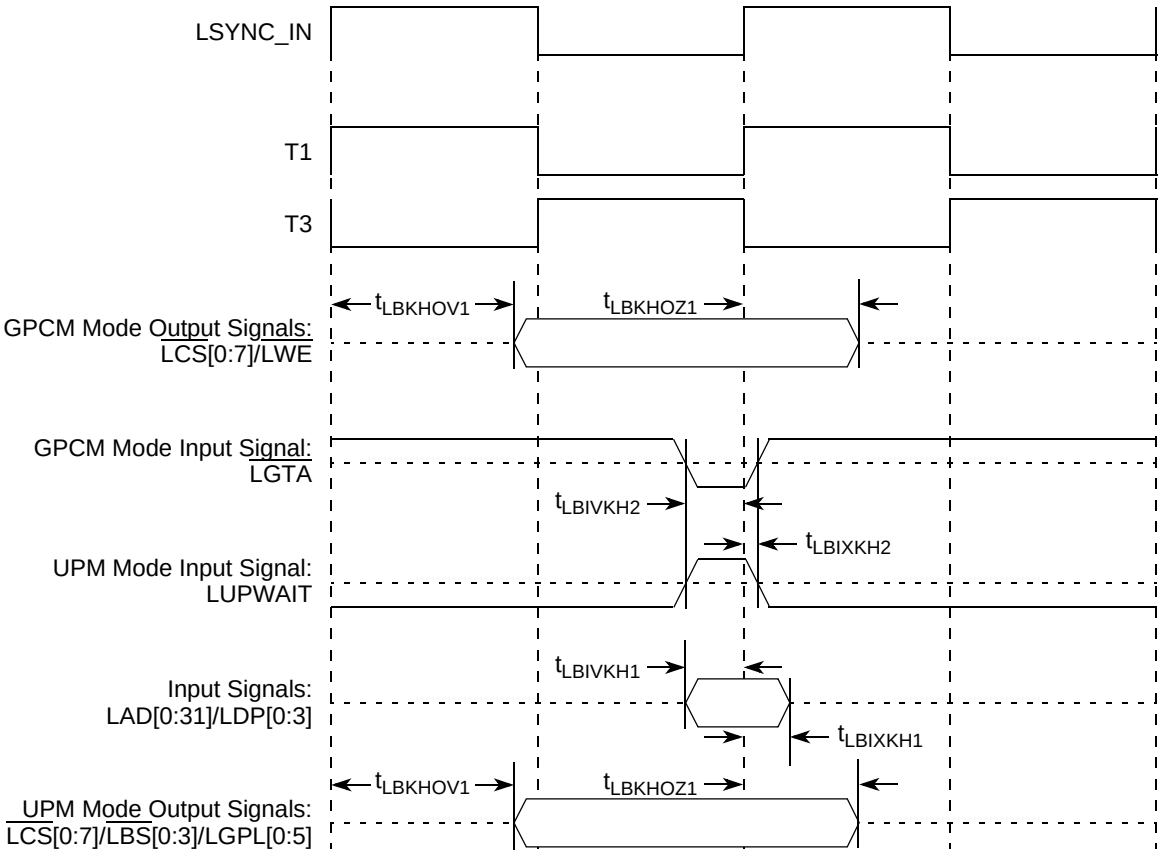

Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

6. Differential Waveform

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = $(V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2$ = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

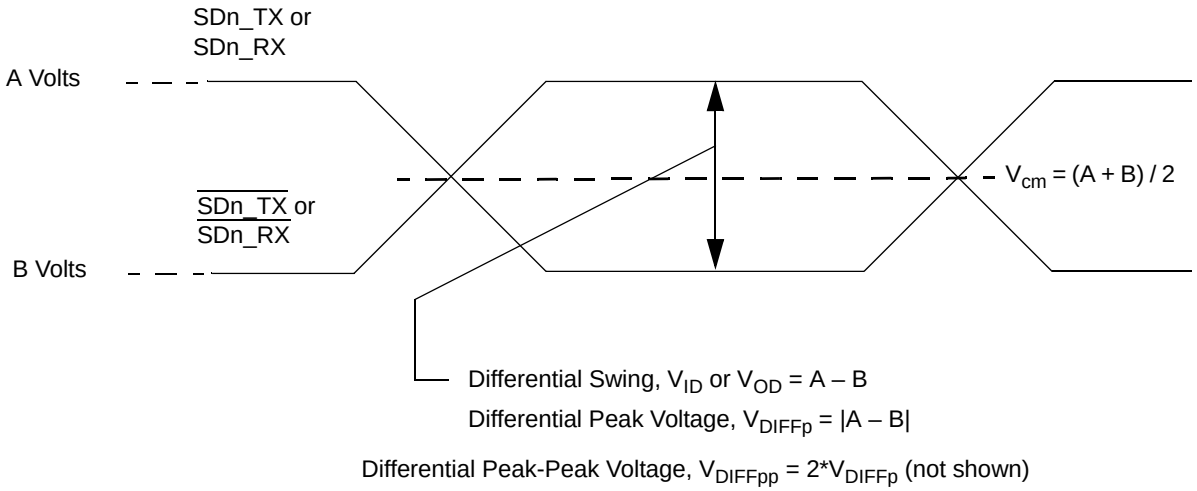

Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

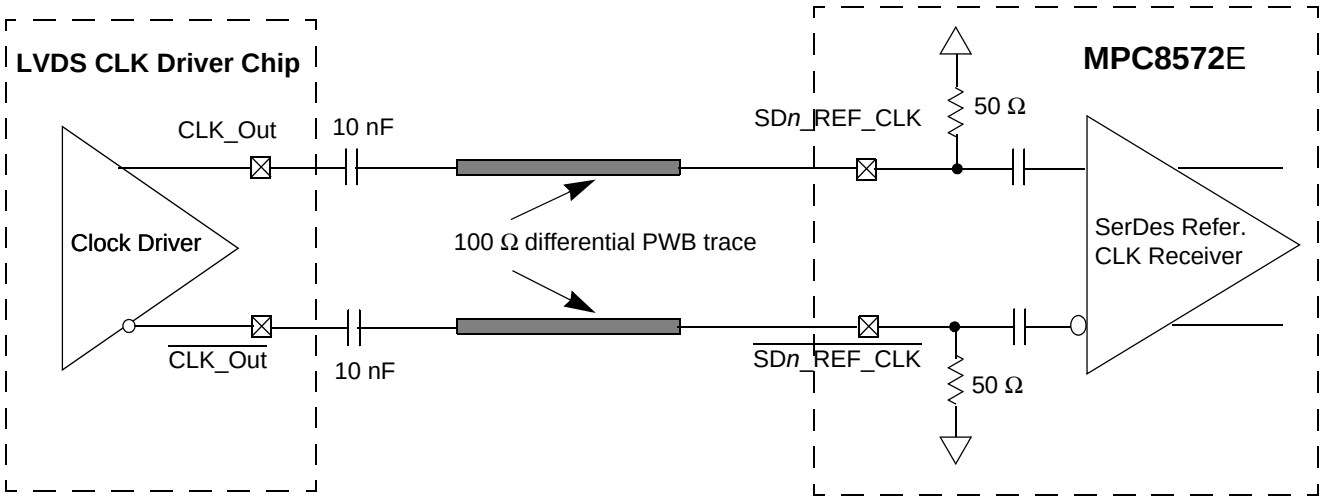

Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Consult

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 57) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 56) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

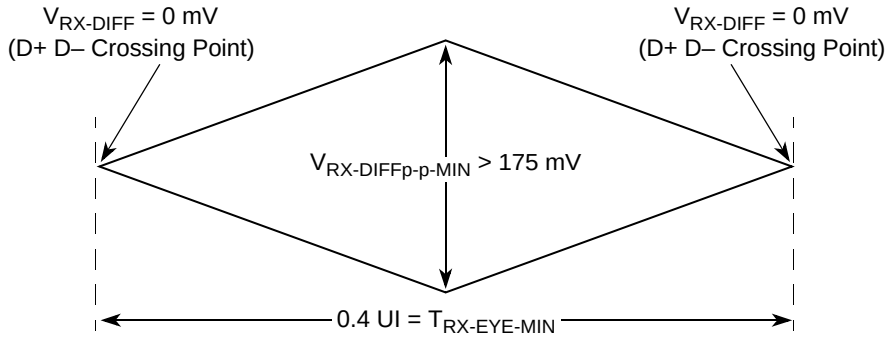

Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification

Table 74. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.

18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

Table 76. MPC8572E Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MDQ[0:63]	Data	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17	I/O	GV_{DD}	—
D1_MECC[0:7]	Error Correcting Code	M10, M7, R8, T11, L12, L11, P9, R10	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	P6	I	GV_{DD}	—
D1_MAPAR_OUT	Address Parity Out	W6	O	GV_{DD}	—
D1_MDM[0:8]	Data Mask	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11	O	GV_{DD}	—
D1_MDQS[0:8]	Data Strobe	A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS}}$[0:8]	Data Strobe	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	GV_{DD}	—
D1_MA[0:15]	Address	Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7	O	GV_{DD}	—
D1_MBA[0:2]	Bank Select	AA7, AA8, R7	O	GV_{DD}	—
$\overline{\text{D1\_MWE}}$	Write Enable	AC12	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	Write Enable	AA2	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	Column Address Strobe	AD1	O	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	Row Address Strobe	AA1	O	GV_{DD}	—
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	O	GV_{DD}	11
$\overline{\text{D2\_MCS}}$[0:3]	Chip Select	AB1, AG2, AC1, AH2	O	GV_{DD}	—
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	O	GV_{DD}	—
$\overline{\text{D2\_MCK}}$[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	O	GV_{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	O	GV_{DD}	—
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV_{DD}	25
Local Bus Controller Interface					
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV_{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV_{DD}	—
LA[27]	Burst Address	J21	O	BV_{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	O	BV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:4]	Chip Selects	B23, E16, D20, B25, A22	O	BV_{DD}	10
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA2\_DREQ}}$[1]	Chip Selects / DMA Request	D19	I/O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[6]/$\overline{\text{DMA2\_DACK}}$[1]	Chip Selects / DMA Ack	E19	O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[7]/$\overline{\text{DMA2\_DDONE}}$[1]	Chip Selects / DMA Done	C21	O	BV_{DD}	1, 10
$\overline{\text{LWE}}$[0]/$\overline{\text{LBS}}$[0]/$\overline{\text{LFWE}}$	Write Enable / Byte Select	D17	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$[1]	Write Enable / Byte Select	F15	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[2]/$\overline{\text{LBS}}$[2]	Write Enable / Byte Select	B24	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[3]/$\overline{\text{LBS}}$[3]	Write Enable / Byte Select	D18	O	BV_{DD}	5, 9
LALE	Address Latch Enable	F19	O	BV_{DD}	5, 8, 9
LBCTL	Buffer Control	L18	O	BV_{DD}	5, 8, 9

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0]	Receive Data Valid	AL24	I	LV_{DD}	1
TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1]	Receive Data Error	AM29	I	LV_{DD}	1
TSEC1_TX_CLK/FIFO1_TX_CLK	Transmit Clock In	AB20	I	LV_{DD}	1
TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0]	Transmit Enable	AJ24	O	LV_{DD}	1, 22
TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1]	Transmit Error	AK25	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 2					
TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8]	Receive Data	AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20	I	LV_{DD}	1
TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8]	Transmit Data	AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18	O	LV_{DD}	1, 5, 9, 24
TSEC2_COL/FIFO2_TX_FC	Collision Detect/Flow Control	AE19	I	LV_{DD}	1
TSEC2_CRS/FIFO2_RX_FC	Carrier Sense/Flow Control	AJ20	I/O	LV_{DD}	1, 16
TSEC2_GTX_CLK	Transmit Clock Out	AE18	O	LV_{DD}	—
TSEC2_RX_CLK/FIFO2_RX_CLK	Receive Clock	AL23	I	LV_{DD}	1
TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2]	Receive Data Valid	AJ22	I	LV_{DD}	1
TSEC2_RX_ER/FIFO2_RX_ER	Receive Data Error	AD19	I	LV_{DD}	1
TSEC2_TX_CLK/FIFO2_TX_CLK	Transmit Clock In	AC19	I	LV_{DD}	1
TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2]	Transmit Enable	AB19	O	LV_{DD}	1, 22
TSEC2_TX_ER/FIFO2_TX_ERR	Transmit Error	AB17	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 3					
TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0]	Transmit Data	AG18, AG17, AH17, AH19	O	TV_{DD}	1, 5, 9
TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0]	Receive Data	AG16, AK19, AD16, AJ19	I	TV_{DD}	1

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

Table 77. MPC8572E Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1067 MHz		1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” Section 19.3, “e500 Core PLL Ratio,” and Section 19.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.

Table 87. Part Numbering Nomenclature—Rev 2.1

MPC	*nnnn*	*e*	*t*	*l*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = –40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 150- MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included
		Blank = Not included					D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 88. Part Numbering Nomenclature—Rev 1.1.1

MPC	*nnnn*	*e*	*t*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank=0 to 105°C C= –40 to 105°C	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz process or; 667 MT/s DDR datarate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included
		Blank = Not included				B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.