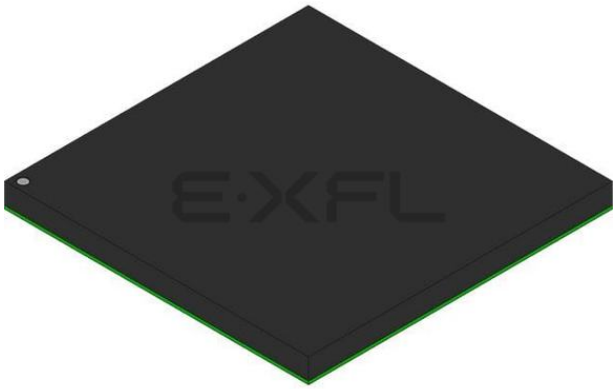

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572evtaulb

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
DDR2 signal	18 36 (half strength mode)	GV_{DD} = 1.8 V	2
DDR3 signal	20 40 (half strength mode)	GV_{DD} = 1.5 V	2
eTSEC/10/100 signals	45	L/TV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I2C	150	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD_SRDS1} and SV_{DD_SRDS2}, TV_{DD}, XV_{DD_SRDS1} and XV_{DD_SRDS2}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for GV_{DD} is not required.

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to $MV_{REF}n$. This rail should track variations in the DC level of $MV_{REF}n$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	µA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.175 V.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Notes:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2*t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.
2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	LV_{DD}/TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD}/TV_{DD} = Max, V_{IN} [3] = 2.1 V)	I_{IH}	—	40	µA	—

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=3.3 V) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV_{DD}/TV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	µA	—

Note:
1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbol referenced in Table 1.

Table 44. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=2.5 V)

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:

1 EC1_MDC and EC1_MDIO operate on LV_{DD}.
2 EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

9.2 MII Management AC Electrical Specifications

Table 45 provides the MII management AC timing specifications.There are three sets of Ethernet management signals (EC1_MDC and EC1_MDIO, EC3_MDC and EC3_MDIO, EC5_MDC and EC5_MDIO). These are not explicitly shown in the table or in the figure following.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
ECn_MDC frequency	f_{MDC}	0.9	2.5	9.3	MHz	2, 3
ECn_MDC period	t_{MDC}	107.5	—	1120	ns	—
ECn_MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
ECn_MDC to ECn_MDIO delay	t_{MDKHDX}	10	—	$16*t_{plb\_clk}$	ns	5

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
ECn_MDIO to ECn_MDC setup time	t_{MDDVKH}	5	—	—	ns	—
ECn_MDIO to ECn_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
ECn_MDC rise time	t_{MDCR}	—	—	10	ns	4
ECn_MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
4. Guaranteed by design.
5. t_{plb_clk} is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.

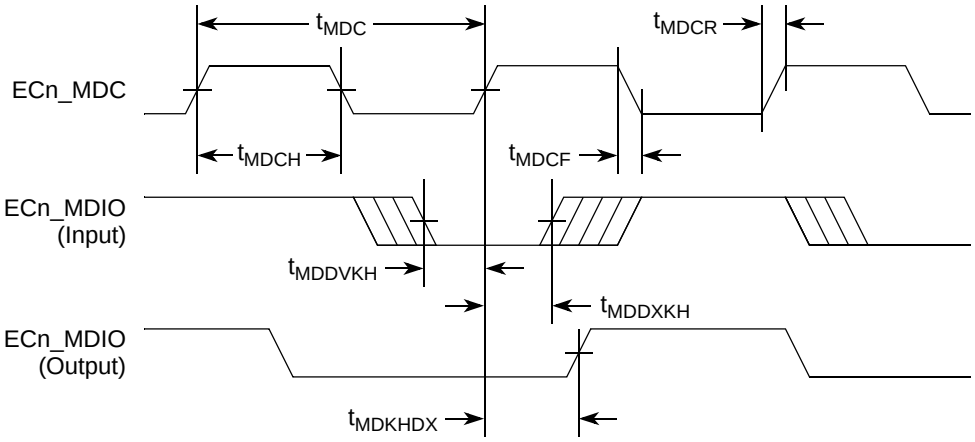


Figure 28. MII Management Interface Timing Diagram

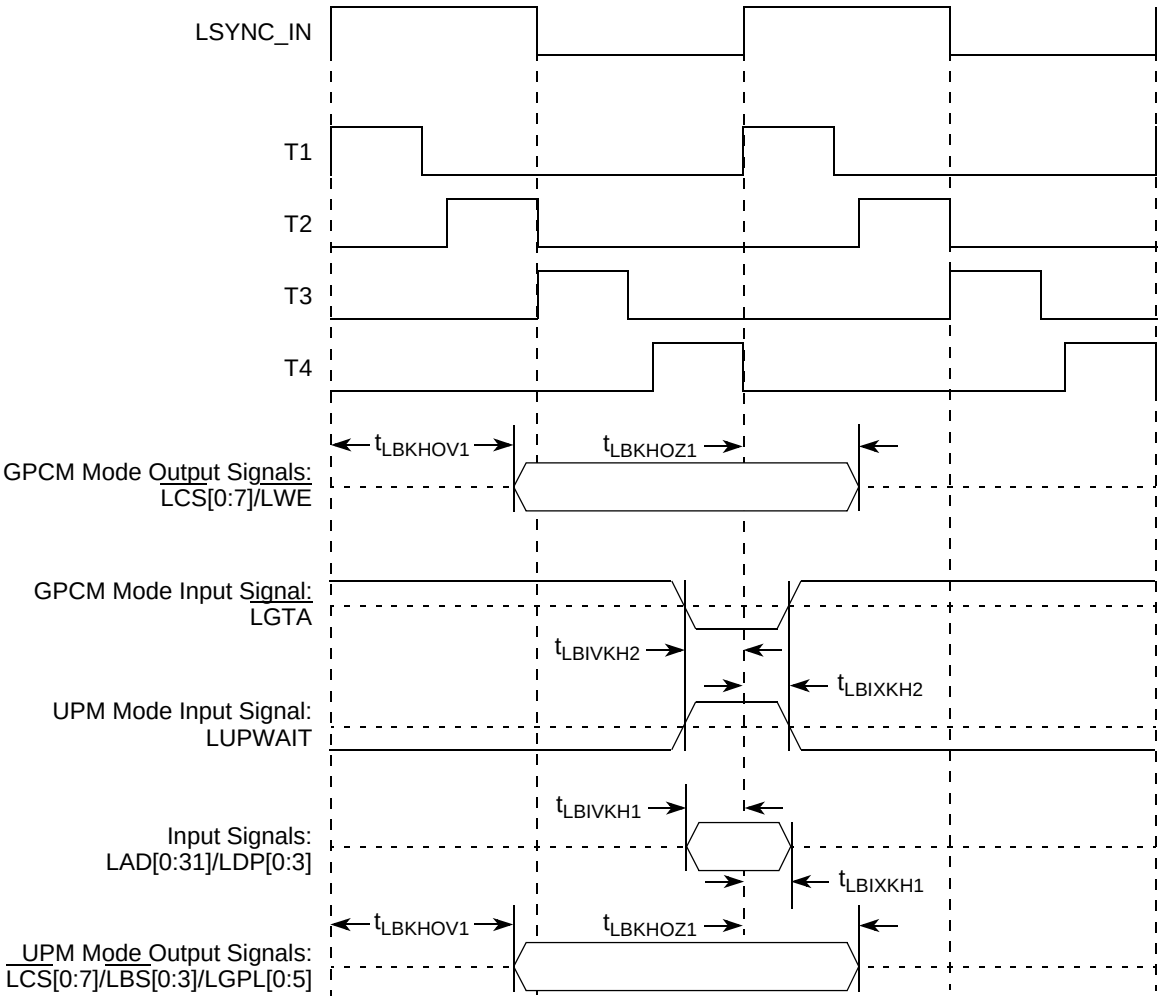


Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at BV_{DD} = 3.3 V DC.

Table 56. GPIO DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at BV_{DD} = 2.5 V DC.

Table 57. GPIO DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

- Section 17, “Serial RapidIO”

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

16.2 AC Requirements for PCI Express SerDes Reference Clocks

Table 61 lists AC requirements.

Table 61. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:
1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

16.4.1 Differential Transmitter (TX) Output

Table 62 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

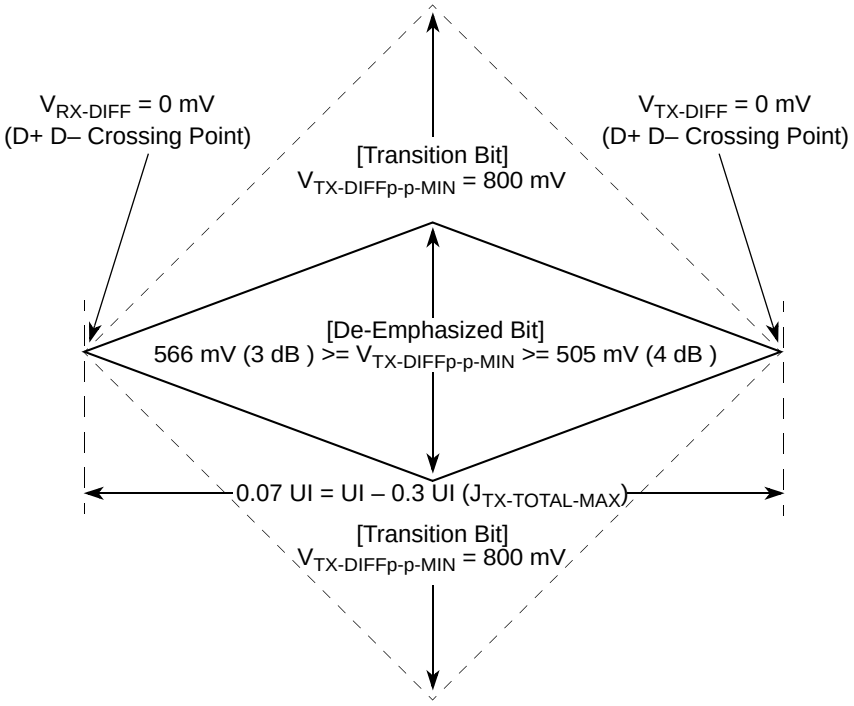


Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications

16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 63. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p}$ = 2*|V_{RX-D+} - V_{RX-D-}| See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

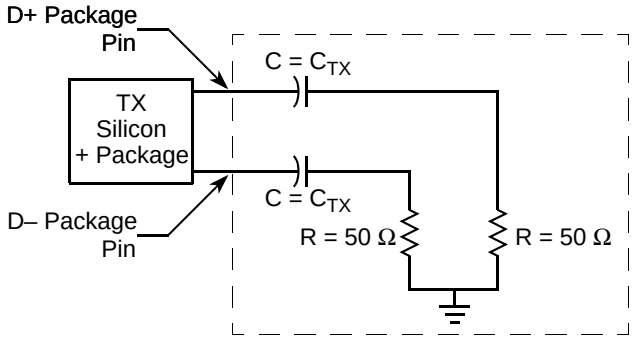


Figure 57. Compliance Test/Measurement Load

17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{D1\_MCAS}}$	Column Address Strobe	AC9	O	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	Row Address Strobe	AB12	O	GV_{DD}	—
D1_MCKE[0:3]	Clock Enable	M8, L9, T9, N8	O	GV_{DD}	11
$\overline{\text{D1\_MCS}}$[0:3]	Chip Select	AB9, AF10, AB11, AE11	O	GV_{DD}	—
D1_MCK[0:5]	Clock	V7, E13, AH11, Y9, F14, AG10	O	GV_{DD}	—
$\overline{\text{D1\_MCK}}$[0:5]	Clock Complements	Y10, E12, AH12, AA11, F13, AG11	O	GV_{DD}	—
D1_MODT[0:3]	On Die Termination	AD10, AF12, AC10, AE12	O	GV_{DD}	—
D1_MDIC[0:1]	Driver Impedance Calibration	E15, G14	I/O	GV_{DD}	25
DDR SDRAM Memory Interface 2					
D2_MDQ[0:63]	Data	A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7	I/O	GV_{DD}	—
D2_MECC[0:7]	Error Correcting Code	J5, H7, L7, N6, H4, H6, M4, M5	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N1	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	W2	O	GV_{DD}	—
D2_MDM[0:8]	Data Mask	A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5	O	GV_{DD}	—
D2_MDQS[0:8]	Data Strobe	B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS}}$[0:8]	Data Strobe	C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6	I/O	GV_{DD}	—
D2_MA[0:15]	Address	W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	Write Enable	AA2	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	Column Address Strobe	AD1	O	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	Row Address Strobe	AA1	O	GV_{DD}	—
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	O	GV_{DD}	11
$\overline{\text{D2\_MCS}}$[0:3]	Chip Select	AB1, AG2, AC1, AH2	O	GV_{DD}	—
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	O	GV_{DD}	—
$\overline{\text{D2\_MCK}}$[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	O	GV_{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	O	GV_{DD}	—
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV_{DD}	25
Local Bus Controller Interface					
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV_{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV_{DD}	—
LA[27]	Burst Address	J21	O	BV_{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	O	BV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:4]	Chip Selects	B23, E16, D20, B25, A22	O	BV_{DD}	10
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA2\_DREQ}}$[1]	Chip Selects / DMA Request	D19	I/O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[6]/$\overline{\text{DMA2\_DACK}}$[1]	Chip Selects / DMA Ack	E19	O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[7]/$\overline{\text{DMA2\_DDONE}}$[1]	Chip Selects / DMA Done	C21	O	BV_{DD}	1, 10
$\overline{\text{LWE}}$[0]/$\overline{\text{LBS}}$[0]/$\overline{\text{LFWE}}$	Write Enable / Byte Select	D17	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$[1]	Write Enable / Byte Select	F15	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[2]/$\overline{\text{LBS}}$[2]	Write Enable / Byte Select	B24	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[3]/$\overline{\text{LBS}}$[3]	Write Enable / Byte Select	D18	O	BV_{DD}	5, 9
LALE	Address Latch Enable	F19	O	BV_{DD}	5, 8, 9
LBCTL	Buffer Control	L18	O	BV_{DD}	5, 8, 9

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ\_OUT}}$	Interrupt Output	U24	O	OV_{DD}	2, 4
1588					
TSEC_1588_CLK	Clock In	AM22	I	LV_{DD}	—
TSEC_1588_TRIG_IN	Trigger In	AM23	I	LV_{DD}	—
TSEC_1588_TRIG_OUT	Trigger Out	AA23	O	LV_{DD}	5, 9
TSEC_1588_CLK_OUT	Clock Out	AC23	O	LV_{DD}	5, 9
TSEC_1588_PULSE_OUT1	Pulse Out1	AA22	O	LV_{DD}	5, 9
TSEC_1588_PULSE_OUT2	Pulse Out2	AB23	O	LV_{DD}	5, 9
Ethernet Management Interface 1					
EC1_MDC	Management Data Clock	AL30	O	LV_{DD}	5, 9
EC1_MDIO	Management Data In/Out	AM25	I/O	LV_{DD}	—
Ethernet Management Interface 3					
EC3_MDC	Management Data Clock	AF19	O	TV_{DD}	5, 9
EC3_MDIO	Management Data In/Out	AF18	I/O	TV_{DD}	—
Ethernet Management Interface 5					
EC5_MDC	Management Data Clock	AF14	O	TV_{DD}	21
EC5_MDIO	Management Data In/Out	AF15	I/O	TV_{DD}	—
Gigabit Ethernet Reference Clock					
EC_GTX_CLK125	Reference Clock	AM24	I	LV_{DD}	32
Three-Speed Ethernet Controller 1					
TSEC1_RXD[7:0]/FIFO1_RXD[7:0]	Receive Data	AM28, AL28, AM26, AK23, AM27, AK26, AL29, AM30	I	LV_{DD}	1
TSEC1_TXD[7:0]/FIFO1_TXD[7:0]	Transmit Data	AC20, AD20, AE22, AB22, AC22, AD21, AB21, AE21	O	LV_{DD}	1, 5, 9
TSEC1_COL/FIFO1_TX_FC	Collision Detect/Flow Control	AJ23	I	LV_{DD}	1
TSEC1_CRS/FIFO1_RX_FC	Carrier Sense/Flow Control	AM31	I/O	LV_{DD}	1, 16
TSEC1_GTX_CLK	Transmit Clock Out	AK27	O	LV_{DD}	
TSEC1_RX_CLK/FIFO1_RX_CLK	Receive Clock	AL25	I	LV_{DD}	1

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MSRCID[0:1]	Memory Debug Source Port ID	U27, T29	O	OV_{DD}	5, 9, 30
MSRCID[2:4]	Memory Debug Source Port ID	U28, W24, W28	O	OV_{DD}	21
MDVAL	Memory Debug Data Valid	V26	O	OV_{DD}	2, 21
CLK_OUT	Clock Out	U32	O	OV_{DD}	11
Clock					
RTC	Real Time Clock	V25	I	OV_{DD}	—
SYSCLK	System Clock	Y32	I	OV_{DD}	—
DDRCLK	DDR Clock	AA29	I	OV_{DD}	31
JTAG					
TCK	Test Clock	T28	I	OV_{DD}	
TDI	Test Data In	T27	I	OV_{DD}	12
TDO	Test Data Out	T26	O	OV_{DD}	—
TMS	Test Mode Select	U26	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test Reset	AA32	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 Test Clock	V32	I	OV_{DD}	18
L2_TSTCLK	L2 Test Clock	V31	I	OV_{DD}	18
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	N24	I	OV_{DD}	18
$\overline{\text{TEST\_SEL}}$	Test Select 0	K28	I	OV_{DD}	18
Power Management					
ASLEEP	Asleep	P28	O	OV_{DD}	9, 15, 21

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

Table 81. e500 Core1 to CCB Clock Ratio

Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Table 82. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1

Table 82. DDR Clock Ratio (continued)

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
101	12:1
110	14:1
111	Synchronous mode

19.5 Frequency Options

19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

Table 83. Frequency Options for Platform Frequency

CCB to SYSCLK Ratio	SYSCLK (MHz)							
	33.33	41.66	50	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)							
4						400	444	533
5					415	500	555	
6				400	498	600		
8			400	533				
10		417	500					
12	400	500	600					

19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, “I/O Port Selection,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, “Link Width,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the “PCI Express link width”

Figure 62 shows the PLL power supply filter circuits.

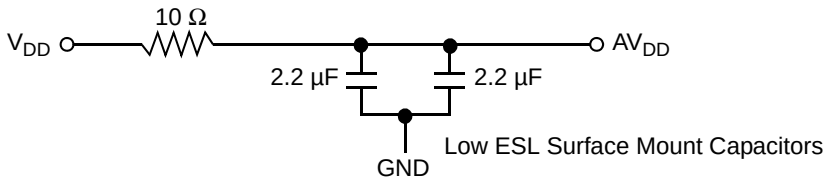
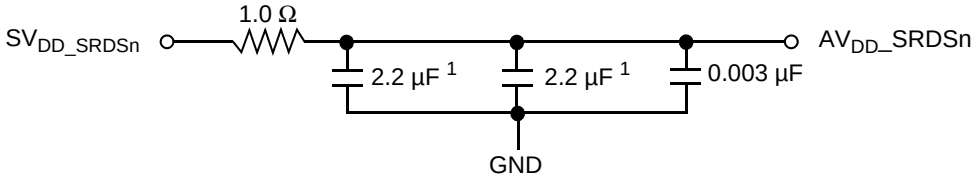


Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD}_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

AV_{DD}_SRDSn should be a filtered version of SV_{DD}_SRDS*n*.

NOTE

Signals on the SerDesn interface are fed from the XV_{DD}_SRDS*n* power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

This noise must be prevented from reaching other components in the MPC8572E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SV_{DD}_SRDSn and XV_{DD}_SRDSn) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (SV_{DD}_SRDSn and XV_{DD}_SRDSn) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND pins of the device.