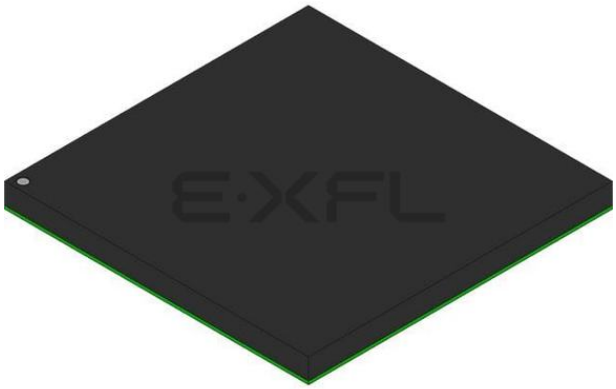

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.5GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 1023-BFBGA, FCBGA |
| Supplier Device Package | 1023-FCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572evtavnb |

- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing.
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
- Interrupt summary registers allow fast identification of interrupt source.

- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, SSL/TLS, SRTP, 802.16e, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 4096 bits
    - Elliptic curve cryptography with $F_2m$ and F(p) modes and programmable field size up to 1023 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB, CBC and OFB-64 modes for both DES and 3DES
  - AESU—Advanced Encryption Standard unit
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, CTR, CCM, GCM, CMAC, OFB-128, CFB-128, and LRW modes
    - 128-, 192-, and 256-bit key lengths
  - AFEU—ARC four execution unit
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - MDEU—message digest execution unit
    - SHA-1 with 160-bit message digest
    - SHA-2 (SHA-256, SHA-384, SHA-512)
    - MD5 with 128-bit message digest
    - HMAC with all algorithms
  - KEU—Kasumi execution unit
    - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
    - Also supports A5/3 and GEA-3 algorithms
  - RNG—random number generator
  - XOR engine for parity checking in RAID storage applications
  - CRC execution unit
    - CRC-32 and CRC-32C
- Pattern Matching Engine with DEFLATE decompression

## 2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

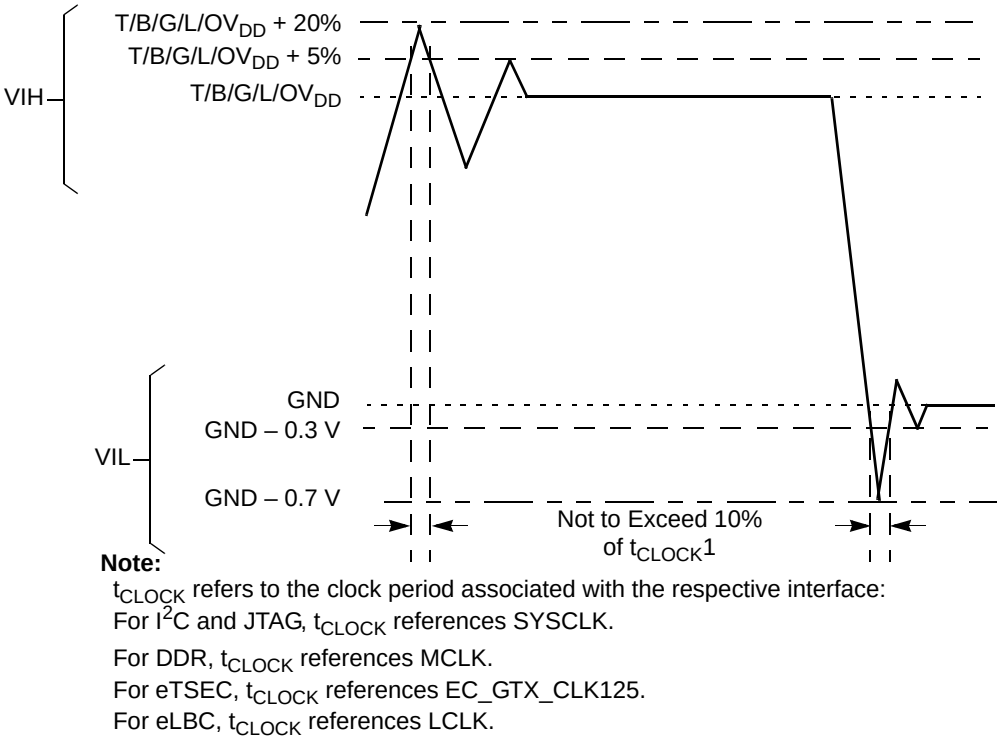
**Table 2. Recommended Operating Conditions**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | 1.1 V ± 55 mV | V | — |
| PLL supply voltage | | $AV_{DD}$ | 1.1 V ± 55 mV | V | 1 |
| Core power supply for SerDes transceivers | | $SV_{DD}$ | 1.1 V ± 55 mV | V | — |
| Pad power supply for SerDes transceivers | | $XV_{DD}$ | 1.1 V ± 55 mV | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | 1.8 V ± 90 mV | V | — |
| | DDR3 SDRAM Interface | | 1.5 V ± 75 mV | | — |
| Three-speed Ethernet I/O voltage | | $LV_{DD}$<br>$TV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>3.3 V ± 165 mV<br>2.5 V ± 125 mV | V | 4<br>4 |
| DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 3 |
| Local bus and GPIO I/O voltage | | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | — |
| Input voltage | DDR2 and DDR3 SDRAM Interface signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | 2 |
| | DDR2 and DDR3 SDRAM Interface reference | $MV_{REF}n$ | $GV_{DD}/2$ ± 1% | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to $LV_{DD}$<br>GND to $TV_{DD}$ | V | 4 |
| | Local bus and GPIO signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | — |
| | Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | GND to $OV_{DD}$ | V | 3 |
| Junction temperature range | | $T_J$ | 0 to 105 | °C | — |

**Notes:**

1. This voltage is the input to the filter discussed in Section 21.2.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the $AV_{DD}$ pin, that may be reduced from $V_{DD}$ by the filter.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $L/TV_{IN}$ must not exceed $L/TV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8572E.




**Note:**
$t_{CLOCK}$ refers to the clock period associated with the respective interface:
For $I^2C$ and JTAG, $t_{CLOCK}$ references SYSCLK.
For DDR, $t_{CLOCK}$ references MCLK.
For eTSEC, $t_{CLOCK}$ references EC_GTX_CLK125.
For eLBC, $t_{CLOCK}$ references LCLK.

**Figure 2. Overshoot/Undershoot Voltage for $TV_{DD}/BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$**

The core voltage must always be provided at nominal 1.1 V. (See Table 2 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Figure 9 shows the GMII transmit AC timing diagram.

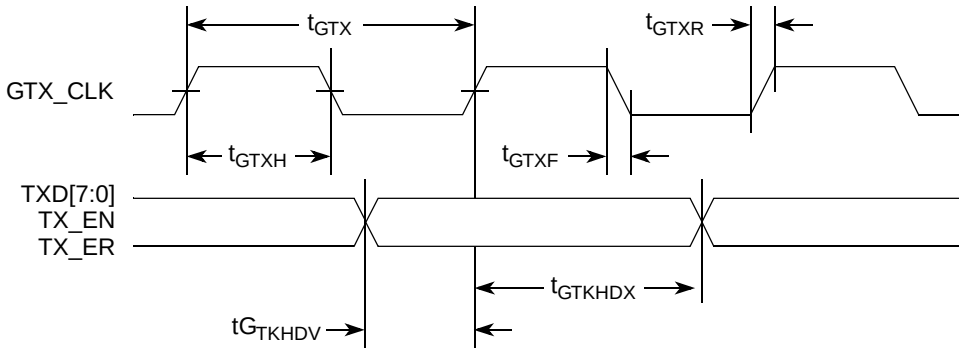



**Figure 9. GMII Transmit AC Timing Diagram**

### 8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

**Table 28. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0 | — | — | ns |
| RX_CLK clock rise (20%-80%) | $t_{GRXR}$[2] | — | — | 1.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{GRXF}$[2] | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

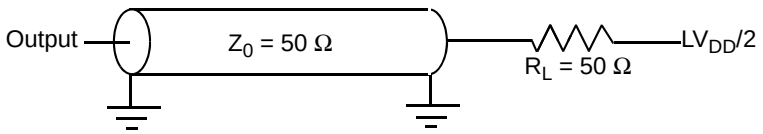



**Figure 10. eTSEC AC Test Load**

### 8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX[n]}}$) as depicted in Figure 23.

**Table 38. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| Output high voltage | VOH | — | — | $XV_{DD\_SRDS2-Typ}/2 + \lvert\overline{V_{OD}}\rvert_{-max}/2$ | mV | 1 |
| Output low voltage | VOL | $XV_{DD\_SRDS2-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | — |
| Output differential voltage[2, 3, 5] | $\lvert V_{OD}\rvert$ | 359 | 550 | 791 | mV | Equalization setting: 1.0x |
| | | 329 | 505 | 725 | | Equalization setting: 1.09x |
| | | 299 | 458 | 659 | | Equalization setting: 1.2x |
| | | 270 | 414 | 594 | | Equalization setting: 1.33x |
| | | 239 | 367 | 527 | | Equalization setting: 1.5x |
| | | 210 | 322 | 462 | | Equalization setting: 1.71x |
| | | 180 | 275 | 395 | | Equalization setting: 2.0x |
| Output offset voltage | $V_{OS}$ | 473 | 550 | 628 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | — |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | — |
| Change in $V_{OD}$ between “0” and “1” | $\Delta \lvert V_{OD}\rvert$ | — | — | 25 | mV | — |

## 8.4 eTSEC IEEE Std 1588™ AC Specifications

Figure 26 shows the data and command output timing diagram.

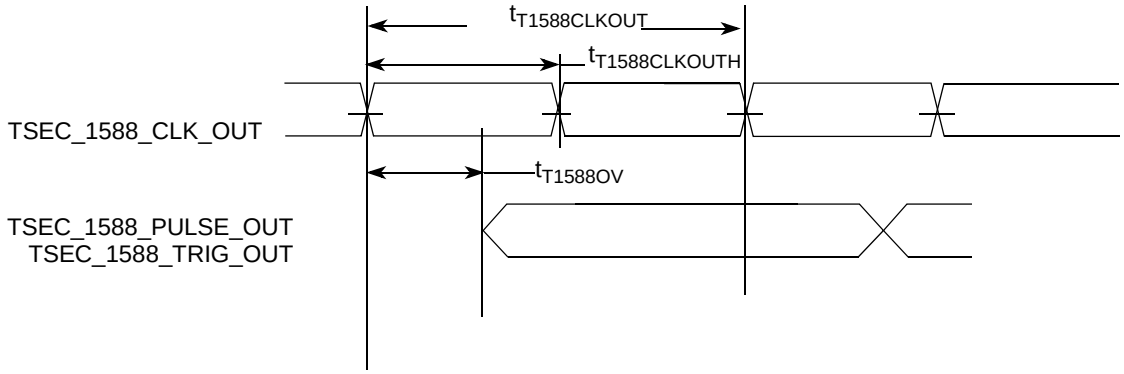



**Figure 26. eTSEC IEEE 1588 Output AC Timing**

1 The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 27 shows the data and command input timing diagram.

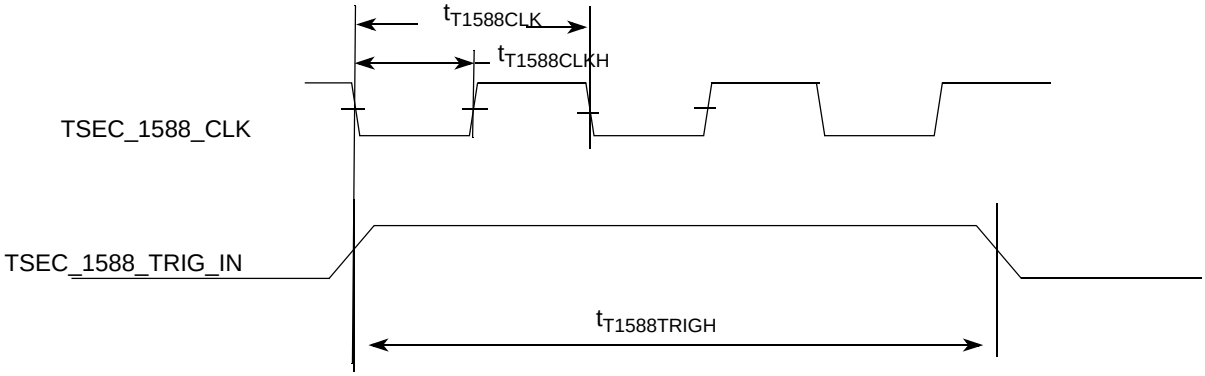



**Figure 27. eTSEC IEEE 1588 Input AC timing**

Table 42 provides the IEEE 1588 AC timing specifications.

**Table 42. eTSEC IEEE 1588 AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK clock period | $t_{T1588CLK}$ | 3.3 | — | $T_{TX\_CLK}$*9 | ns | 1 |
| TSEC_1588_CLK duty cycle | $t_{T1588CLKH}$ /$t_{T1588CLK}$ | 40 | 50 | 60 | % | — |
| TSEC_1588_CLK peak-to-peak jitter | $t_{T1588CLKINJ}$ | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | $t_{T1588CLKINR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | $t_{T1588CLKINF}$ | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | $t_{T1588CLKOUT}$ | 2*$t_{T1588CLK}$ | — | — | ns | — |

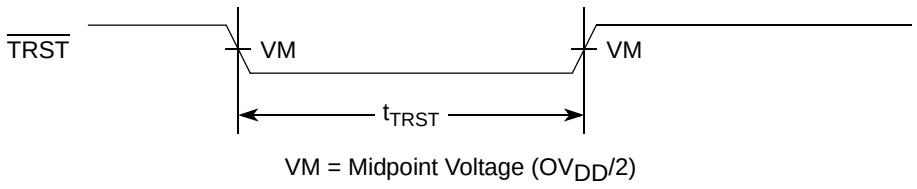



**Figure 38. $\overline{\text{TRST}}$ Timing Diagram**

Figure 39 provides the boundary-scan timing diagram.

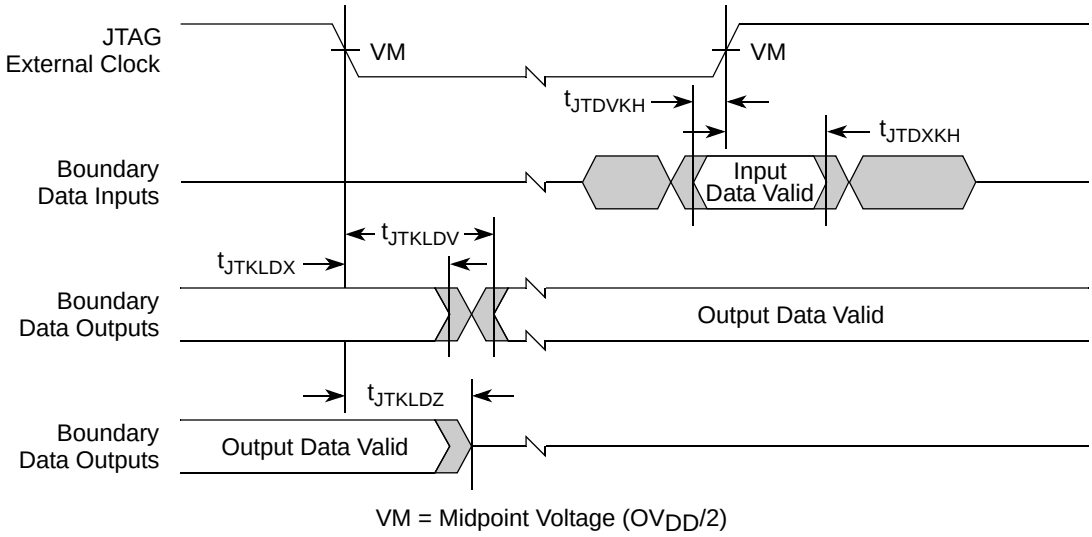



**Figure 39. Boundary-Scan Timing Diagram**

# 13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8572E.

## 13.1 I²C DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the I²C interfaces.

**Table 54. I²C DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.4 | V | 1 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 2 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | µA | 3 |

**Table 63. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7. |
| $V_{RX-CM-ACp}$ | AC Peak Common Mode Input Voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$<br>$V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$<br>See Note 2 |
| $RL_{RX-DIFF}$ | Differential Return Loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.<br>See Note 4 |
| $RL_{RX-CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4 |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC Differential mode impedance. See Note 5 |
| $Z_{RX-DC}$ | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 200 k | — | — | Ω | Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$<br>Measured at the package pins of the Receiver |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms | An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |

## 17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

## 17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

**Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10(8) | — | ns | 8 ns applies only to serial RapidIO with 125-MHz reference clock |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 80 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –40 | — | 40 | ps | — |

## 17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Package outline | 33 mm × 33 mm |
| Interconnects | 1023 |
| Ball Pitch | 1 mm |
| Ball Diameter (Typical) | 0.6 mm |
| Solder Balls | 63% Sn |
| | 37% Pb |
| Solder Balls (Lead-Free) | 96.5% Sn |
| | 3.5% Ag |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0] | Receive Data Valid | AL24 | I | $LV_{DD}$ | 1 |
| TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1] | Receive Data Error | AM29 | I | $LV_{DD}$ | 1 |
| TSEC1_TX_CLK/FIFO1_TX_CLK | Transmit Clock In | AB20 | I | $LV_{DD}$ | 1 |
| TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0] | Transmit Enable | AJ24 | O | $LV_{DD}$ | 1, 22 |
| TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1] | Transmit Error | AK25 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 2** | | | | | |
| TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8] | Receive Data | AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20 | I | $LV_{DD}$ | 1 |
| TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8] | Transmit Data | AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18 | O | $LV_{DD}$ | 1, 5, 9, 24 |
| TSEC2_COL/FIFO2_TX_FC | Collision Detect/Flow Control | AE19 | I | $LV_{DD}$ | 1 |
| TSEC2_CRS/FIFO2_RX_FC | Carrier Sense/Flow Control | AJ20 | I/O | $LV_{DD}$ | 1, 16 |
| TSEC2_GTX_CLK | Transmit Clock Out | AE18 | O | $LV_{DD}$ | — |
| TSEC2_RX_CLK/FIFO2_RX_CLK | Receive Clock | AL23 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2] | Receive Data Valid | AJ22 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_ER/FIFO2_RX_ER | Receive Data Error | AD19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_CLK/FIFO2_TX_CLK | Transmit Clock In | AC19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2] | Transmit Enable | AB19 | O | $LV_{DD}$ | 1, 22 |
| TSEC2_TX_ER/FIFO2_TX_ERR | Transmit Error | AB17 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 3** | | | | | |
| TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0] | Transmit Data | AG18, AG17, AH17, AH19 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0] | Receive Data | AG16, AK19, AD16, AJ19 | I | $TV_{DD}$ | 1 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| MSRCID[0:1] | Memory Debug Source Port ID | U27, T29 | O | $OV_{DD}$ | 5, 9, 30 |
| MSRCID[2:4] | Memory Debug Source Port ID | U28, W24, W28 | O | $OV_{DD}$ | 21 |
| MDVAL | Memory Debug Data Valid | V26 | O | $OV_{DD}$ | 2, 21 |
| CLK_OUT | Clock Out | U32 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | | |
| RTC | Real Time Clock | V25 | I | $OV_{DD}$ | — |
| SYSCLK | System Clock | Y32 | I | $OV_{DD}$ | — |
| DDRCLK | DDR Clock | AA29 | I | $OV_{DD}$ | 31 |
| **JTAG** | | | | | |
| TCK | Test Clock | T28 | I | $OV_{DD}$ | |
| TDI | Test Data In | T27 | I | $OV_{DD}$ | 12 |
| TDO | Test Data Out | T26 | O | $OV_{DD}$ | — |
| TMS | Test Mode Select | U26 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | Test Reset | AA32 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | | |
| L1_TSTCLK | L1 Test Clock | V32 | I | $OV_{DD}$ | 18 |
| L2_TSTCLK | L2 Test Clock | V31 | I | $OV_{DD}$ | 18 |
| $\overline{\text{LSSD\_MODE}}$ | LSSD Mode | N24 | I | $OV_{DD}$ | 18 |
| $\overline{\text{TEST\_SEL}}$ | Test Select 0 | K28 | I | $OV_{DD}$ | 18 |
| **Power Management** | | | | | |
| ASLEEP | Asleep | P28 | O | $OV_{DD}$ | 9, 15, 21 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SGND_SRDS1 | SerDes Transceiver Core Logic GND (xcorevss) | C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32 | — | — | — |
| SGND_SRDS2 | SerDes Transceiver Core Logic GND (xcorevss) | AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32 | — | — | — |
| AGND_SRDS1 | SerDes PLL GND | J31 | — | — | — |
| AGND_SRDS2 | SerDes PLL GND | AH31 | — | — | — |
| OVDD | General I/O Supply | U31, V24, V28, Y31, AA27, AB25, AB29 | — | OVDD | — |
| LVDD | TSEC 1&2 I/O Supply | AC18, AC21, AG21, AL27 | — | LVDD | — |
| TVDD | TSEC 3&4 I/O Supply | AC15, AE16, AH18 | — | TVDD | — |
| GVDD | SSTL_1.8 DDR Supply | B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2 | — | GVDD | — |
| BVDD | Local Bus and GPIO Supply | A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20 | — | BVDD | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| VDD | Core, L2, Logic Supply | L14, M13, M15, M17, N12, N14, N16, N20, N22, P11, P13, P15, P17, P19, P21, P23, R12, R14, R16, R18, R20, R22, T13, T15, T19, T21, T23, U12, U14, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA12, AA14, AA16, AA18, AA20, AB13 | — | VDD | — |
| SVDD_SRDS1 | SerDes Core 1 Logic Supply (xcorevdd) | C31, D29, E28, E32, F30, G28, G31, H29, K30, L31, M29, N32, P30 | — | — | — |
| SVDD_SRDS2 | SerDes Core 2 Logic Supply (xcorevdd) | AD32, AF31, AG29, AJ32, AK29, AK30 | — | — | — |
| XVDD_SRDS1 | SerDes1 Transceiver Supply (xpadvdd) | C26, D24, E27, F25, G26, H24, J27, K25, L26, M24, N27 | — | — | — |
| XVDD_SRDS2 | SerDes2 Transceiver Supply (xpadvdd) | AD24, AD28, AE26, AF25, AG27, AH24, AJ26 | — | — | — |
| AVDD_LBIU | Local Bus PLL Supply | A19 | — | — | 19 |
| AVDD_DDR | DDR PLL Supply | AM20 | — | — | 19 |
| AVDD_CORE0 | CPU PLL Supply | B18 | — | — | 19 |
| AVDD_CORE1 | CPU PLL Supply | A17 | — | — | 19 |
| AVDD_PLAT | Platform PLL Supply | AB32 | — | — | 19 |
| AVDD_SRDS1 | SerDes1 PLL Supply | J29 | — | — | 19 |
| AVDD_SRDS2 | SerDes2 PLL Supply | AH29 | — | — | 19 |
| SENSEVDD | VDD Sensing Pin | N18 | — | — | 13 |
| SENSEVSS | GND Sensing Pin | P18 | — | — | 13 |
| **Analog Signals** | | | | | |
| MVREF1 | SSTL_1.8 Reference Voltage | C16 | I | $GV_{DD}/2$ | — |
| MVREF2 | SSTL_1.8 Reference Voltage | AM19 | I | $GV_{DD}/2$ | — |

# 19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

**Table 77. MPC8572E Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1067 MHz | | 1200 MHz | | 1333 MHz | | 1500 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 800 | 1067 | 800 | 1200 | 800 | 1333 | 800 | 1500 | MHz | 1, 2 |
| CCB frequency | 400 | 533 | 400 | 533 | 400 | 533 | 400 | 600 | MHz | |
| DDR Data Rate | 400 | 667 | 400 | 667 | 400 | 667 | 400 | 800 | MHz | |

**Notes**:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” Section 19.3, “e500 Core PLL Ratio,” and Section 19.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.

**Table 78. Memory Bus Clocking Specifications**

| Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Memory bus clock frequency | 200 | 400 | MHz | 1, 2, 3, 4 |

**Notes:**
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn\_MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in Table 80 and Table 81;
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from Table 79;
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 82. Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

## 19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 79:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

**Table 82. DDR Clock Ratio (continued)**

| Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals | DDR:DDRCLK Ratio |
|---|---|
| 101 | 12:1 |
| 110 | 14:1 |
| 111 | Synchronous mode |

## 19.5 Frequency Options

### 19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

**Table 83. Frequency Options for Platform Frequency**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 33.33 | 41.66 | 50 | 66.66 | 83 | 100 | 111 | 133.33 |
| | Platform /CCB Frequency (MHz) | | | | | | | |
| **4** | | | | | | 400 | 444 | 533 |
| **5** | | | | | 415 | 500 | 555 | |
| 6 | | | | 400 | 498 | 600 | | |
| **8** | | | 400 | 533 | | | | |
| **10** | | 417 | 500 | | | | | |
| **12** | 400 | 500 | 600 | | | | | |

### 19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, “I/O Port Selection,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, “Link Width,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the “PCI Express link width”

## 21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including $I^2C$ pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA\_DACK}}$[0:1], EC5_MDC, $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$, MSRCID[2:4], MDVAL, and ASLEEP. The $\overline{\text{TEST\_SEL}}$ pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

## 21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

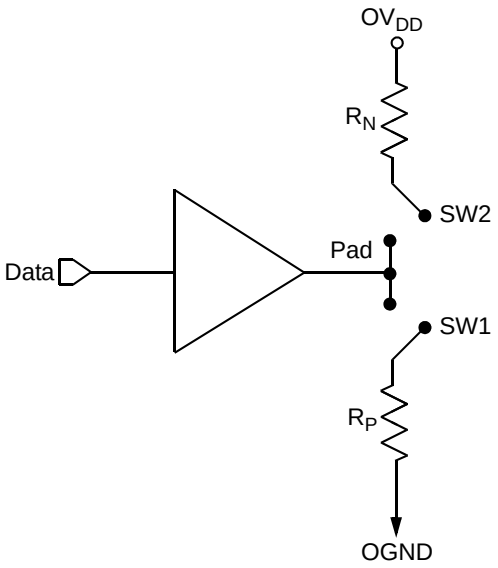



**Figure 64. Driver Impedance Measurement**

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

### 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

# 22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 22.1, “Part Numbers Fully Addressed by this Document.”

## 22.1 Part Numbers Fully Addressed by this Document

Table 86 through Table 88 provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 86. Part Numbering Nomenclature—Rev 2.2.1**

| MPC | *nnnn* | *e* | *t* | *l* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|---|
| **Product Code[1]** | **Part Identifier** | **Security Engine** | **Temperature** | **Power** | **Package Sphere Type[2]** | **Processor Frequency/ DDR Data Rate[3]** | **Silicon Revision** |
| MPC<br>PPC | 8572 | E = Included | Blank = 0 to 105°C<br>C = –40 to 105°C | Blank = Standard<br>L = Low | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA[4]<br>VJ = Fully Pb-free FC-PBGA[5] | AVN = 1500-MHz processor; 800 MT/s DDR data rate<br><br>AUL = 1333-MHz processor; 667 MT/s DDR data rate<br><br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br><br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included |
| | | Blank = Not included | | | | | E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included |

**Notes:**

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

4. The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.

5. The VJ part number is entirely lead-free. This includes the C4 die bumps.