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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8572evtavnd">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8572evtavnd</a>

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- 10/100 Fast Ethernet controller (FEC) management interface
  - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
  - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
  - Four DMA channels per controller
  - All channels accessible by the local masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
  - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins (DMA2\_DREQ[2]) is made available

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

### 8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in [Table 24](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	$V_{DD}$ $V_{TVDD}$	3.13	3.47	V	1, 2
Output high voltage ( $V_{DD}/V_{TVDD} = \text{Min}$ , $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.40	$V_{DD}/V_{TVDD} + 0.3$	V	—
Output low voltage ( $V_{DD}/V_{TVDD} = \text{Min}$ , $I_{OL} = 4.0 \text{ mA}$ )	$V_{OL}$	GND	0.50	V	—
Input high voltage	$V_{IH}$	2.0	$V_{DD}/V_{TVDD} + 0.3$	V	—
Input low voltage	$V_{IL}$	-0.3	0.90	V	—
Input high current ( $V_{IN} = V_{DD}$ , $V_{IN} = V_{TVDD}$ )	$I_{IH}$	—	40	$\mu\text{A}$	1, 2, 3
Input low current ( $V_{IN} = \text{GND}$ )	$I_{IL}$	-600	—	$\mu\text{A}$	3

**Notes:**

- <sup>1</sup>  $V_{DD}$  supports eTSECs 1 and 2.
- <sup>2</sup>  $V_{TVDD}$  supports eTSECs 3 and 4 or FEC.
- <sup>3</sup> The symbol  $V_{IN}$ , in this case, represents the  $V_{DD}$  and  $V_{TVDD}$  symbols referenced in [Table 1](#).

**Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics**

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	$V_{DD}/V_{TVDD}$	2.37	2.63	V	1,2
Output high voltage ( $V_{DD}/V_{TVDD} = \text{Min}$ , $I_{OH} = -1.0 \text{ mA}$ )	$V_{OH}$	2.00	$V_{DD}/V_{TVDD} + 0.3$	V	—
Output low voltage ( $V_{DD}/V_{TVDD} = \text{Min}$ , $I_{OL} = 1.0 \text{ mA}$ )	$V_{OL}$	GND - 0.3	0.40	V	—
Input high voltage	$V_{IH}$	1.70	$V_{DD}/V_{TVDD} + 0.3$	V	—
Input low voltage	$V_{IL}$	-0.3	0.70	V	—

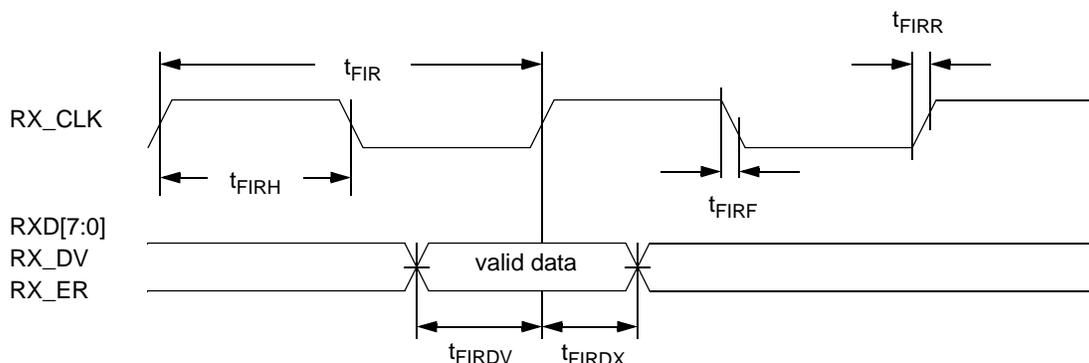


Figure 8. FIFO Receive AC Timing Diagram

## 8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/TV_{DD}$  of 2.5/ 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	$t_{GTKHDV}$	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	$t_{GTKHDX}$	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	$t_{GTXR}^2$	—	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	$t_{GTXF}^2$	—	—	1.0	ns

**Notes:**

- The symbols used for timing specifications herein follow the pattern  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{GTKHDV}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also,  $t_{GTKHDX}$  symbolizes GMII transmit timing (GT) with respect to the  $t_{GTX}$  clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GTX}$  represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 9 shows the GMII transmit AC timing diagram.

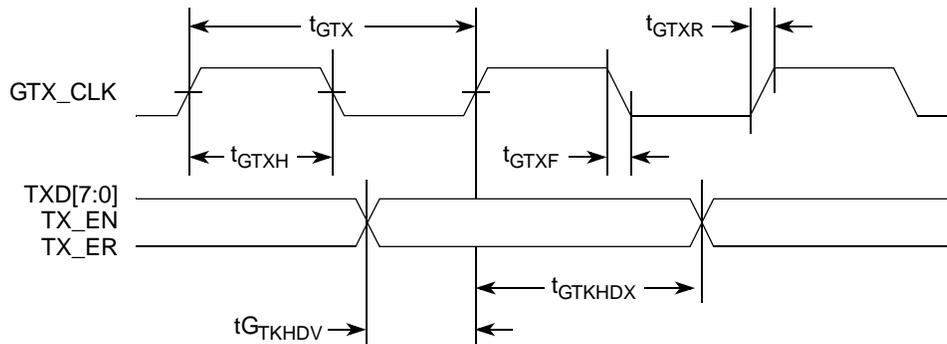


Figure 9. GMII Transmit AC Timing Diagram

### 8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with  $V_{DD}/TV_{DD}$  of 2.5/ 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
RX_CLK clock period	$t_{GRX}$	—	8.0	—	ns
RX_CLK duty cycle	$t_{GRXH}/t_{GRX}$	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	$t_{GRDVKH}$	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	$t_{GRDXKH}$	0	—	—	ns
RX_CLK clock rise (20%-80%)	$t_{GRXR}^2$	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	$t_{GRXF}^2$	—	—	1.0	ns

**Note:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{GRDVKH}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{RX}$  clock reference (K) going to the high state (H) or setup time. Also,  $t_{GRDXKL}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{GRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GRX}$  represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

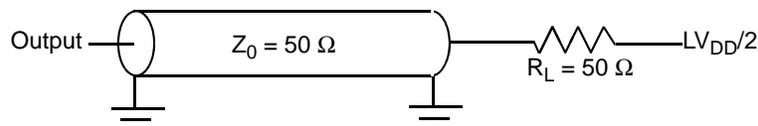


Figure 10. eTSEC AC Test Load

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

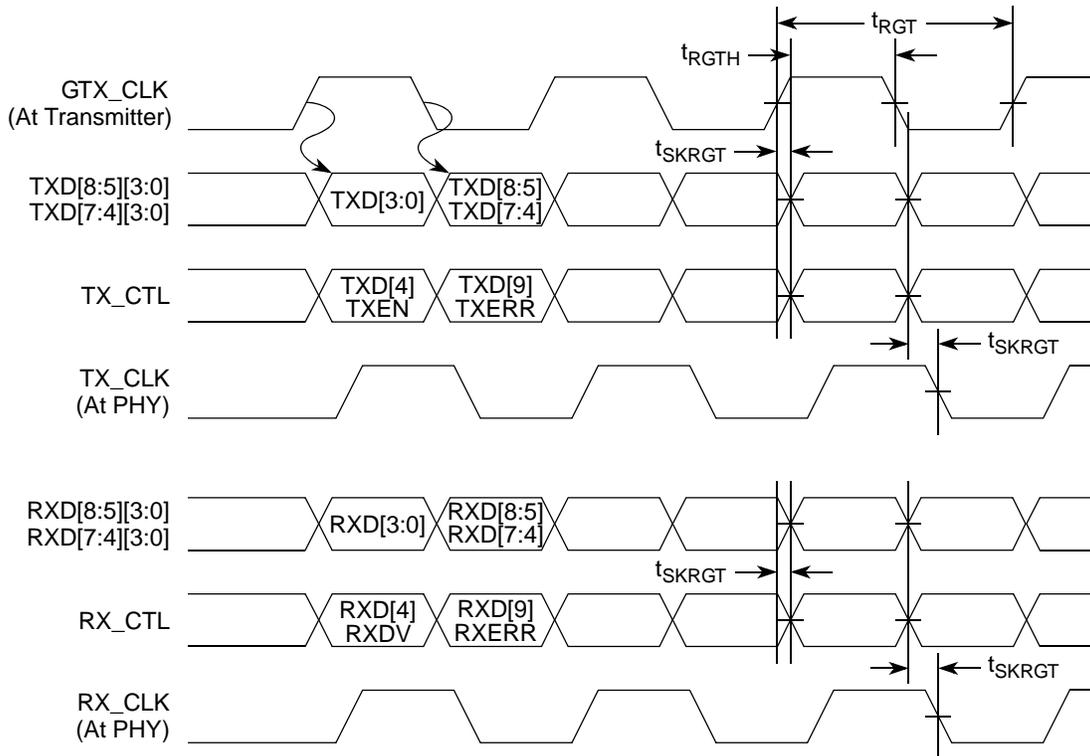


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

## 8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV<sub>DD</sub>/TV<sub>DD</sub> of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t <sub>RMT</sub>	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t <sub>RMTH</sub>	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t <sub>RMTJ</sub>	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t <sub>RMTR</sub>	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t <sub>RMTF</sub>	1.0	—	2.0	ns

**Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)**

 At recommended operating conditions with  $BV_{DD}$  of  $3.3\text{ V} \pm 5\%$ 

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-1.3	—	ns	4, 5
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	$t_{LBOTOT}$	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	-0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	-0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0.0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-3.3	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-3.3	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

**Notes:**

- The symbols used for timing specifications herein follow the pattern of  $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{LBIXKH1}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{LBK}$  clock reference (K) goes high (H), in this case for clock one(1). Also,  $t_{LBKHGX}$  symbolizes local bus timing (LB) for the  $t_{LBK}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by  $t_{LBKHKT}$ .
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at  $BV_{DD}/2$ .
- All signals are measured from  $BV_{DD}/2$  of the rising edge of local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- $t_{LBOTOT}$  is a measurement of the minimum time between the negation of LALE and any change in LAD.  $t_{LBOTOT}$  is programmed with the LBCR[AHD] parameter.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

**NOTE**

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of  $t_{LBKHKT}$ . In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of  $\overline{\text{LGTA/LUPWAIT}}$  (which is captured on the rising edge of the internal clock).

Local Bus Controller (eLBC)

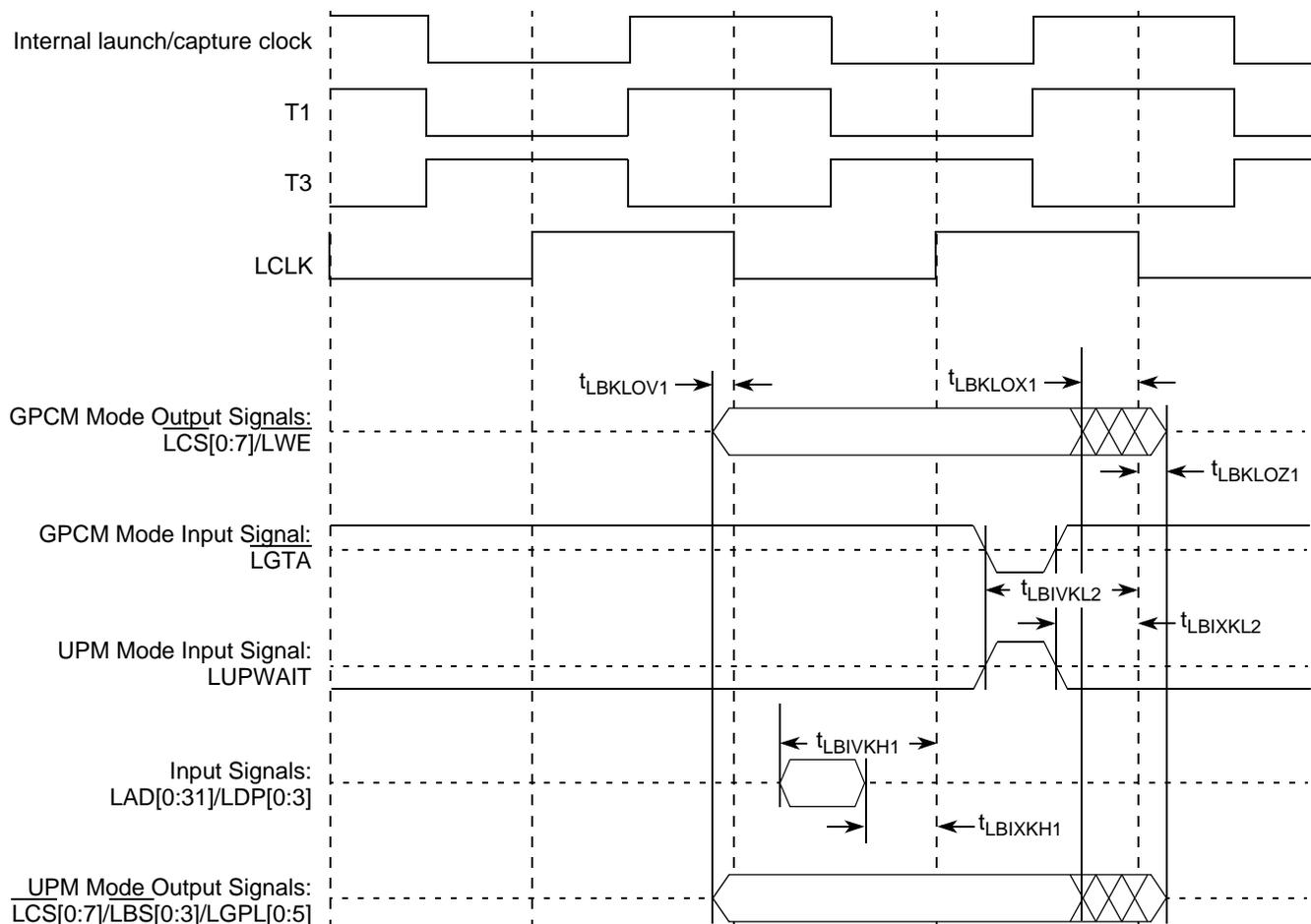


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

**Table 54. I<sup>2</sup>C DC Electrical Characteristics (continued)**

Capacitance for each I/O pin	C <sub>I</sub>	—	10	pF	—
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**Notes:**

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV<sub>DD</sub> is switched off.

## 13.2 I<sup>2</sup>C AC Electrical Specifications

Table 55 provides the AC timing parameters for the I<sup>2</sup>C interfaces.

**Table 55. I<sup>2</sup>C AC Electrical Specifications**

At recommended operating conditions with OV<sub>DD</sub> of 3.3 V ± 5%. All values refer to V<sub>IH</sub> (min) and V<sub>IL</sub> (max) levels (see Table 2).

Parameter	Symbol <sup>1</sup>	Min	Max	Unit
SCL clock frequency	f <sub>I2C</sub>	0	400	kHz <sup>4</sup>
Low period of the SCL clock	t <sub>I2CL</sub>	1.3	—	μs
High period of the SCL clock	t <sub>I2CH</sub>	0.6	—	μs
Setup time for a repeated START condition	t <sub>I2SVKH</sub>	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t <sub>I2SXKL</sub>	0.6	—	μs
Data setup time	t <sub>I2DVKH</sub>	100	—	ns
Data input hold time: CBUS compatible masters I <sup>2</sup> C bus devices	t <sub>I2DXKL</sub>	— 0 <sup>2</sup>	— —	μs
Data output delay time	t <sub>I2OVKL</sub>	—	0.9 <sup>3</sup>	μs
Setup time for STOP condition	t <sub>I2PVKH</sub>	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>I2KHDX</sub>	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	0.1 × OV <sub>DD</sub>	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	0.2 × OV <sub>DD</sub>	—	V

# 14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

## 14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at  $BV_{DD} = 3.3$  V DC.

**Table 56. GPIO DC Electrical Characteristics (3.3 V DC)**

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	$BV_{DD}$	3.13	3.47	V
High-level input voltage	$V_{IH}$	2	$BV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
Input current ( $BV_{IN}^1 = 0$ V or $BV_{IN} = BV_{DD}$ )	$I_{IN}$	—	$\pm 5$	$\mu A$
High-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OH} = -2$ mA)	$V_{OH}$	$BV_{DD} - 0.2$	—	V
Low-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OL} = 2$ mA)	$V_{OL}$	—	0.2	V

**Note:**

- Note that the symbol  $BV_{IN}$ , in this case, represents the  $BV_{IN}$  symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at  $BV_{DD} = 2.5$  V DC.

**Table 57. GPIO DC Electrical Characteristics (2.5 V DC)**

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	$BV_{DD}$	2.37	2.63	V
High-level input voltage	$V_{IH}$	1.70	$BV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.7	V
Input current ( $BV_{IN}^1 = 0$ V or $BV_{IN} = BV_{DD}$ )	$I_{IH}$	—	10	$\mu A$
	$I_{IL}$		-15	
High-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OH} = -1$ mA)	$V_{OH}$	2.0	$BV_{DD} + 0.3$	V
Low-level output voltage ( $BV_{DD} = \text{min}$ , $I_{OL} = 1$ mA)	$V_{OL}$	GND - 0.3	0.4	V

**Note:**

- The symbol  $BV_{IN}$ , in this case, represents the  $BV_{IN}$  symbol referenced in Table 1.

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

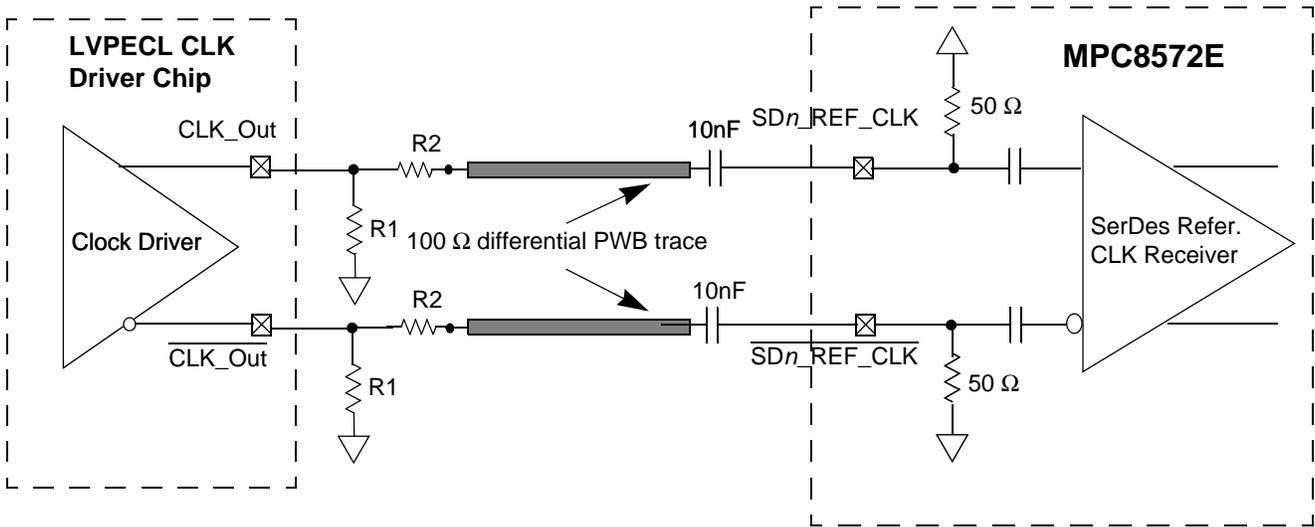


Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

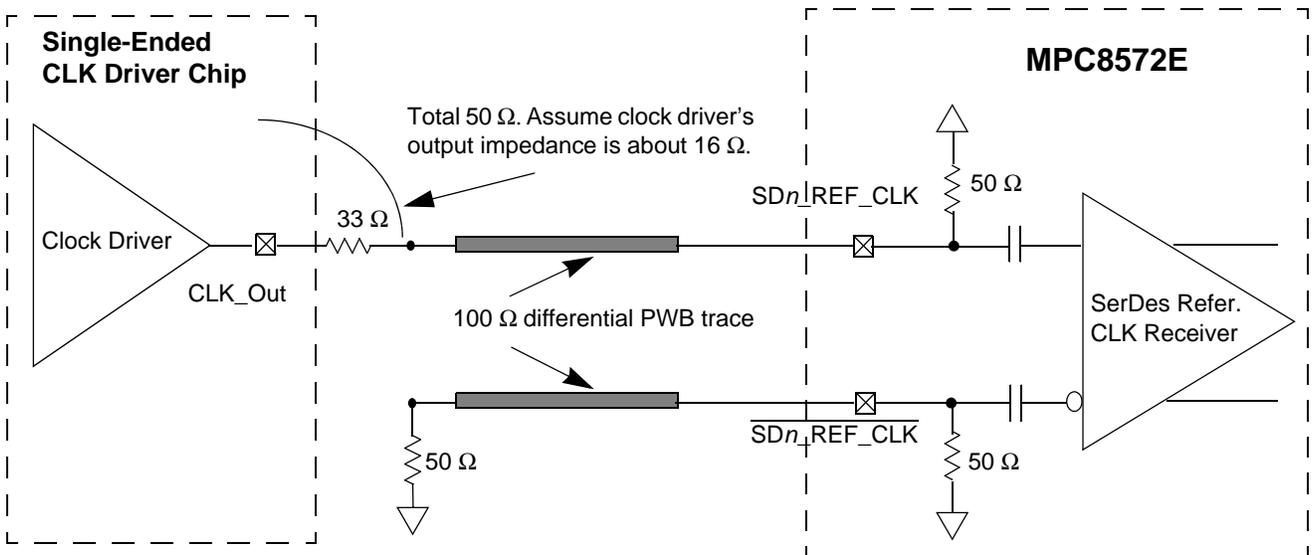


Figure 51. Single-Ended Connection (Reference Only)

### 15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

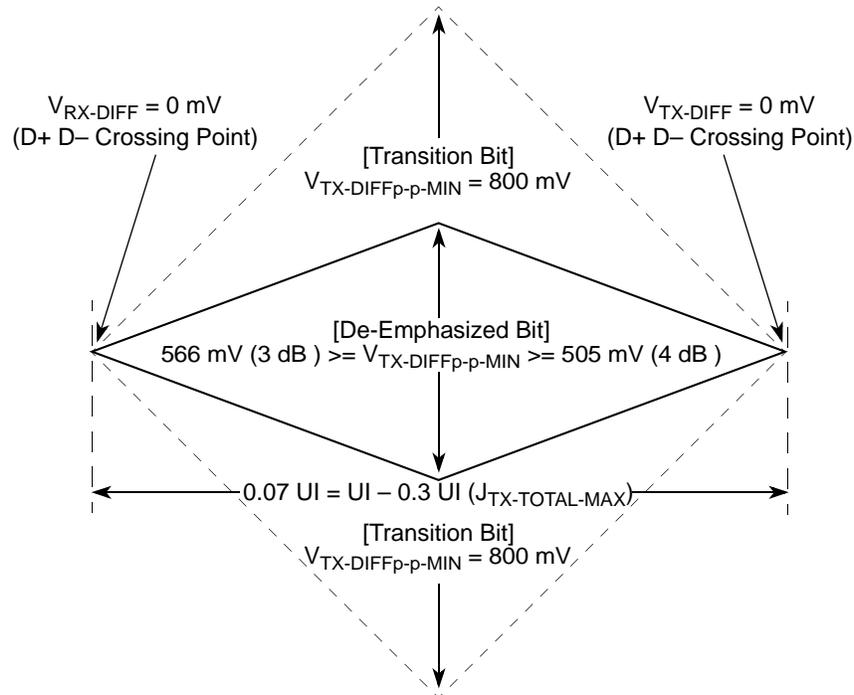


Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications

### 16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 63. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 *  V_{RX-D+} - V_{RX-D-} $ See Note 2.
$T_{RX-EYE}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

## 16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

### NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

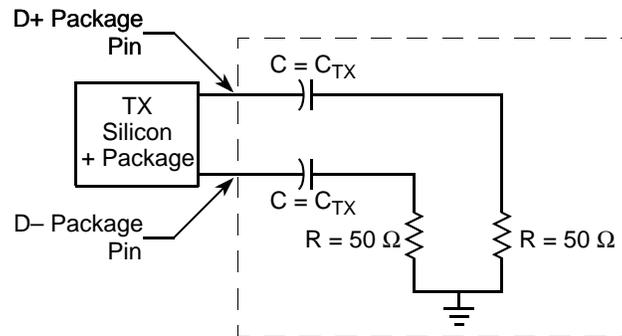


Figure 57. Compliance Test/Measurement Load

## 17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of  $\pm 100$  ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

**Table 72. Receiver AC Timing Specifications—1.25 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	$J_D$	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	$J_{DR}$	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance <sup>1</sup>	$J_T$	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	$S_{MI}$	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	$10^{-12}$	—	—
Unit Interval	UI	800	800	ps	+/- 100 ppm

**Note:**

- Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 59](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

**Table 73. Receiver AC Timing Specifications—2.5 GBaud**

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	$V_{IN}$	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	$J_D$	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	$J_{DR}$	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance <sup>1</sup>	$J_T$	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	$S_{MI}$	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	$10^{-12}$	—	—
Unit Interval	UI	400	400	ps	+/- 100 ppm

**Note:**

- Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 59](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	O	BV <sub>DD</sub>	5, 9
LGPL1/LFALE	UPM General Purpose Line 1 / Flash Address Latch Enable	J16	O	BV <sub>DD</sub>	5, 9
LGPL2/LOE/LFRE	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O	BV <sub>DD</sub>	5, 8, 9
LGPL3/LFWP	UPM General Purpose Line 3 / Flash Write Protect	K16	O	BV <sub>DD</sub>	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE /LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV <sub>DD</sub>	—
LGPL5	UPM General Purpose Line 5 / Amux	B26	O	BV <sub>DD</sub>	5, 9
LCLK[0:2]	Local Bus Clock	F17, F16, A23	O	BV <sub>DD</sub>	—
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV <sub>DD</sub>	—
LSYNC_OUT	Local Bus DLL Synchronization	A21	O	BV <sub>DD</sub>	—
<b>DMA</b>					
DMA1_DACK[0:1]	DMA Acknowledge	W25, U30	O	OV <sub>DD</sub>	21
DMA2_DACK[0]	DMA Acknowledge	AA26	O	OV <sub>DD</sub>	5, 9
DMA1_DREQ[0:1]	DMA Request	Y29, V27	I	OV <sub>DD</sub>	—
DMA2_DREQ[0]	DMA Request	V29	I	OV <sub>DD</sub>	—
DMA1_DDONE[0:1]	DMA Done	Y28, V30	O	OV <sub>DD</sub>	5, 9
DMA2_DDONE[0]	DMA Done	AA28	O	OV <sub>DD</sub>	5, 9
DMA2_DREQ[2]	DMA Request	M23	I	BV <sub>DD</sub>	—
<b>Programmable Interrupt Controller</b>					
UDE0	Unconditional Debug Event Processor 0	AC25	I	OV <sub>DD</sub>	—
UDE1	Unconditional Debug Event Processor 1	AA25	I	OV <sub>DD</sub>	—
MCP0	Machine Check Processor 0	M28	I	OV <sub>DD</sub>	—
MCP1	Machine Check Processor 1	L28	I	OV <sub>DD</sub>	—
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV <sub>DD</sub>	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
VDD	Core, L2, Logic Supply	L14, M13, M15, M17, N12, N14, N16, N20, N22, P11, P13, P15, P17, P19, P21, P23, R12, R14, R16, R18, R20, R22, T13, T15, T19, T21, T23, U12, U14, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA12, AA14, AA16, AA18, AA20, AB13	—	VDD	—
SVDD_SRDS1	SerDes Core 1 Logic Supply (xcorevdd)	C31, D29, E28, E32, F30, G28, G31, H29, K30, L31, M29, N32, P30	—	—	—
SVDD_SRDS2	SerDes Core 2 Logic Supply (xcorevdd)	AD32, AF31, AG29, AJ32, AK29, AK30	—	—	—
XVDD_SRDS1	SerDes1 Transceiver Supply (xpadvdd)	C26, D24, E27, F25, G26, H24, J27, K25, L26, M24, N27	—	—	—
XVDD_SRDS2	SerDes2 Transceiver Supply (xpadvdd)	AD24, AD28, AE26, AF25, AG27, AH24, AJ26	—	—	—
AVDD_LBIU	Local Bus PLL Supply	A19	—	—	19
AVDD_DDR	DDR PLL Supply	AM20	—	—	19
AVDD_CORE0	CPU PLL Supply	B18	—	—	19
AVDD_CORE1	CPU PLL Supply	A17	—	—	19
AVDD_PLAT	Platform PLL Supply	AB32	—	—	19
AVDD_SRDS1	SerDes1 PLL Supply	J29	—	—	19
AVDD_SRDS2	SerDes2 PLL Supply	AH29	—	—	19
SENSEVDD	VDD Sensing Pin	N18	—	—	13
SENSEVSS	GND Sensing Pin	P18	—	—	13
<b>Analog Signals</b>					
MVREF1	SSTL_1.8 Reference Voltage	C16	I	$GV_{DD}/2$	—
MVREF2	SSTL_1.8 Reference Voltage	AM19	I	$GV_{DD}/2$	—

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of  $\overline{\text{LWE}}[0]/\text{LBS}[0]/\text{LFWE}$ ,  $\text{UART\_SOUT}[1]$ , and  $\text{READY\_P1}$  signals at power up, as shown in Table 81.

**Table 81. e500 Core1 to CCB Clock Ratio**

Binary Value of $\overline{\text{LWE}}[0]/\text{LBS}[0]/\text{LFWE}$ , $\text{UART\_SOUT}[1]$ , $\text{READY\_P1}$ Signals	e500 Core1:CCB Clock Ratio	Binary Value of $\overline{\text{LWE}}[0]/\text{LBS}[0]/\text{LFWE}$ , $\text{UART\_SOUT}[1]$ , $\text{READY\_P1}$ Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

## 19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock,  $\text{DDRCLK}$ , which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

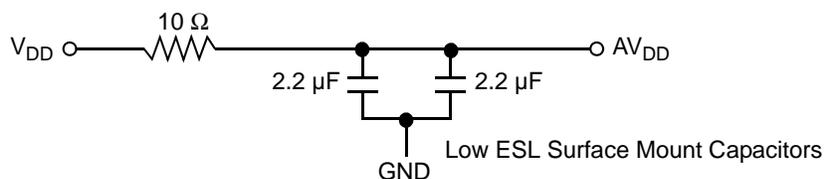
In asynchronous mode, the DDR PLL rate to  $\text{DDRCLK}$  ratios listed in Table 82 reflects the DDR data rate to  $\text{DDRCLK}$  ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input,  $\text{DDRCLK}$ , is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

**Table 82. DDR Clock Ratio**

Binary Value of $\text{TSEC\_1588\_CLK\_OUT}$ , $\text{TSEC\_1588\_PULSE\_OUT1}$ , $\text{TSEC\_1588\_PULSE\_OUT2}$ Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1

Figure 62 shows the PLL power supply filter circuits.

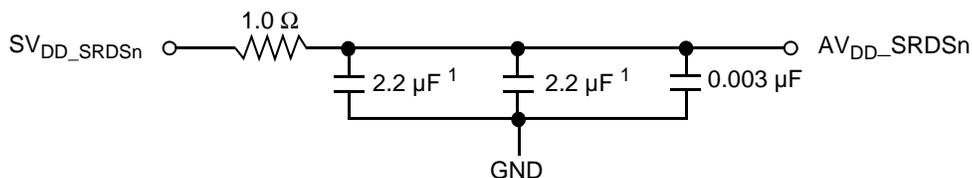


**Figure 62. PLL Power Supply Filter Circuit**

**NOTE**

It is recommended to have the minimum number of vias in the  $AV_{DD}$  trace for board layout. For example, zero vias might be possible if the  $AV_{DD}$  filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for  $AV_{DD}$  and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The  $AV_{DD\_SRDSn}$  signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the  $AV_{DD\_SRDSn}$  ball to ensure it filters out as much noise as possible. The ground connection should be near the  $AV_{DD\_SRDSn}$  ball. The 0.003- $\mu$ F capacitor is closest to the ball, followed by the two 2.2  $\mu$ F capacitors, and finally the 1  $\Omega$  resistor to the board supply plane. The capacitors are connected from  $AV_{DD\_SRDSn}$  to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 63. SerDes PLL Power Supply Filter**

**NOTE**

$AV_{DD\_SRDSn}$  should be a filtered version of  $SV_{DD\_SRDSn}$ .

**NOTE**

Signals on the SerDes interface are fed from the  $XV_{DD\_SRDSn}$  power plane.

### 21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ ,  $105^{\circ}\text{C}$ .

**Table 85. Impedance Characteristics**

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
$R_N$	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	$Z_0$	$\Omega$
$R_P$	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	$Z_0$	$\Omega$

Note: Nominal supply voltages. See Table 1,  $T_j = 105^{\circ}\text{C}$ .

## 21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of  $4.7\text{ k}\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately  $20\text{ k}\Omega$ . This value should permit the  $4.7\text{-k}\Omega$  resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform /system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 21.9 JTAG Configuration Signals

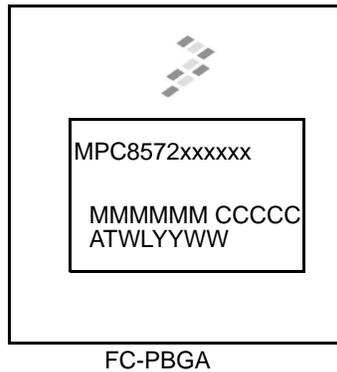
Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The  $\overline{\text{TRST}}$  signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires  $\overline{\text{TRST}}$  to be asserted during power-on reset flow to ensure that the JTAG boundary

<sup>3</sup> Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

## 22.2 Part Marking

Parts are marked as the example shown in [Figure 67](#).



**Notes:**

MMMMMM is the 6-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 67. Part Marking for FC-PBGA Device**

[Table 89](#) explains line four of [Figure 67](#).

**Table 89. Meaning of Last Line of Part Marking**

Digit	Description
A	Assembly Site E Oak Hill Q KLM
WL	Lot number
YY	Year assembled
WW	Work week assembled

## 23 Document Revision History

[Table 90](#) provides a revision history for the MPC8572E hardware specification.

**Table 90. Document Revision History**

Rev. Number	Date	Substantive Change(s)
7	03/2016	<ul style="list-style-type: none"> <li>Updated <a href="#">Section 22.2, "Part Marking,"</a> changed the five-digit mask number to six digits.</li> </ul>

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