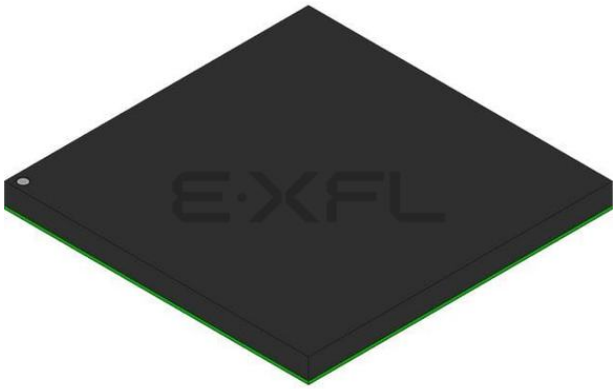

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572evtavne

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Range	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface	—	–0.3 to 1.65		—
Three-speed Ethernet I/O, FEC management interface, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2) TV_{DD} (for eTSEC3 and eTSEC4, FEC)	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 3.63 –0.3 to 2.75	V — —	2 2
DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus and GPIO I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 and DDR3 SDRAM interface reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus and GPIO signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3V ± 5% or 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TV_{DD}=2.5V L/TV_{DD}=3.3V	t_{G125R}, t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD}=2.5V, and from 0.6V and 2.7V for L/TV_{DD}=3.3V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

Table 8. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	100	MHz	1
DDRCLK cycle time	t_{DDRCLK}	10.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	3

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to $MV_{REF}n$. This rail should track variations in the DC level of $MV_{REF}n$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	µA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.175 V.

Table 14 provides the current draw characteristics for $MV_{REF}n$.

Table 14. Current Draw Characteristics for MV_{REF} *n*

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	$I_{MVREF}n$	—	1500	µA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	>=667 MHz	V_{ILAC}	—	$MV_{REF}n$ – 0.20	V	—
	<= 533 MHz		—	$MV_{REF}n$ – 0.25		
AC input high voltage	>=667 MHz	V_{IHAC}	$MV_{REF}n$ + 0.20	—	V	—
—	<= 533 MHz		$MV_{REF}n$ + 0.25	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REF}n$ – 0.175	V	—
AC input high voltage	V_{IHAC}	$MV_{REF}n$ + 0.175	—	V	—

Table 38. SGMII DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Change in V_{OS} between "0" and "1"	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ}$=1.1 V.
2. $|V_{OD}| = |V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of MPC8572E's SerDes 2 Control Register:
   - •The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - •The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
   - 5.The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.1V, no common mode offset variation (V_{OS} =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and $\overline{SD2\_TX}$[n].

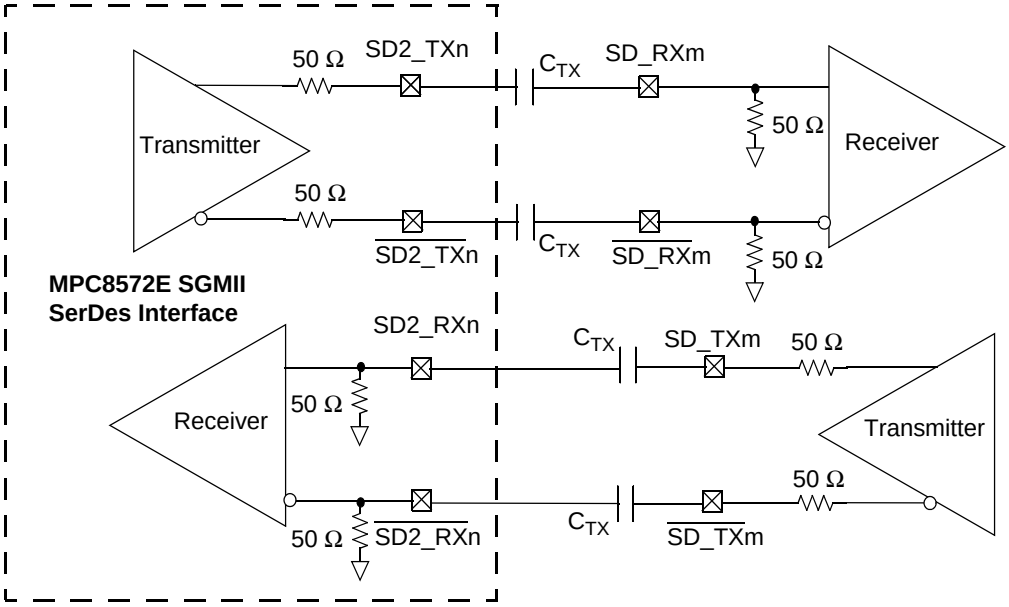


Figure 22. 4-Wire AC-Coupled SGMII Serial Link Connection Example

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Notes:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

6. Differential Waveform

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = $(V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2$ = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

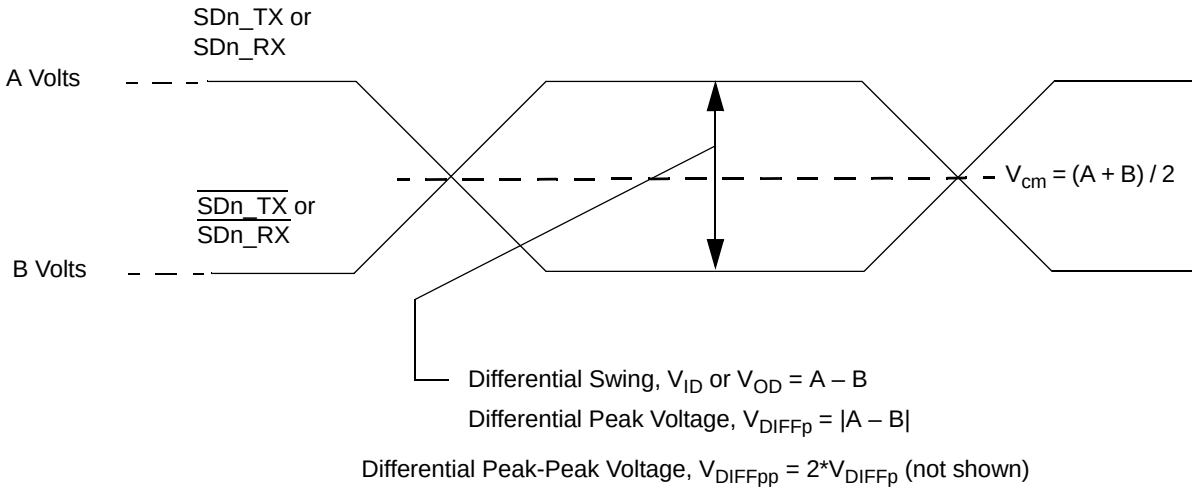


Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.

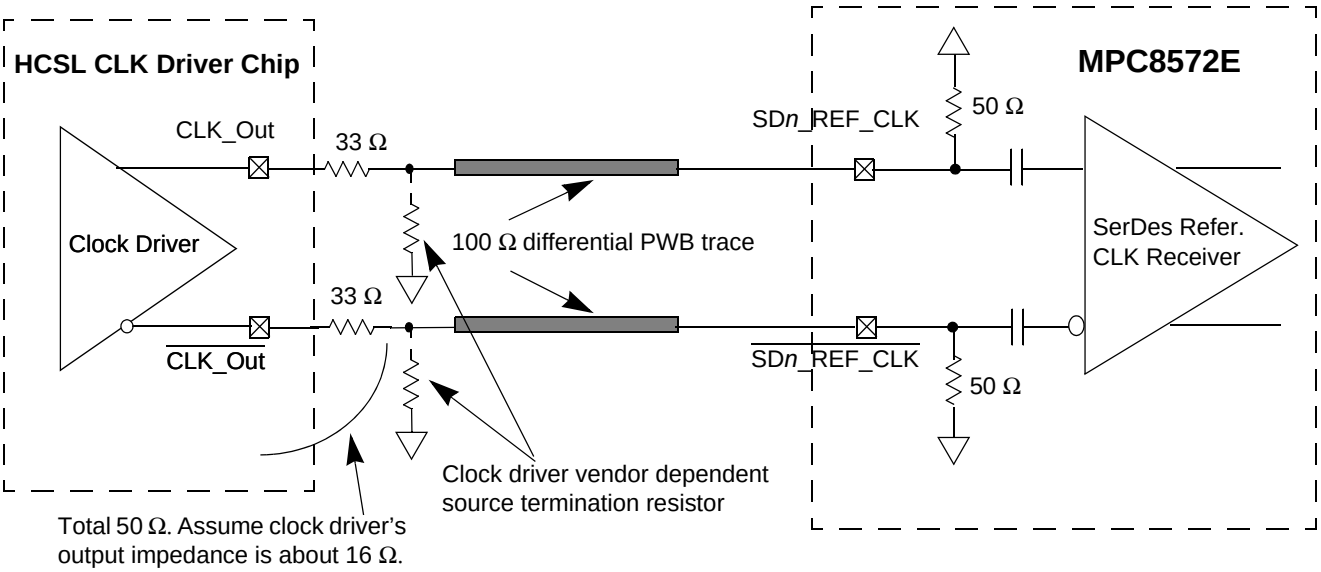


Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 57) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 56) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

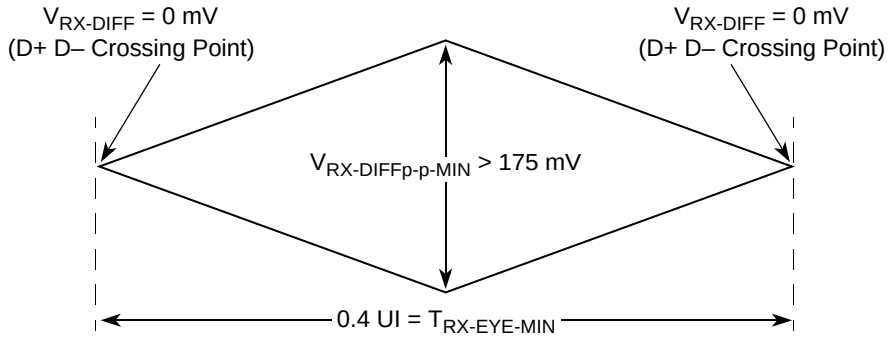


Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

17.5 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 65. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 69. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 70. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 58 with the parameters specified in Figure 71 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Ball Pitch	1 mm
Ball Diameter (Typical)	0.6 mm
Solder Balls	63% Sn
	37% Pb
Solder Balls (Lead-Free)	96.5% Sn
	3.5% Ag

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_GTX_CLK	Transmit Clock Out	AE17	O	TV_{DD}	
TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK	Receive Clock	AF17	I	TV_{DD}	1
TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV	Receive Data Valid	AG14	I	TV_{DD}	1
TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER	Receive Error	AH15	I	TV_{DD}	1
TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK	Transmit Clock In	AF16	I	TV_{DD}	1
TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN	Transmit Enable	AJ18	O	TV_{DD}	1, 22
Three-Speed Ethernet Controller 4					
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4]	Transmit Data	AD15, AC16, AC14, AB16	O	TV_{DD}	1, 5, 9
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4]	Receive Data	AE15, AF13, AE14, AH14	I	TV_{DD}	1
TSEC4_GTX_CLK	Transmit Clock Out	AB14	O	TV_{DD}	—
TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC	Receive Clock	AG13	I	TV_{DD}	1
TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC	Receive Data Valid	AD13	I/O	TV_{DD}	1, 23
TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER	Transmit Enable	AB15	O	TV_{DD}	1, 22
DUART					
$\overline{\text{UART\_CTS}}$[0:1]	Clear to Send	W30, Y27	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	Ready to Send	W31, Y30	O	OV_{DD}	5, 9
UART_SIN[0:1]	Receive Data	Y26, W29	I	OV_{DD}	—
UART_SOUT[0:1]	Transmit Data	Y25, W26	O	OV_{DD}	5, 9
I^2C Interface					
IIC1_SCL	Serial Clock	AC30	I/O	OV_{DD}	4, 20
IIC1_SDA	Serial Data	AB30	I/O	OV_{DD}	4, 20
IIC2_SCL	Serial Clock	AD30	I/O	OV_{DD}	4, 20
IIC2_SDA	Serial Data	AD29	I/O	OV_{DD}	4, 20
SerDes (x10) PCIe, SRIO					

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_RX[7:0]	Receive Data (positive)	P32, N30, M32, L30, G30, F32, E30, D32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_RX}}$[7:0]	Receive Data (negative)	P31, N29, M31, L29, G29, F31, E29, D31	I	XV_{DD_SRDS1}	—
SD1_TX[7]	PCIe1 Tx Data Lane 7 / SRIO or PCIe2 Tx Data Lane 3 / PCIe3 TX Data Lane 1	M26	O	XV_{DD_SRDS1}	—
SD1_TX[6]	PCIe1 Tx Data Lane 6 / SRIO or PCIe2 Tx Data Lane 2 / PCIe3 TX Data Lane 0	L24	O	XV_{DD_SRDS1}	—
SD1_TX[5]	PCIe1 Tx Data Lane 5 / SRIO or PCIe2 Tx Data Lane 1	K26	O	XV_{DD_SRDS1}	—
SD1_TX[4]	PCIe1 Tx Data Lane 4 / SRIO or PCIe2 Tx Data Lane 0	J24	O	XV_{DD_SRDS1}	—
SD1_TX[3]	PCIe1 Tx Data Lane 3	G24	O	XV_{DD_SRDS1}	—
SD1_TX[2]	PCIe1 Tx Data Lane 2	F26	O	XV_{DD_SRDS1}	—
SD1_TX[1]	PCIe1 Tx Data Lane 1]	E24	O	XV_{DD_SRDS1}	—
SD1_TX[0]	PCIe1 Tx Data Lane 0	D26	O	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_TX}}$[7:0]	Transmit Data (negative)	M27, L25, K27, J25, G25, F27, E25, D27	O	XV_{DD_SRDS1}	—
SD1_PLL_TPD	PLL Test Point Digital	J32	O	XV_{DD_SRDS1}	17
SD1_REF_CLK	PLL Reference Clock	H32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference Clock Complement	H31	I	XV_{DD_SRDS1}	—
Reserved	—	C29, K32	—	—	26
Reserved	—	C30, K31	—	—	27
Reserved	—	C24, C25, H26, H27	—	—	28
Reserved	—	AL20, AL21	—	—	29
SerDes (x4) SGMII					
SD2_RX[3:0]	Receive Data (positive)	AK32, AJ30, AF30, AE32	I	XV_{DD_SRDS2}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS1	SerDes Transceiver Core Logic GND (xcorevss)	C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32	—	—	—
SGND_SRDS2	SerDes Transceiver Core Logic GND (xcorevss)	AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32	—	—	—
AGND_SRDS1	SerDes PLL GND	J31	—	—	—
AGND_SRDS2	SerDes PLL GND	AH31	—	—	—
OVDD	General I/O Supply	U31, V24, V28, Y31, AA27, AB25, AB29	—	OVDD	—
LVDD	TSEC 1&2 I/O Supply	AC18, AC21, AG21, AL27	—	LVDD	—
TVDD	TSEC 3&4 I/O Supply	AC15, AE16, AH18	—	TVDD	—
GVDD	SSTL_1.8 DDR Supply	B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2	—	GVDD	—
BVDD	Local Bus and GPIO Supply	A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20	—	BVDD	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω (±1%) to GND	—
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	O	AVDD_SRDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	I	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	I	100Ω (±1%) to GND	—
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	O	AVDD_SRDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	—	internal diode	14
No Connection Pins					

Table 78. Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn\_MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in Table 80 and Table 81;
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from Table 79;
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 82. Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 79:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

Figure 62 shows the PLL power supply filter circuits.

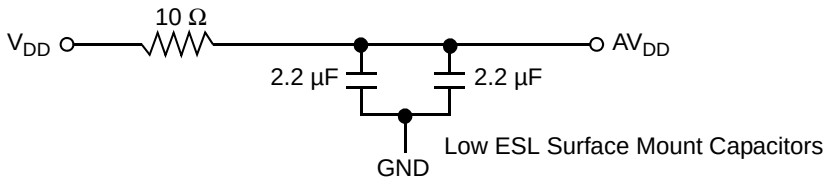
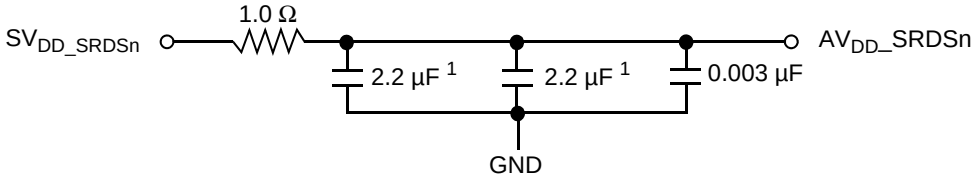


Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD}_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

AV_{DD}_SRDSn should be a filtered version of SV_{DD}_SRDS*n*.

NOTE

Signals on the SerDesn interface are fed from the XV_{DD}_SRDS*n* power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.