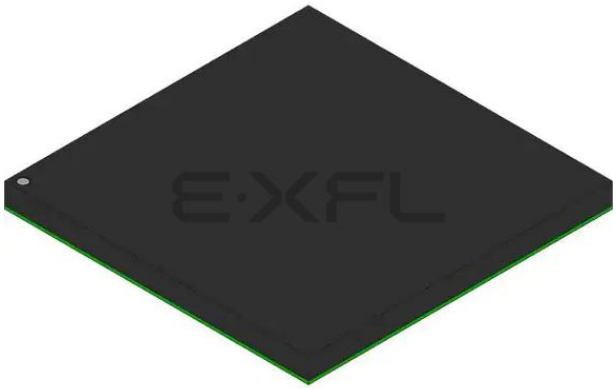

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Number of Cores/Bus Width | - |
| Speed | - |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | - |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | - |
| Operating Temperature | - |
| Security Features | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572lvjavne |

- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing.
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
- Interrupt summary registers allow fast identification of interrupt source.

- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, SSL/TLS, SRTP, 802.16e, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 4096 bits
    - Elliptic curve cryptography with $F_2m$ and F(p) modes and programmable field size up to 1023 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB, CBC and OFB-64 modes for both DES and 3DES
  - AESU—Advanced Encryption Standard unit
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, CTR, CCM, GCM, CMAC, OFB-128, CFB-128, and LRW modes
    - 128-, 192-, and 256-bit key lengths
  - AFEU—ARC four execution unit
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - MDEU—message digest execution unit
    - SHA-1 with 160-bit message digest
    - SHA-2 (SHA-256, SHA-384, SHA-512)
    - MD5 with 128-bit message digest
    - HMAC with all algorithms
  - KEU—Kasumi execution unit
    - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
    - Also supports A5/3 and GEA-3 algorithms
  - RNG—random number generator
  - XOR engine for parity checking in RAID storage applications
  - CRC execution unit
    - CRC-32 and CRC-32C
- Pattern Matching Engine with DEFLATE decompression

  - Regular expression (regex) pattern matching
    - Built-in case insensitivity, wildcard support, no pattern explosion
    - Cross-packet pattern detection
    - Fast pattern database compilation and fast incremental updates
    - 16000 patterns, each up to 128 bytes in length
    - Patterns can be split into 256 sets, each of which can contain 16 subsets
  - Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
    - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
    - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
    - 8192 stateful rules
  - Deflate engine
    - Supports decompression of DEFLATE compression format including zlib and gzip
    - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)
- Two Table Lookup Units (TLU)
  - Hardware-based lookup engine offloads table searches from e500 cores
  - Longest prefix match, exact match, chained hash, and flat data table formats
  - Up to 32 tables, with each table up to 16M entries
  - 32-, 64-, 96-, or 128-bit keys
- Two $I^2C$ controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Enhanced local bus controller (eLBC)

Figure 16 shows the TBI receive AC timing diagram.

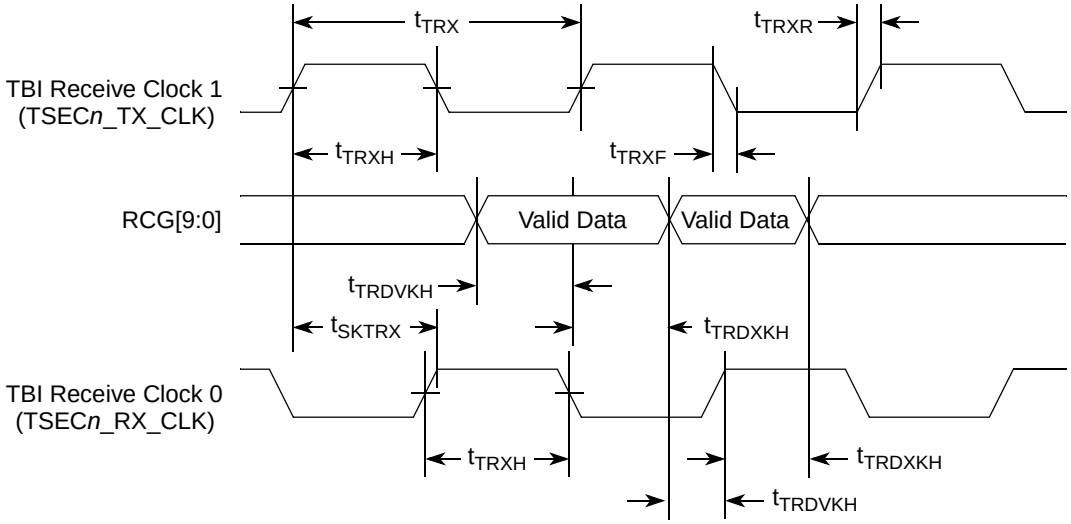



**Figure 16. TBI Receive AC Timing Diagram**

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

**Table 33. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRRX}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRRX}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

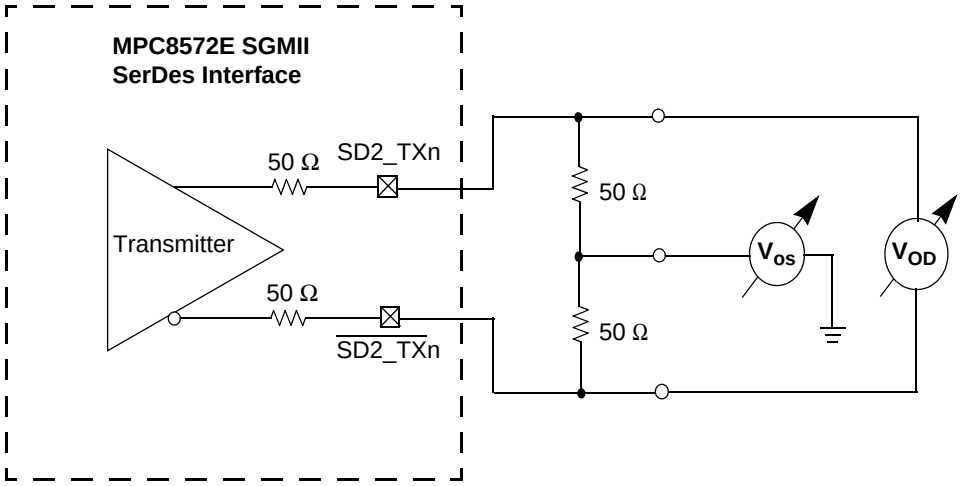



**Figure 23. SGMII Transmitter DC Measurement Circuit**

Table 39 lists the SGMII DC receiver electrical characteristics.

**Table 39. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX\_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM\_ACp-p}$ | | — | 100 | mV | 5 |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | | $Z_{RX\_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of MPC8572E's SerDes 2 Control Register.
5. $V_{CM\_ACp-p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

**Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | $t_{T1588OV}$ | 0.5 | — | 3.0 | ns | — |
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | $2*t_{T1588CLK\_MAX}$ | — | — | ns | 2 |

**Note:**

1. When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of $t_{T1588CLK}$ is defined in terms of $T_{TX\_CLK}$, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the $T_{TX\_CLK}$ is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.
2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

## 9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

**Table 43. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=3.3 V)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $LV_{DD}/TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | $OV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ =Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($LV_{DD}/TV_{DD}$ = Max, $V_{IN}$ [3] = 2.1 V) | $I_{IH}$ | — | 40 | µA | — |

**Table 45. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| ECn_MDIO to ECn_MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |
| ECn_MDIO to ECn_MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| ECn_MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | 4 |
| ECn_MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | 4 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency ($f_{CCB}$). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC}$ = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency ($f_{CCB}$), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
4. Guaranteed by design.
5. $t_{plb\_clk}$ is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.

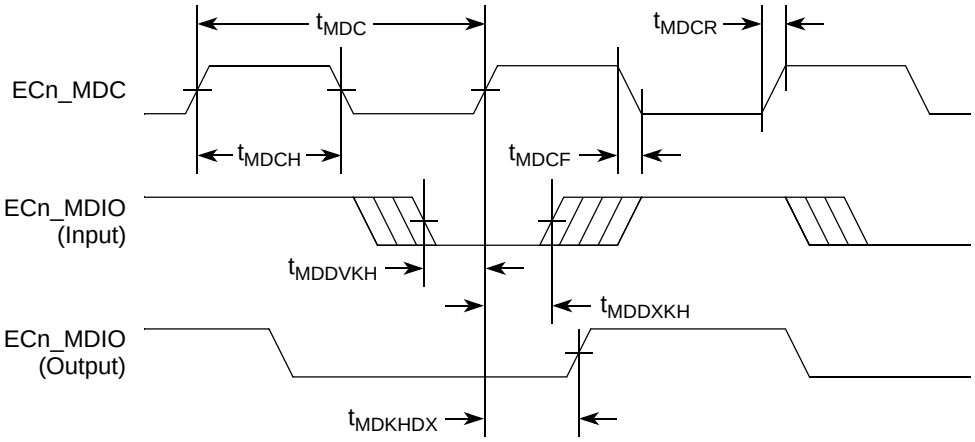



**Figure 28. MII Management Interface Timing Diagram**

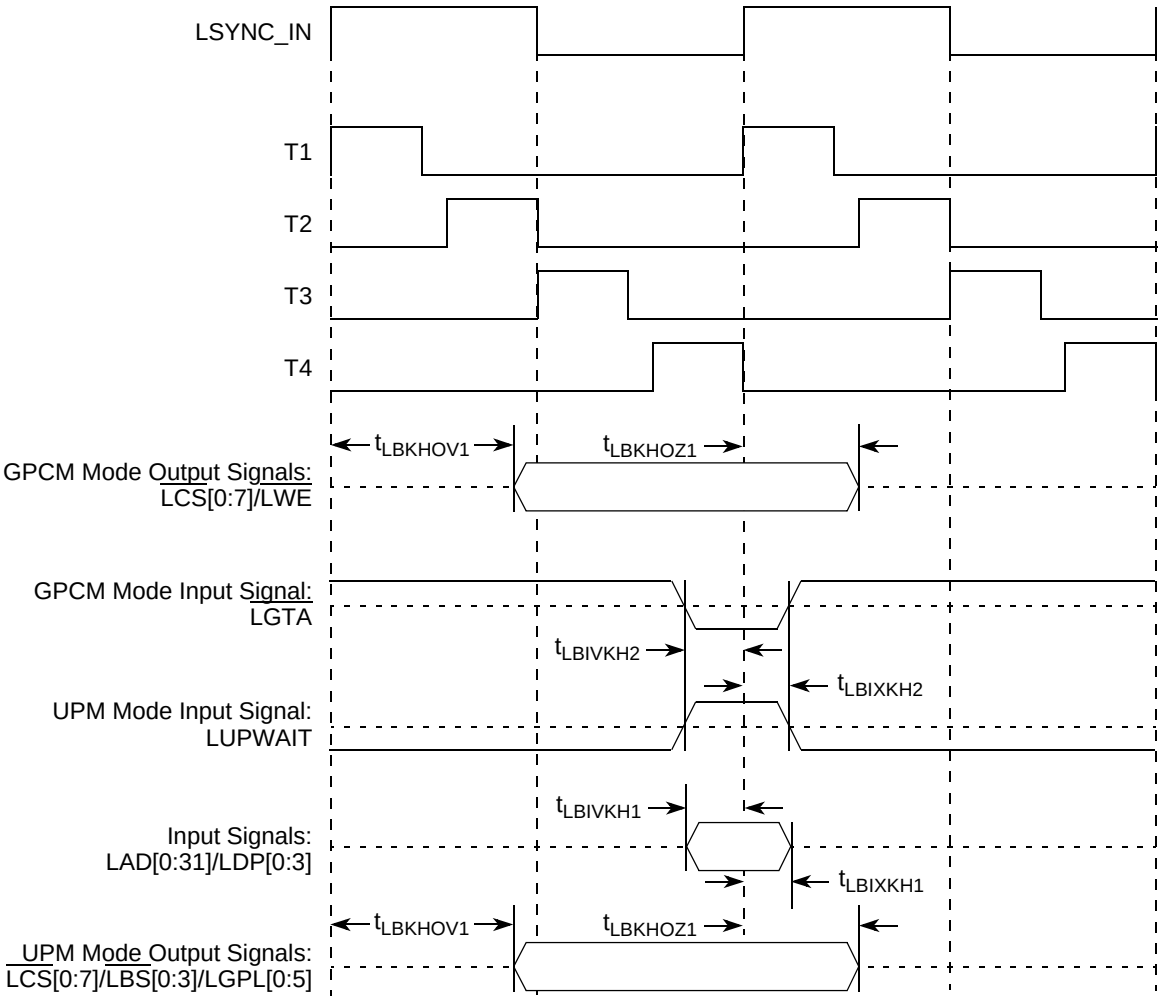



**Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)**

**Table 54. I²C DC Electrical Characteristics (continued)**

| | | | | | |
|---|---|---|---|---|---|
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 13.2 I²C AC Electrical Specifications

Table 55 provides the AC timing parameters for the I²C interfaces.

**Table 55. I²C AC Electrical Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%. All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 2).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz[4] |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | µs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | µs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | µs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | µs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data input hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>— | µs |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9[3] | µs |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | µs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |

**Table 55. I²C AC Electrical Specifications (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%. All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 2).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Capacitive load for each bus line | Cb | — | 400 | pF |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8572E provides a delay time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8572E acts as the I2C bus master while transmitting, the MPC8572E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8572E would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8572E as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum $t_{I2OVKL}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*.

Figure 40 provides the AC test load for the I²C.

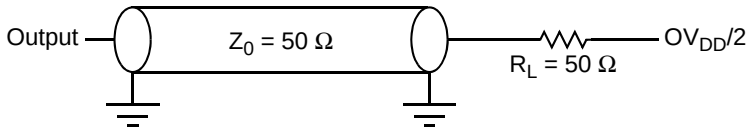



**Figure 40. I²C AC Test Load**

Figure 41 shows the AC timing diagram for the I²C bus.

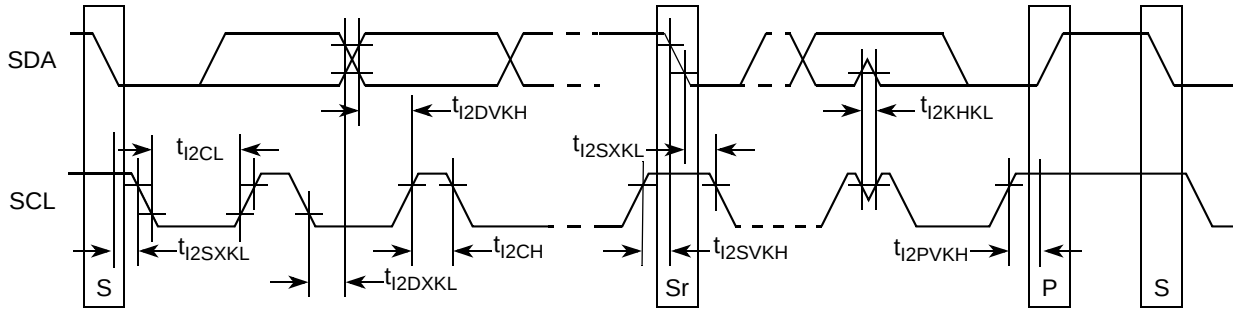



**Figure 41. I²C Bus AC Timing Diagram**

# 15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The $V_{OD}$ value can be either positive or negative.

3. **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The $V_{ID}$ value can be either positive or negative.

4. **Differential Peak Voltage, $V_{DIFFp}$**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

**6. Differential Waveform**

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, $V_{cm}$

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out}$ = $(V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2$ = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

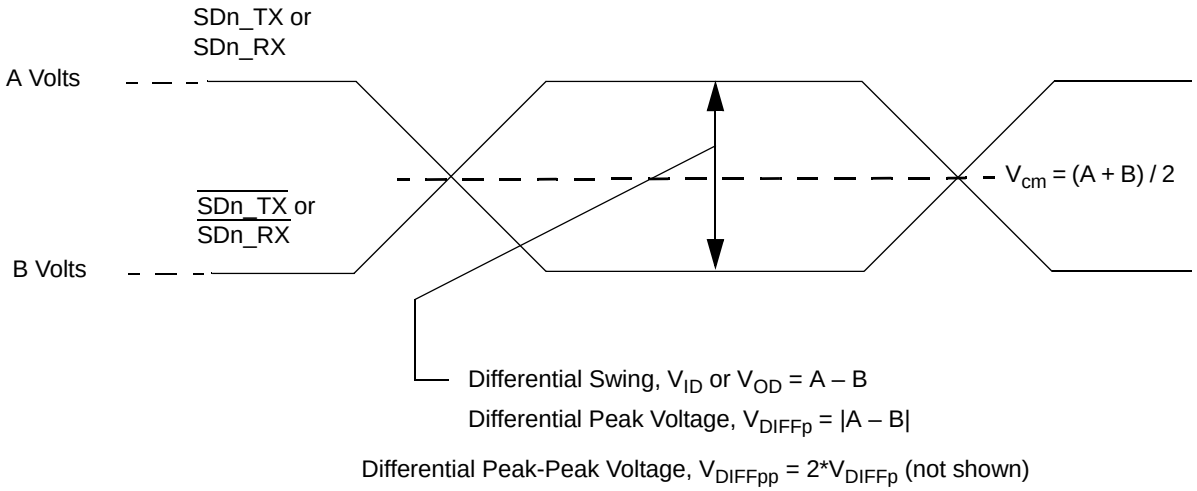



**Figure 43. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

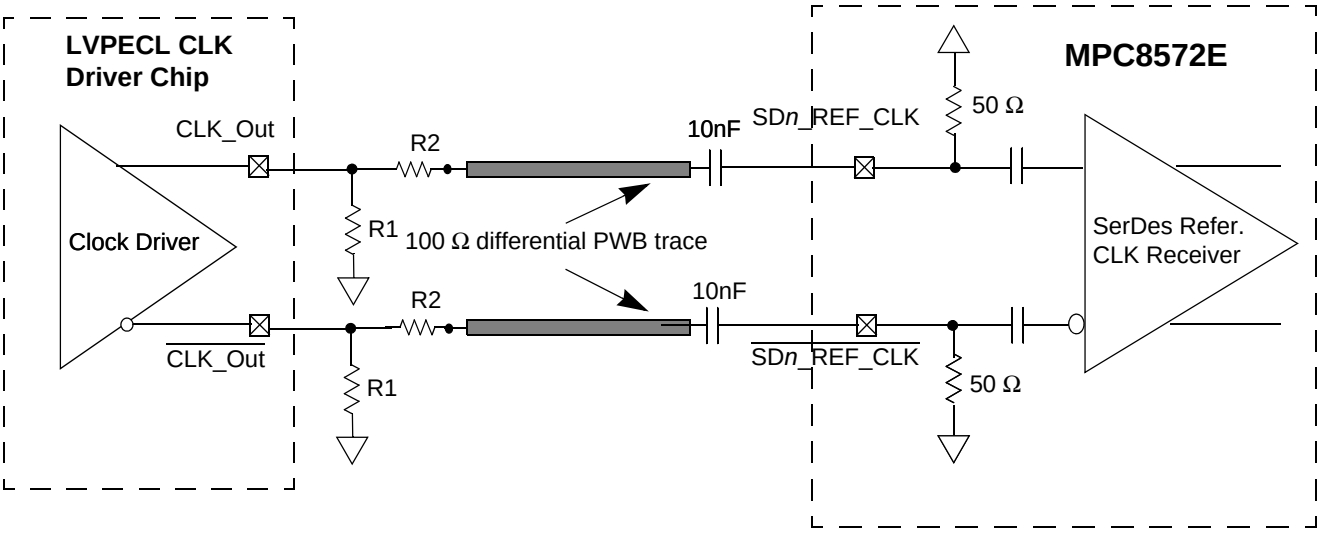



**Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

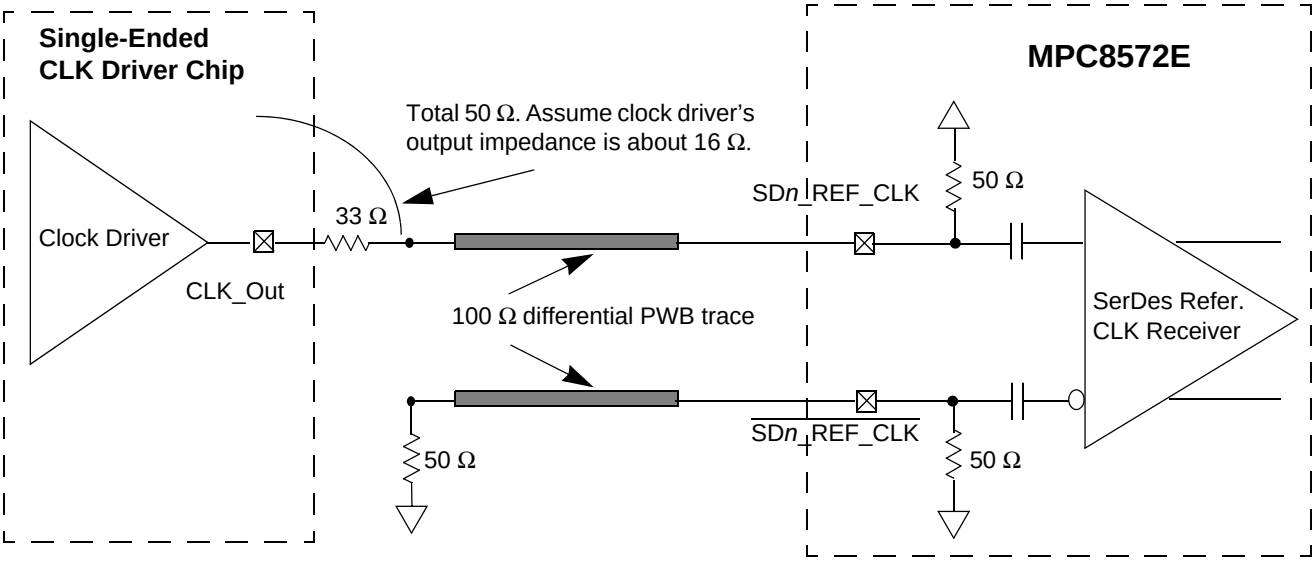



**Figure 51. Single-Ended Connection (Reference Only)**

## 15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

- Section 17, “Serial RapidIO”

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

# 16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

## 16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

## 16.2 AC Requirements for PCI Express SerDes Reference Clocks

Table 61 lists AC requirements.

**Table 61. SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | — |

**Notes:**
1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

## 16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

## 16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

### 16.4.1 Differential Transmitter (TX) Output

Table 62 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 62. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{TX-DIFFp-p}$ | Differential Peak-to-Peak Output Voltage | 0.8 | — | 1.2 | V | $V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2. |
| $V_{TX-DE-RATIO}$ | De- Emphasized Differential Output Voltage (Ratio) | –3.0 | –3.5 | -4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2. |
| $T_{TX-EYE}$ | Minimum TX Eye Width | 0.70 | — | — | UI | The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3. |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| $T_{TX-RISE}$, $T_{TX-FALL}$ | D+/D- TX Output Rise/Fall Time | 0.125 | — | — | UI | See Notes 2 and 5 |
| $V_{TX-CM-ACp}$ | RMS AC Peak Common Mode Output Voltage | — | — | 20 | mV | $V_{TX-CM-ACp} = RMS(\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC})$<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$<br>See Note 2 |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | 0 | — | 100 | mV | $\|V_{TX-CM-DC\ (during\ L0)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\| <= 100$ mV<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [L0]<br>$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [Electrical Idle]<br>See Note 2. |
| $V_{TX-CM-DC-LINE-DELTA}$ | Absolute Delta of DC Common Mode between D+ and D– | 0 | — | 25 | mV | $\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| <= 25$ mV<br>$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$<br>$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$<br>See Note 2. |
| $V_{TX-IDLE-DIFFp}$ | Electrical Idle differential Peak Output Voltage | 0 | — | 20 | mV | $V_{TX-IDLE-DIFFp} = \|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\| <= 20$ mV<br>See Note 2. |
| $V_{TX-RCV-DETECT}$ | The amount of voltage change allowed during Receiver Detection | | — | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6. |

**Table 63. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7. |
| $V_{RX-CM-ACp}$ | AC Peak Common Mode Input Voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$<br>$V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$<br>See Note 2 |
| $RL_{RX-DIFF}$ | Differential Return Loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.<br>See Note 4 |
| $RL_{RX-CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4 |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC Differential mode impedance. See Note 5 |
| $Z_{RX-DC}$ | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 200 k | — | — | Ω | Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$<br>Measured at the package pins of the Receiver |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms | An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |

## 18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Package outline | 33 mm × 33 mm |
| Interconnects | 1023 |
| Ball Pitch | 1 mm |
| Ball Diameter (Typical) | 0.6 mm |
| Solder Balls | 63% Sn |
| | 37% Pb |
| Solder Balls (Lead-Free) | 96.5% Sn |
| | 3.5% Ag |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC3_GTX_CLK | Transmit Clock Out | AE17 | O | $TV_{DD}$ | |
| TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK | Receive Clock | AF17 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV | Receive Data Valid | AG14 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER | Receive Error | AH15 | I | $TV_{DD}$ | 1 |
| TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK | Transmit Clock In | AF16 | I | $TV_{DD}$ | 1 |
| TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN | Transmit Enable | AJ18 | O | $TV_{DD}$ | 1, 22 |
| **Three-Speed Ethernet Controller 4** | | | | | |
| TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4] | Transmit Data | AD15, AC16, AC14, AB16 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4] | Receive Data | AE15, AF13, AE14, AH14 | I | $TV_{DD}$ | 1 |
| TSEC4_GTX_CLK | Transmit Clock Out | AB14 | O | $TV_{DD}$ | — |
| TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC | Receive Clock | AG13 | I | $TV_{DD}$ | 1 |
| TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC | Receive Data Valid | AD13 | I/O | $TV_{DD}$ | 1, 23 |
| TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER | Transmit Enable | AB15 | O | $TV_{DD}$ | 1, 22 |
| **DUART** | | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | Clear to Send | W30, Y27 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | Ready to Send | W31, Y30 | O | $OV_{DD}$ | 5, 9 |
| UART_SIN[0:1] | Receive Data | Y26, W29 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | Transmit Data | Y25, W26 | O | $OV_{DD}$ | 5, 9 |
| **$I^2C$ Interface** | | | | | |
| IIC1_SCL | Serial Clock | AC30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC1_SDA | Serial Data | AB30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SCL | Serial Clock | AD30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SDA | Serial Data | AD29 | I/O | $OV_{DD}$ | 4, 20 |
| **SerDes (x10) PCIe, SRIO** | | | | | |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| VDD | Core, L2, Logic Supply | L14, M13, M15, M17, N12, N14, N16, N20, N22, P11, P13, P15, P17, P19, P21, P23, R12, R14, R16, R18, R20, R22, T13, T15, T19, T21, T23, U12, U14, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA12, AA14, AA16, AA18, AA20, AB13 | — | VDD | — |
| SVDD_SRDS1 | SerDes Core 1 Logic Supply (xcorevdd) | C31, D29, E28, E32, F30, G28, G31, H29, K30, L31, M29, N32, P30 | — | — | — |
| SVDD_SRDS2 | SerDes Core 2 Logic Supply (xcorevdd) | AD32, AF31, AG29, AJ32, AK29, AK30 | — | — | — |
| XVDD_SRDS1 | SerDes1 Transceiver Supply (xpadvdd) | C26, D24, E27, F25, G26, H24, J27, K25, L26, M24, N27 | — | — | — |
| XVDD_SRDS2 | SerDes2 Transceiver Supply (xpadvdd) | AD24, AD28, AE26, AF25, AG27, AH24, AJ26 | — | — | — |
| AVDD_LBIU | Local Bus PLL Supply | A19 | — | — | 19 |
| AVDD_DDR | DDR PLL Supply | AM20 | — | — | 19 |
| AVDD_CORE0 | CPU PLL Supply | B18 | — | — | 19 |
| AVDD_CORE1 | CPU PLL Supply | A17 | — | — | 19 |
| AVDD_PLAT | Platform PLL Supply | AB32 | — | — | 19 |
| AVDD_SRDS1 | SerDes1 PLL Supply | J29 | — | — | 19 |
| AVDD_SRDS2 | SerDes2 PLL Supply | AH29 | — | — | 19 |
| SENSEVDD | VDD Sensing Pin | N18 | — | — | 13 |
| SENSEVSS | GND Sensing Pin | P18 | — | — | 13 |
| **Analog Signals** | | | | | |
| MVREF1 | SSTL_1.8 Reference Voltage | C16 | I | $GV_{DD}/2$ | — |
| MVREF2 | SSTL_1.8 Reference Voltage | AM19 | I | $GV_{DD}/2$ | — |

in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

See Section 20.4, "1x/4x LP-Serial Signal Descriptions," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

# 20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, 1023 33 × 33 FC-PBGA.

The package uses a 29.6 × 29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

**Table 84. Package Thermal Characteristics**

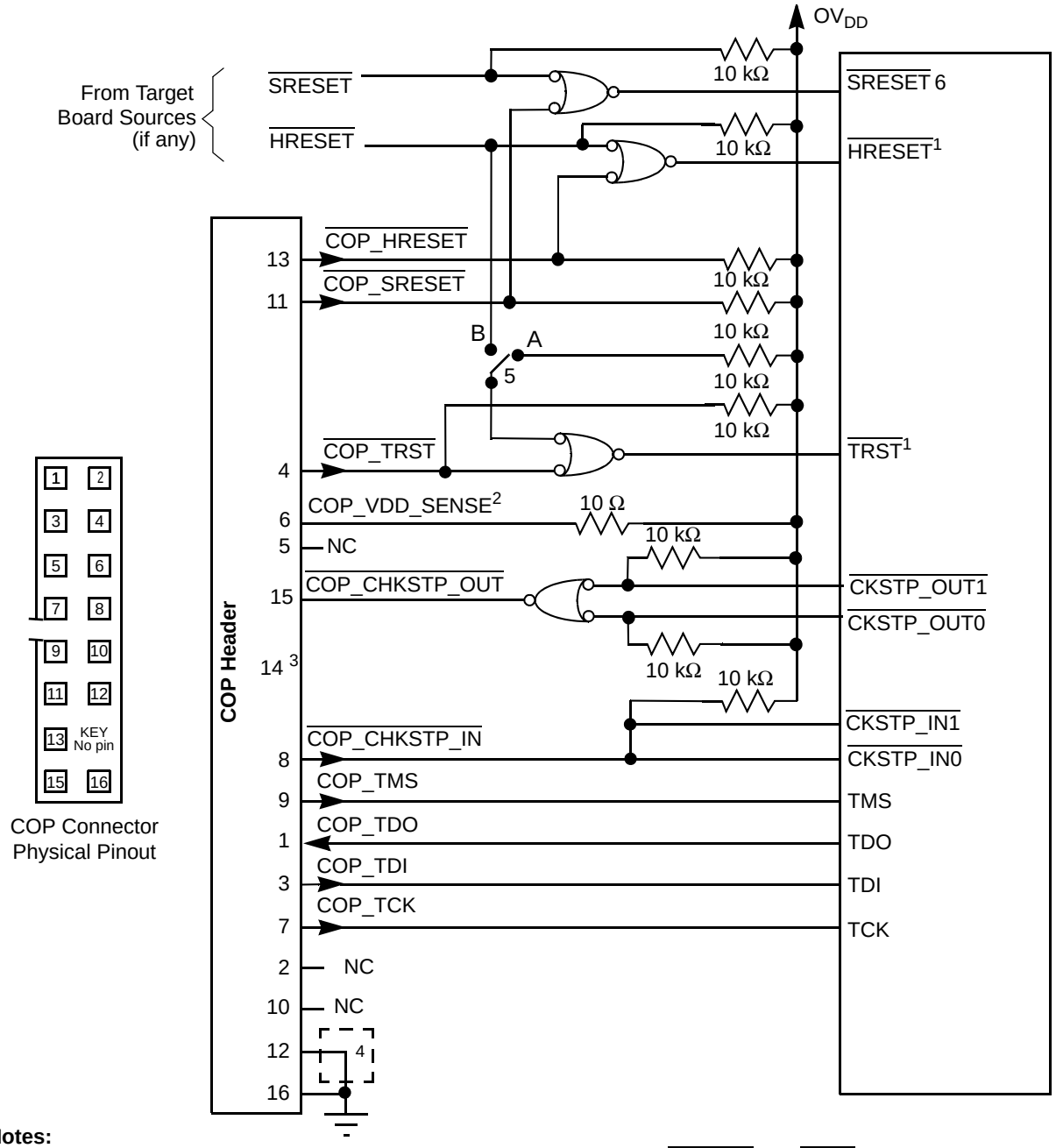
| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Single-layer (1s) | $R_{\Theta JA}$ | 15 | °C/W | 1, 2 |
| Junction to ambient, natural convection | Four-layer (2s2p) | $R_{\Theta JA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (at 200 ft./min.) | Single-layer (1s) | $R_{\Theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (ar 200 ft./min.) | Four-layer (2s2p) | $R_{\Theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction to board | — | $R_{\Theta JB}$ | 4 | °C/W | 4 |
| Junction to case | — | $R_{\Theta JC}$ | 0.5 | °C/W | 5 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

## 20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 cores.