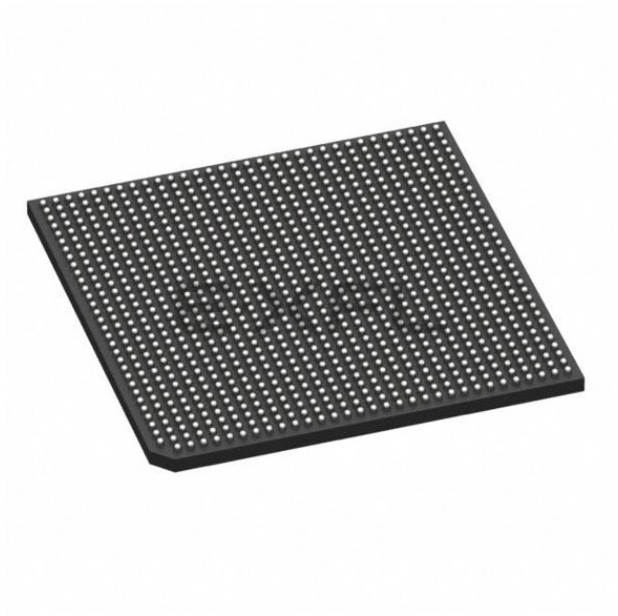

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572lvtatld

  - Three inbound windows plus a configuration window on PCI Express
  - Four inbound windows plus a default window on Serial RapidIO®
  - Four outbound windows plus default translation for PCI Express
  - Eight outbound windows plus default translation for Serial RapidIO with segmentation and sub-segmentation support

- Two 64-bit DDR2/DDR3 memory controllers
  - Programmable timing supporting DDR2 and DDR3 SDRAM
  - 64-bit data interface per controller
  - Four banks of memory supported, each up to 4 Gbytes, for a maximum of 16 Gbytes per controller
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Full ECC support
  - Page mode support
    - Up to 32 simultaneous open pages for DDR2 or DDR3
  - Contiguous or discontiguous memory mapping
  - Cache line, page, bank, and super-bank interleaving between memory controllers
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support when using DDR2 or DDR3
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access through JTAG port
  - 1.8-V SSTL_1.8 compatible I/O
  - Support 1.5-V operation for DDR3. The detail is TBD pending on official release of appropriate industry specifications.
  - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts per processor with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters per processor that can generate interrupts
  - Supports a variety of other internal interrupt sources

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- 10/100 Fast Ethernet controller (FEC) management interface
  - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
  - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
  - Four DMA channels per controller
  - All channels accessible by the local masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
  - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins ($\overline{\text{DMA2\_DREQ}}$[2]) is made available

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/– 150	ps	4, 5, 6

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	2
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1

Table 9. RESET Initialization Timing Specifications (continued)

PLL config input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the MPC8572E.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Symbol	Min	Typical	Max
PLL lock times	—	100	µs	—
Local bus PLL	—	50	µs	—

6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required GV_{DD}(typ) voltage is 1.8Vor 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	$MV_{REF}n$	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF}n - 0.04$	$MV_{REF}n + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF}n + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF}n - 0.125$	V	—
Output leakage current	I_{OZ}	–50	50	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to $MV_{REF}n$. This rail should track variations in the DC level of $MV_{REF}n$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	µA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.175 V.

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 MHz	—	–200	200	—	—
667 MHz	—	–240	240	—	—
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW.This can be determined by the following equation: tDISKEW =+/–(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

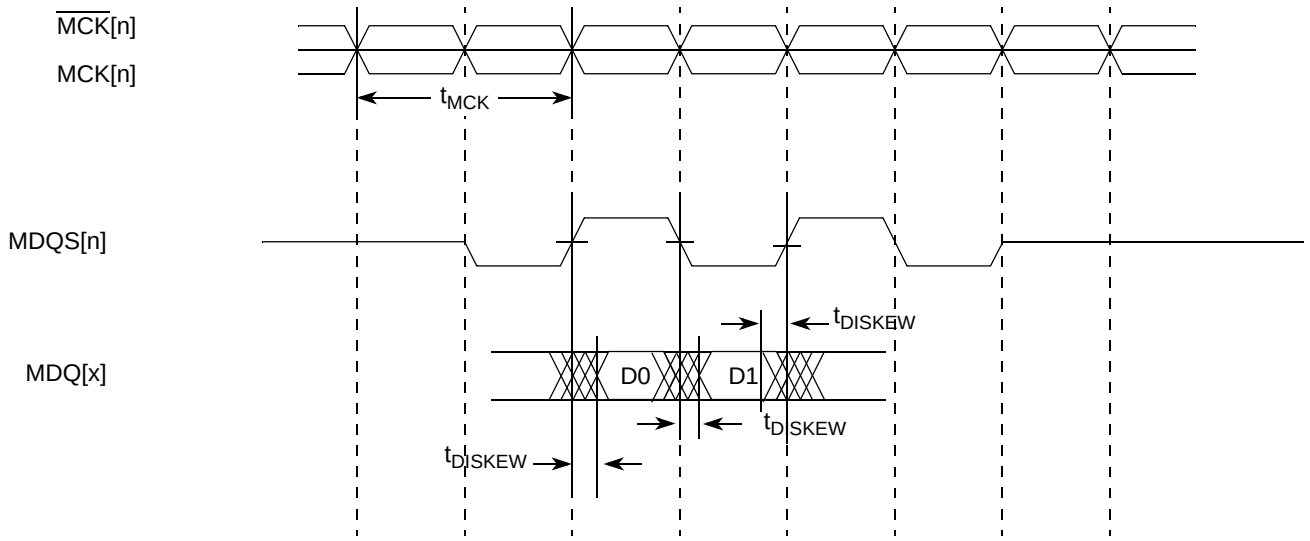


Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t_{DDKHCS}	1.95	—	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
<= 667 MHz		–0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		375	—		
667 MHz		450	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	—		

Figure 6 provides the AC test load for the DDR2 and DDR3 Controller bus.

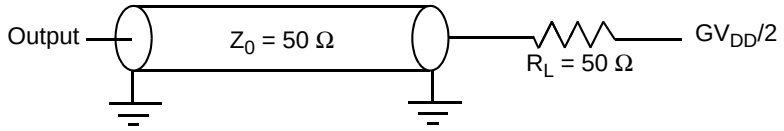
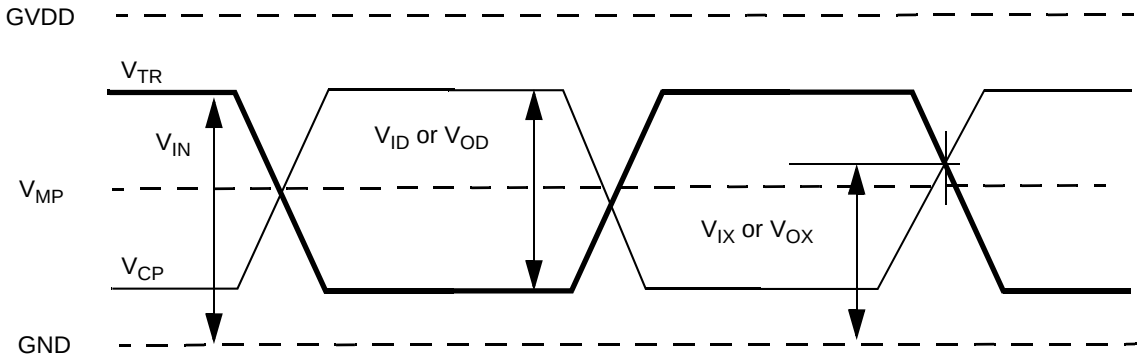


Figure 6. DDR2 and DDR3 Controller bus AC Test Load

6.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E.



NOTE

VID specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 19 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR2 mode.

Table 19. DDR2 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V_{IN}	–0.3	GV_{DD} + 0.3	V	—
DC Differential Input Voltage	V_{ID}	—	—	mV	—
AC Differential Input Voltage	V_{IDAC}	—	—	mV	—
DC Differential Output Voltage	V_{OH}	—	—	mV	—
AC Differential Output Voltage	V_{OHAC}	JEDEC: 0.5	JEDEC: GV_{DD} + 0.6	V	—
AC Differential Cross-point Voltage	V_{IXAC}	—	—	mV	—
Input Midpoint Voltage	V_{MP}	—	—	mV	—

Figure 12 shows the MII transmit AC timing diagram.

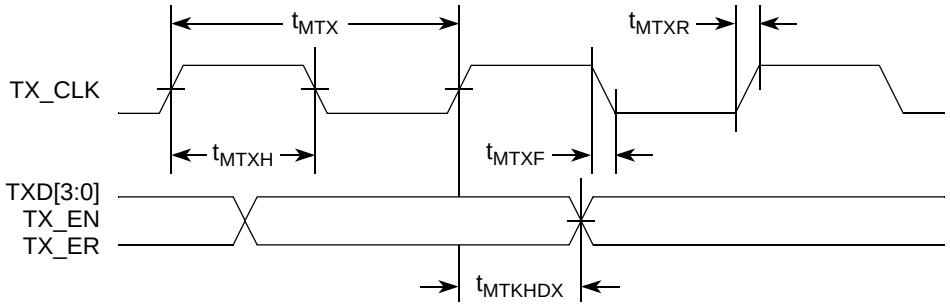


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

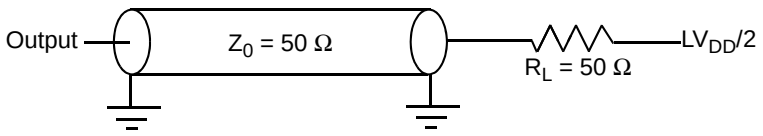


Figure 13. eTSEC AC Test Load

Figure 17 shows the TBI receive the timing diagram.

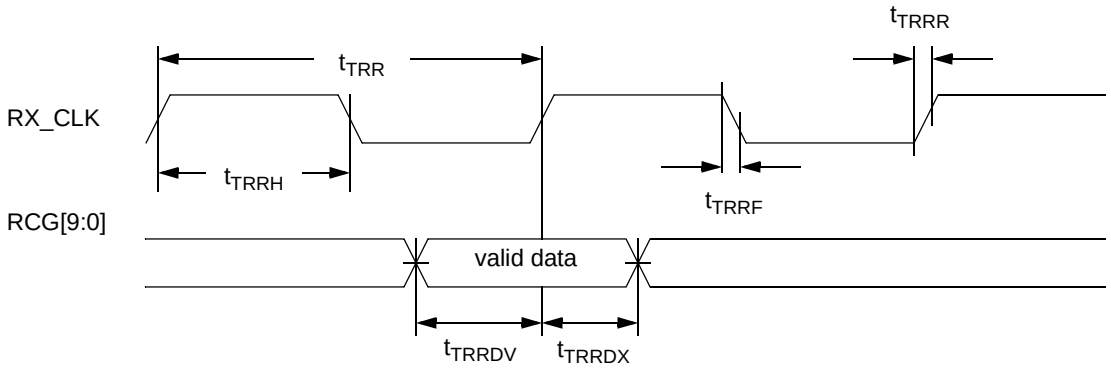


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX[n]}}$) as depicted in Figure 23.

Table 38. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	XV_{DD_SRDS2}	1.045	1.1	1.155	V	—
Output high voltage	VOH	—	—	$XV_{DD\_SRDS2-Typ}/2 + \lvert\overline{V_{OD}}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XV_{DD\_SRDS2-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	359	550	791	mV	Equalization setting: 1.0x
		329	505	725		Equalization setting: 1.09x
		299	458	659		Equalization setting: 1.2x
		270	414	594		Equalization setting: 1.33x
		239	367	527		Equalization setting: 1.5x
		210	322	462		Equalization setting: 1.71x
		180	275	395		Equalization setting: 2.0x
Output offset voltage	V_{OS}	473	550	628	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—

SD1_REF_CLK for PCI Express and Serial RapidIO, or SD2_REF_CLK and SD2_REF_CLK for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 44 shows a receiver reference diagram of the SerDes reference clocks. Characteristics are as follows:

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and SD*n*_REF_CLK are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SD*n*_REF_CLK or SD*n*_REF_CLK) has on-chip 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and SD*n*_REF_CLK inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

Table 60 describes some AC parameters common to SGMII, PCI Express and Serial RapidIO protocols.

Table 60. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200		mV	2
Differential Input Low Voltage	V_{IL}	—	-200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate (SDn_REF_CLK) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 52.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 53.

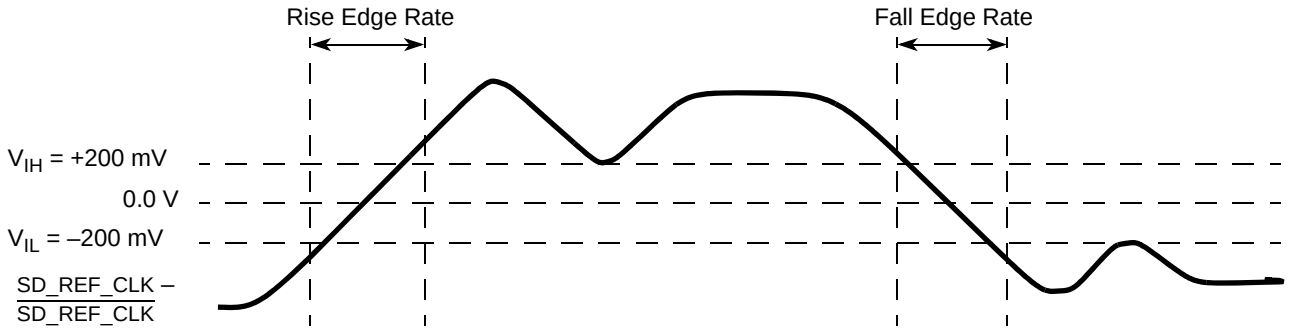


Figure 52. Differential Measurement Points for Rise and Fall Time

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 57) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 56) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

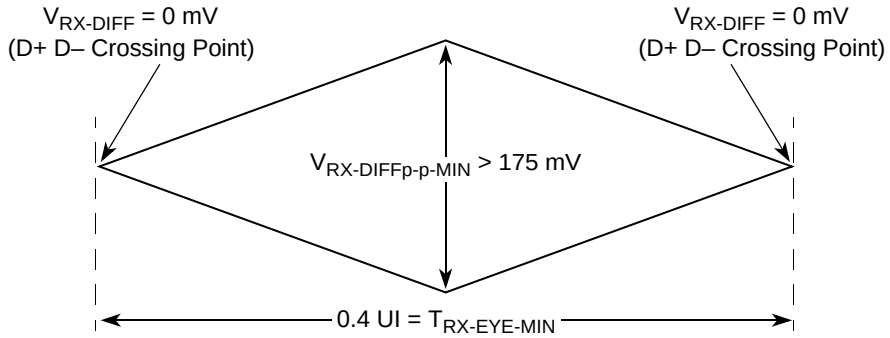


Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

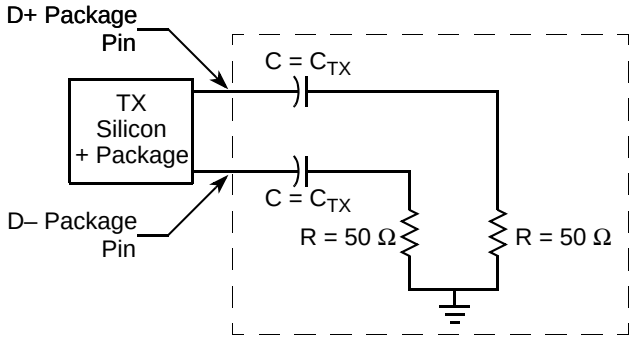


Figure 57. Compliance Test/Measurement Load

17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	Write Enable	AA2	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	Column Address Strobe	AD1	O	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	Row Address Strobe	AA1	O	GV_{DD}	—
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	O	GV_{DD}	11
$\overline{\text{D2\_MCS}}$[0:3]	Chip Select	AB1, AG2, AC1, AH2	O	GV_{DD}	—
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	O	GV_{DD}	—
$\overline{\text{D2\_MCK}}$[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	O	GV_{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	O	GV_{DD}	—
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV_{DD}	25
Local Bus Controller Interface					
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV_{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV_{DD}	—
LA[27]	Burst Address	J21	O	BV_{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	O	BV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:4]	Chip Selects	B23, E16, D20, B25, A22	O	BV_{DD}	10
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA2\_DREQ}}$[1]	Chip Selects / DMA Request	D19	I/O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[6]/$\overline{\text{DMA2\_DACK}}$[1]	Chip Selects / DMA Ack	E19	O	BV_{DD}	1, 10
$\overline{\text{LCS}}$[7]/$\overline{\text{DMA2\_DDONE}}$[1]	Chip Selects / DMA Done	C21	O	BV_{DD}	1, 10
$\overline{\text{LWE}}$[0]/$\overline{\text{LBS}}$[0]/$\overline{\text{LFWE}}$	Write Enable / Byte Select	D17	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[1]/$\overline{\text{LBS}}$[1]	Write Enable / Byte Select	F15	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[2]/$\overline{\text{LBS}}$[2]	Write Enable / Byte Select	B24	O	BV_{DD}	5, 9
$\overline{\text{LWE}}$[3]/$\overline{\text{LBS}}$[3]	Write Enable / Byte Select	D18	O	BV_{DD}	5, 9
LALE	Address Latch Enable	F19	O	BV_{DD}	5, 8, 9
LBCTL	Buffer Control	L18	O	BV_{DD}	5, 8, 9

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

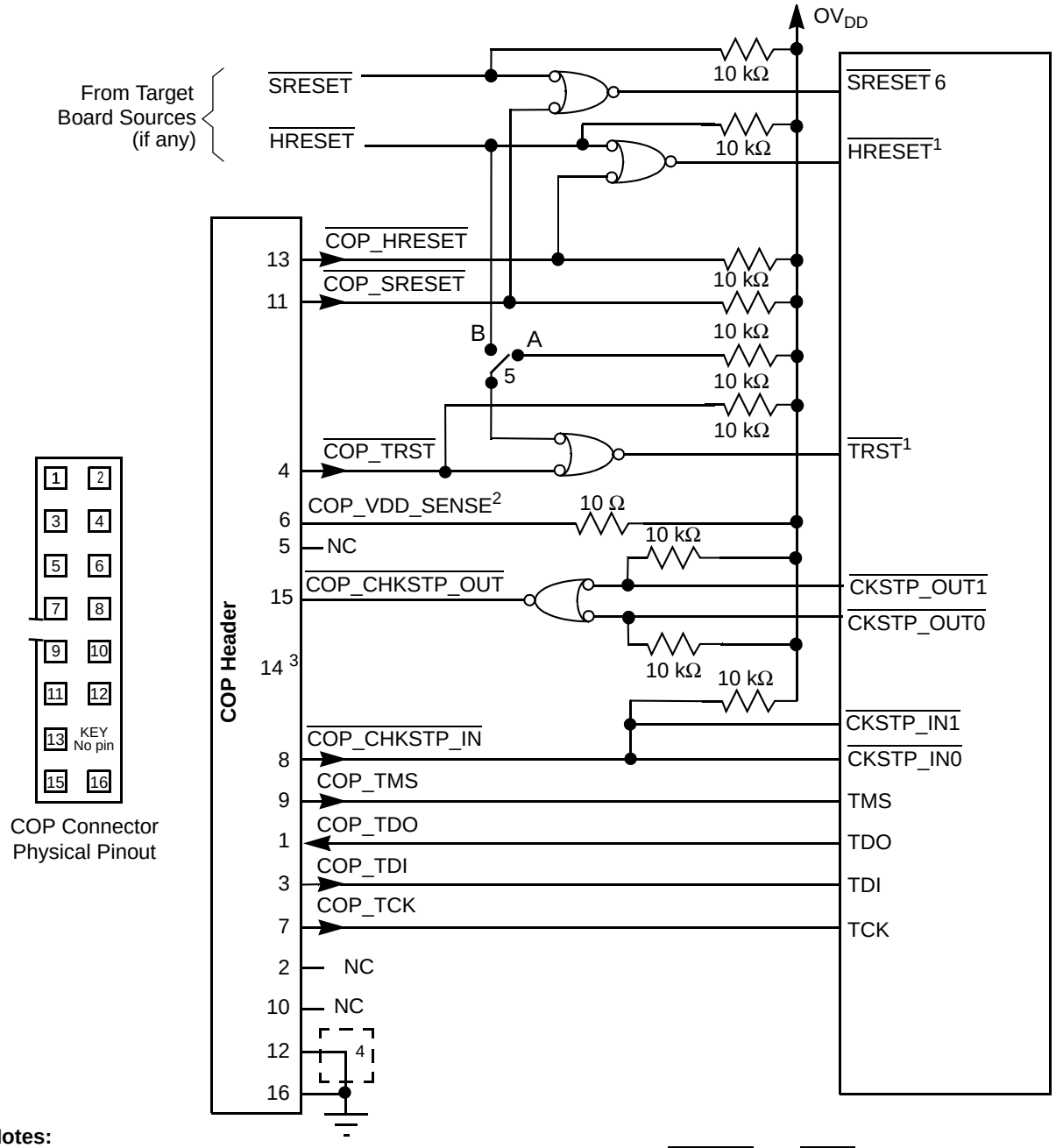
Table 77 provides the clocking specifications for both processor cores.

Table 77. MPC8572E Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1067 MHz		1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” Section 19.3, “e500 Core PLL Ratio,” and Section 19.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 cores.