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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572lvtavnd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.



2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings	Table 1	. Absolute	Maximum	Ratings
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	Characteristic	Symbol	Range	Unit	Notes
Core supply voltag	е	V _{DD}	-0.3 to 1.21	V	—
PLL supply voltage	,	AV _{DD}	-0.3 to 1.21	V	—
Core power supply	for SerDes transceivers	SV _{DD}	-0.3 to 1.21	V	—
Pad power supply for SerDes transceivers DDR SDRAM DDR2 SDRAM Interface		XV _{DD}	-0.3 to 1.21	V	—
DDR SDRAM	DDR2 SDRAM Interface	GV _{DD}	-0.3 to 1.98	V	—
supply voltage	DDR3 SDRAM Interface	_	-0.3 to 1.65		_
Three-speed Ether management volta	net I/O, FEC management interface, MII ge	LV _{DD} (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	2
		TV _{DD} (for eTSEC3 and eTSEC4, FEC)	-0.3 to 3.63 -0.3 to 2.75	—	2
DUART, system co I/O voltage	ntrol and power management, I ² C, and JTAG	OV _{DD}	-0.3 to 3.63	V	—
Local bus and GPI	O I/O voltage	BV _{DD}	-0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	3
	DDR2 and DDR3 SDRAM interface reference	MV _{REF} n	-0.3 to (GV _{DD} /2 + 0.3)	V	—
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	-0.3 to (LV _{DD} + 0.3) -0.3 to (TV _{DD} + 0.3)	V	3
	Local bus and GPIO signals	BV _{IN}	–0.3 to (BV _{DD} + 0.3)	—	—
	DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	–0.3 to (OV _{DD} + 0.3)	V	3
Storage temperatu	re range	T _{STG}	–55 to 150	°C	

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.

3. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.



RESET Initialization

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	_			+/- 150	ps	4, 5, 6

Notes:

- 1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
- 2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 **RESET** Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Мах	Unit	Notes
Required assertion time of HRESET	100	—	μs	2
Minimum assertion time for SRESET	3	—	SYSCLKs	1



PLL config input setup time with stable SYSCLK before HRESET negation	100	_	μs	
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET	4		SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET	2	_	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs	1

Table 9. RESET Initialization Timing Specifications (continued)

Notes:

2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

Table	10.	PLL	Lock	Times
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Parameter/Condition	Symbol	Min	Typical	Max
PLL lock times	_	100	μs	—
Local bus PLL	_	50	μs	_

6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required $GV_{DD}(typ)$ voltage is 1.8Vor 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF} n	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} <i>n</i> – 0.04	$MV_{REF}n + 0.04$	V	3
Input high voltage	V _{IH}	$MV_{REF}n + 0.125$	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} n – 0.125	V	_
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	_	mA	—

DDDO ODDAM Late	uface DO Electula	- I O le ave et eviletie e	$f_{a,m} = O(1 - (f_{a,m})) = A = O(1)$,
DURZ SURAW INTE	rtace DU Electric	al Unaracteristics	TOT (= V = (TVD) = T A V	

^{1.} SYSCLK is the primary clock input for the MPC8572E.

DDR2 and DDR3 SDRAM Controller

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Output low current ($V_{OUT} = 0.280 V$)	I _{OL}	13.4		mA	_

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm GV}_{\rm DD}$ at all times.

- 2. $MV_{REF}n$ is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to MV_{REF}*n*. This rail should track variations in the DC level of MV_{REF}*n*.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV _{DD}	1.425	1.575	V	1
I/O reference voltage	MV _{REF} n	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
Input high voltage	V _{IH}	$MV_{REF}n + 0.100$	GV _{DD}	V	—
Input low voltage	V _{IL}	GND	MV _{REF} <i>n</i> – 0.100	V	—
Output leakage current	I _{OZ}	-50	50	μA	3

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm GV}_{\rm DD}$ at all times.

2. $MV_{REF}n$ is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.

3. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Мах	Unit
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.175 V.



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter	Value	Unit	Notes
Minimum baud rate	f _{CCB} /1,048,576	baud	1, 2
Maximum baud rate	f _{CCB} /16	baud	1, 2, 3
Oversample rate	16	_	1, 4

Notes:

1. Guaranteed by design

- 2. f_{CCB} refers to the internal platform clock frequency.
- 3. Actual attainable baud rate is limited by the latency of interrupt processing.
- 4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V.

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

The electrical characteristics for SGMII is specified in Section 8.3, "SGMII Interface Electrical Characteristics." The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_DD/TV_DD of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to TSECn_TX_CLK rising edge	t _{RMRDX}	2.0	—	_	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 20 provides the AC test load for eTSEC.



Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.



Figure 21. RMII Receive AC Timing Diagram

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of MPC8572E as shown in Figure 22, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 54.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines



Ethernet Management Interface Electrical Characteristics

Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
TSEC_1588_CLK_OUT duty cycle	t _{T1588} CLKOTH /t _{T1588} CLKOUT	30	50	70	%	_
TSEC_1588_PULSE_OUT	t _{T1588OV}	0.5	_	3.0	ns	_
TSEC_1588_TRIG_IN pulse width	t _{T1588} trigh	2*t _{T1588CLK_MAX}	—	_	ns	2

Note:

1.When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of t_{T1588CLK} is defined in terms of T_{TX_CLK}, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of t_{T1588CLK} is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of t_{T1588CLK} is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.

2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	LV _{DD} /TV _{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V	—
Output low voltage (LV _{DD} /TV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V	—
Input high voltage	V _{IH}	2.0	—	V	_
Input low voltage	V _{IL}	—	0.90	V	_
Input high current $(LV_{DD}/TV_{DD} = Max, V_{IN}^{3} = 2.1 \text{ V})$	Iн	_	40	μΑ	—

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD} =3.3 V)



Ethernet Management Interface Electrical Characteristics

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
ECn_MDIO to ECn_MDC setup time	t _{MDDVKH}	5	—	-	ns	_
ECn_MDIO to ECn_MDC hold time	t _{MDDXKH}	0	—	-	ns	_
ECn_MDC rise time	t _{MDCR}	—	—	10	ns	4
ECn_MDC fall time	t _{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state)

(reference)(state) for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3$ MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
- 4. Guaranteed by design.
- 5. t_{plb clk} is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.



Figure 28. MII Management Interface Timing Diagram



10 Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8572E.

10.1 Local Bus DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3 \text{ V}$ DC.

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV _{DD}	3.13	3.47	V
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	_	±5	μA
High-level output voltage (BV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	BV _{DD} – 0.2	—	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	_	0.2	V

 Table 46. Local Bus DC Electrical Characteristics (3.3 V DC)
 Image: Comparison of the second sec

Note:

1. Note that the symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 47 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5 V DC$.

Table 47. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current	I _{IH}	—	10	μΑ
$(BV_{IN} = 0 V \text{ of } BV_{IN} = BV_{DD})$	Ι _{ΙL}		-15	
High-level output voltage (BV _{DD} = min, I _{OH} = -1 mA)	V _{OH}	2.0	BV _{DD} + 0.3	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 1 mA)	V _{OL}	GND – 0.3	0.4	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.



Local Bus Controller (eLBC)

Figure 30 through Figure 35 show the local bus signals.



Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

Table 52 describes the general timing parameters of the local bus interface at $BV_{DD} = 3.3 \text{ V DC}$ with PLL disabled.

Table 52. Local Bus General Timing Parameters—PLL Bypassed

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	12		ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	2.3	4.0	ns	
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	5.8	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	5.7	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.3	_	ns	4, 5



Local Bus Controller (eLBC)



Figure 31. Local Bus Signals (PLL Bypass Mode)



6. Differential Waveform

- 1. The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the non-inverting signal (SDn_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
- 2. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.



Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and



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Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.



Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)



Serial RapidIO



Figure 60. Receiver Input Compliance Mask

Table 75.	Receiver Ir	nput Compliance	Mask Parameters	Exclusive of	of Sinusoidal Jitte
14010 101		ipat eeinpilaliee	maon i aramotoro		

Receiver Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial



Signal	Signal Name Package Pin Numbe		Pin Type	Power Supply	Notes		
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	0	BV _{DD}	5, 9		
LGPL1/LFALE	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	0	BV _{DD} 5, 9			
LGPL2/LOE/LFRE	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O BV _{DD} 5, 8,		5, 8, 9		
LGPL3/LFWP	UPM General Purpose Line 3 / Flash Write Protect	K16	0	BV _{DD}	5, 9		
LGPL4/LGTA/LUPWAIT/LPBSE /LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV _{DD}	_		
LGPL5	UPM General Purpose Line 5 / Amux	B26	0	BV _{DD}	5, 9		
LCLK[0:2]	Local Bus Clock	F17, F16, A23	0	BV _{DD}	-		
LSYNC_IN	Local Bus DLL Synchronization	Local Bus DLL Synchronization B22		BV _{DD}			
LSYNC_OUT	Local Bus DLL Synchronization	A21	0	BV _{DD}			
DMA							
DMA1_DACK[0:1]	DMA Acknowledge	W25, U30	0	OV _{DD}	21		
DMA2_DACK[0]	DMA Acknowledge	AA26	0	OV _{DD}	5, 9		
DMA1_DREQ[0:1]	DMA Request	Y29, V27	I	OV _{DD}	_		
DMA2_DREQ[0]	DMA Request	V29	I	OV _{DD}	_		
DMA1_DDONE[0:1]	DMA Done	Y28, V30	0	OV _{DD}	5, 9		
DMA2_DDONE[0]	DMA Done AA28		0	OV _{DD}	5, 9		
DMA2_DREQ[2]	DMA Request	M23	I	BV _{DD}	_		
Programmable Interrupt Controller							
UDE0	Unconditional Debug Event Processor 0	AC25	I	OV _{DD}	_		
UDE1	Unconditional Debug Event Processor 1	AA25	Ι	OV _{DD}			
MCP0	Machine Check Processor 0	M28	I	OV _{DD}	_		
MCP1	Machine Check Processor 1	L28	I	OV _{DD}	—		
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV _{DD}	_		

Table 76. MPC8572E Pinout Listing (continued)



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω (±1%) to GND	_
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω (±1%) to GND	_
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	0	AVDD_S RDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	Ι	$\begin{array}{c} 200\Omega \\ (\pm1\%) \text{ to} \\ \text{GND} \end{array}$	_
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	Ι	100Ω (±1%) to GND	_
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	0	AVDD_S RDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	_	internal diode	14
No Connection Pins					

Table 76. MPC8572E Pinout Listing (continued)



Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
25 When exerting in DDD2 mode, compact Dr. MDICI01te ground through 40.2.0.4 (full strength mode) as 20.4.0 (holf strength					

25. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect Dn_% resistor, and connect Dn_MDIC[1] to GVDD through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

- 26. These pins should be connected to XVDD_SRDS1.
- 27. These pins should be pulled to ground (XGND_SRDS1) through a 300- Ω (±10%) resistor.
- 28. These pins should be left floating.
- 29. These pins should be pulled up to TVDD through a 2–10 K Ω resistor.
- 30. These pins have other manufacturing or debug test functions. It is recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
- 31. DDRCLK input is only required when the MPC8572E DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the MPC8572E PowerQUICC[™] III Integrated Host Processor Family Reference Manual Rev.0, Table 4-3 in section 4.2.2 "Clock Signals", section 4.4.3.2 "DDR PLL Ratio" and Table 4-10 "DDR Complex Clock PLL Ratio" for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
- 32. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
- 33. These pins should be pulled to ground (GND).
- 34. These pins are sampled at POR for General Purpose configuration use by software. Their value has no impact on the functionality of the hardware.



Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

<u>Bina</u> ry <u>Value</u> of <u>L</u> WE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	<u>Bina</u> ry V <u>alue</u> of <u>L</u> WE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	
000	Reserved	100	2:1	
001	Reserved	101	5:2 (2.5:1)	
010	Reserved	110	3:1	
011	3:2 (1.5:1)	111	7:2 (3.5:1)	

Table 81.	e500	Core1	to	ССВ	Clock	Ratio

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio		
000	3:1		
001	4:1		
010	6:1		
011	8:1		
100	10:1		

Table 82. DDR Clock Ratio



Thermal

 $V_f > 0.40$ V $V_f < 0.90$ V $Operating \ range \ 2-300 \ \mu A$ $Diode \ leakage < 10 \ nA \ @ \ 125^{\circ}C$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$\mathbf{V}_{H} - \mathbf{V}_{L} = \mathbf{n} \frac{\mathrm{KT}}{\mathrm{q}} \left[\mathbf{I} \mathbf{n} \frac{\mathrm{I}_{H}}{\mathrm{I}_{L}} \right]$$

Where:

 $I_{fw} = Forward current$ $I_s = Saturation current$ $V_d = Voltage at diode$ $V_f = Voltage forward biased$ $V_H = Diode voltage while I_H is flowing$ $V_L = Diode voltage while I_L is flowing$ $I_H = Larger diode bias current$ $I_L = Smaller diode bias current$ $q = Charge of electron (1.6 \times 10^{-19} \text{ C})$ n = Ideality factor (normally 1.0) $K = Boltzman's constant (1.38 \times 10^{-23} \text{ Joules/K})$ T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

 $V_{\text{H}} - V_{\text{L}} = ~1.986 \times 10^{-4} \times nT$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{\mathbf{V}_{\mathsf{H}} - \mathbf{V}_{\mathsf{L}}}{1.986 \times 10^{-4}}$$