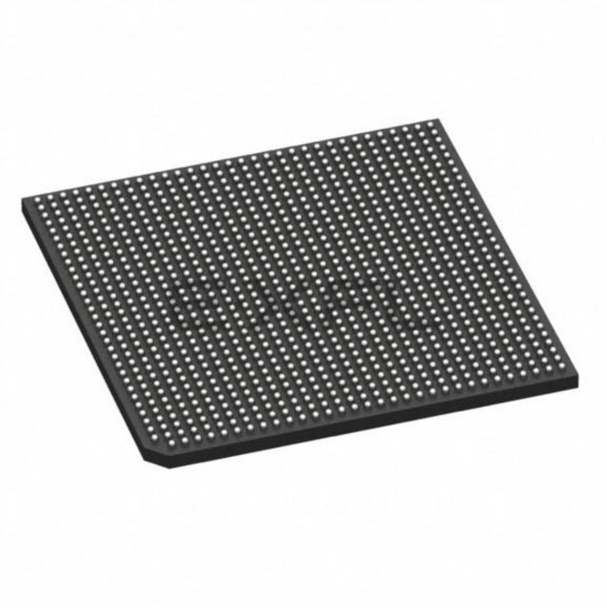


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxarlb

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5, 6

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3V ± 5% or 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TV_{DD}=2.5V L/TV_{DD}=3.3V	t_{G125R}, t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD}=2.5V, and from 0.6V and 2.7V for L/TV_{DD}=3.3V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

Table 8. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	100	MHz	1
DDRCLK cycle time	t_{DDRCLK}	10.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	3

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to $MV_{REF}n$. This rail should track variations in the DC level of $MV_{REF}n$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	μA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for GV_{DD}(typ)=1.8 V and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.175 V.

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 MHz	—	–200	200	—	—
667 MHz	—	–240	240	—	—
533 MHz	—	–300	300	—	—
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW.This can be determined by the following equation: tDISKEW =+/–(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

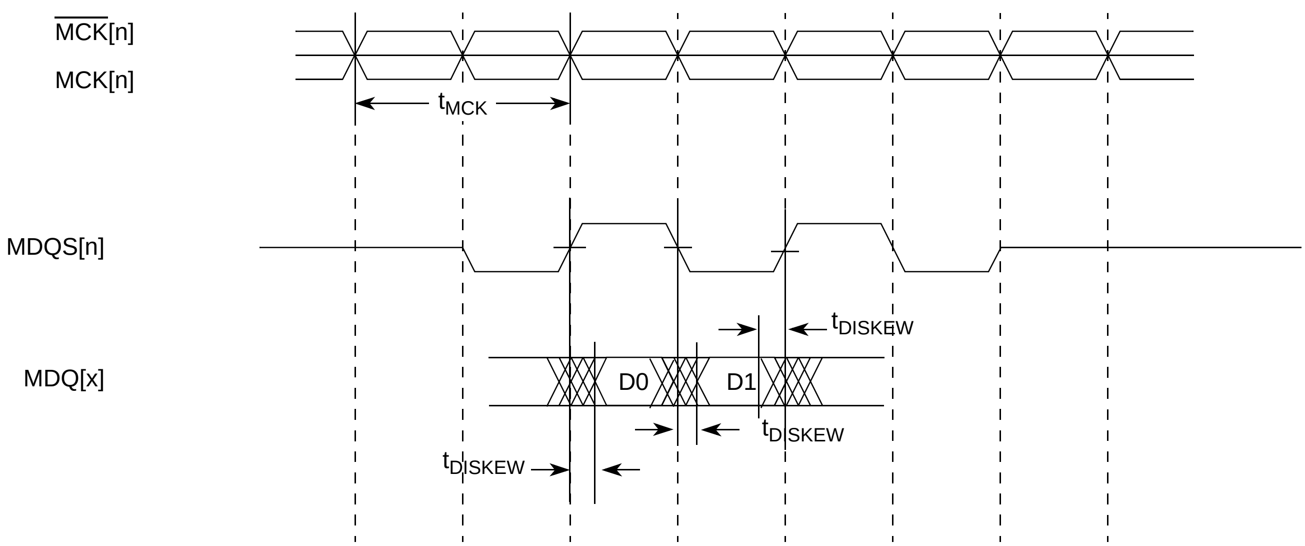


Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)

Parameters	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

[1] LV_{DD} supports eTSECs 1 and 2.
[2] TV_{DD} supports eTSECs 3 and 4 or FEC.
[3] Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

Table 25. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period[1]	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%

Figure 12 shows the MII transmit AC timing diagram.

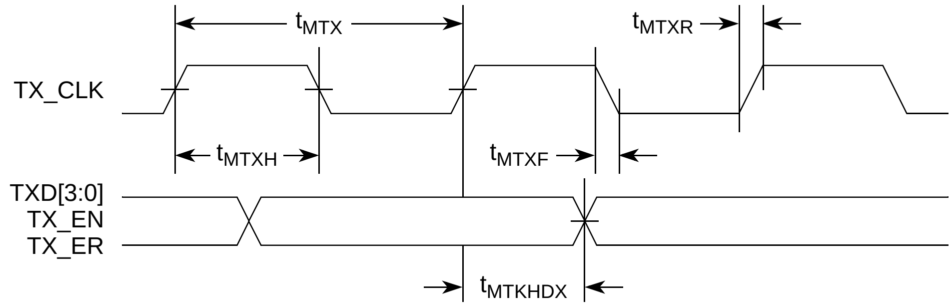


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

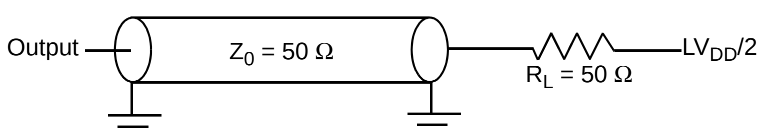


Figure 13. eTSEC AC Test Load

Figure 16 shows the TBI receive AC timing diagram.

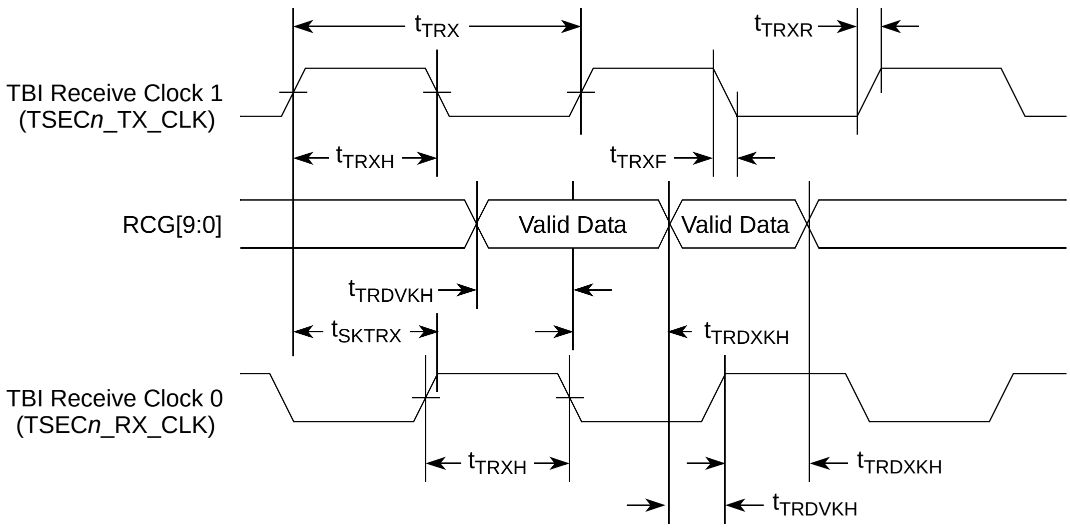


Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	—	—	ns

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

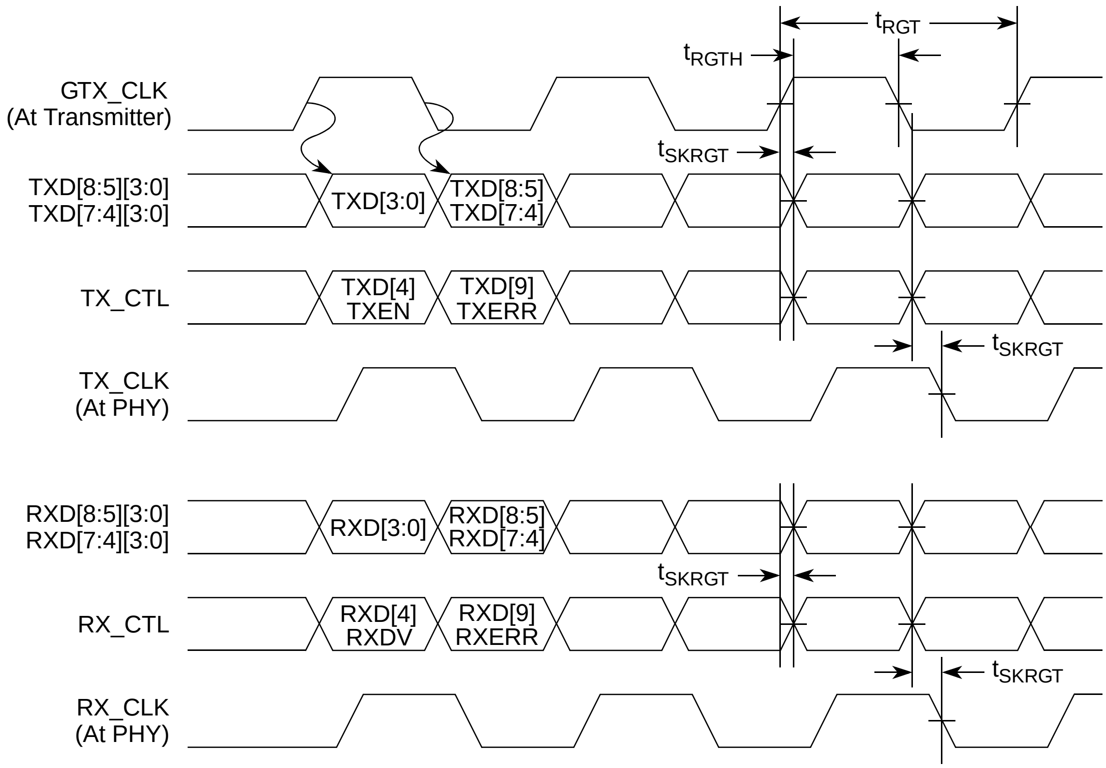


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 23.

Table 38. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	XV_{DD_SRDS2}	1.045	1.1	1.155	V	—
Output high voltage	VOH	—	—	$XV_{DD\_SRDS2\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	VOL	$XV_{DD\_SRDS2\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	359	550	791	mV	Equalization setting: 1.0x
		329	505	725		Equalization setting: 1.09x
		299	458	659		Equalization setting: 1.2x
		270	414	594		Equalization setting: 1.33x
		239	367	527		Equalization setting: 1.5x
		210	322	462		Equalization setting: 1.71x
		180	275	395		Equalization setting: 2.0x
Output offset voltage	V_{OS}	473	550	628	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	6.67	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	2.4	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.

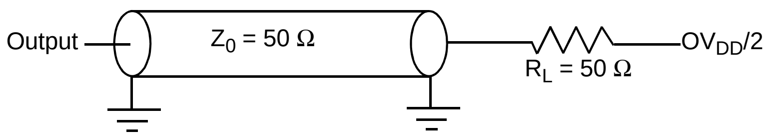


Figure 36. AC Test Load for the JTAG Interface

Figure 37 provides the JTAG clock input timing diagram.

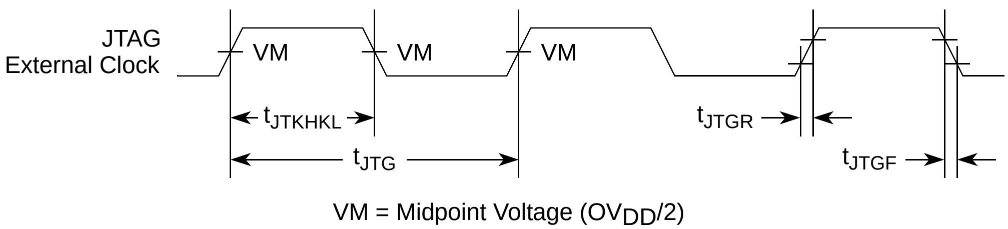


Figure 37. JTAG Clock Input Timing Diagram

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} – V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: V_{SDn_RX} - $V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage**, **V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A – B|$ Volts.

5. **Differential Peak-to-Peak**, **$V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$L_{RX\text{-}SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 57 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 56). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 57). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

Table 64. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Table 74. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

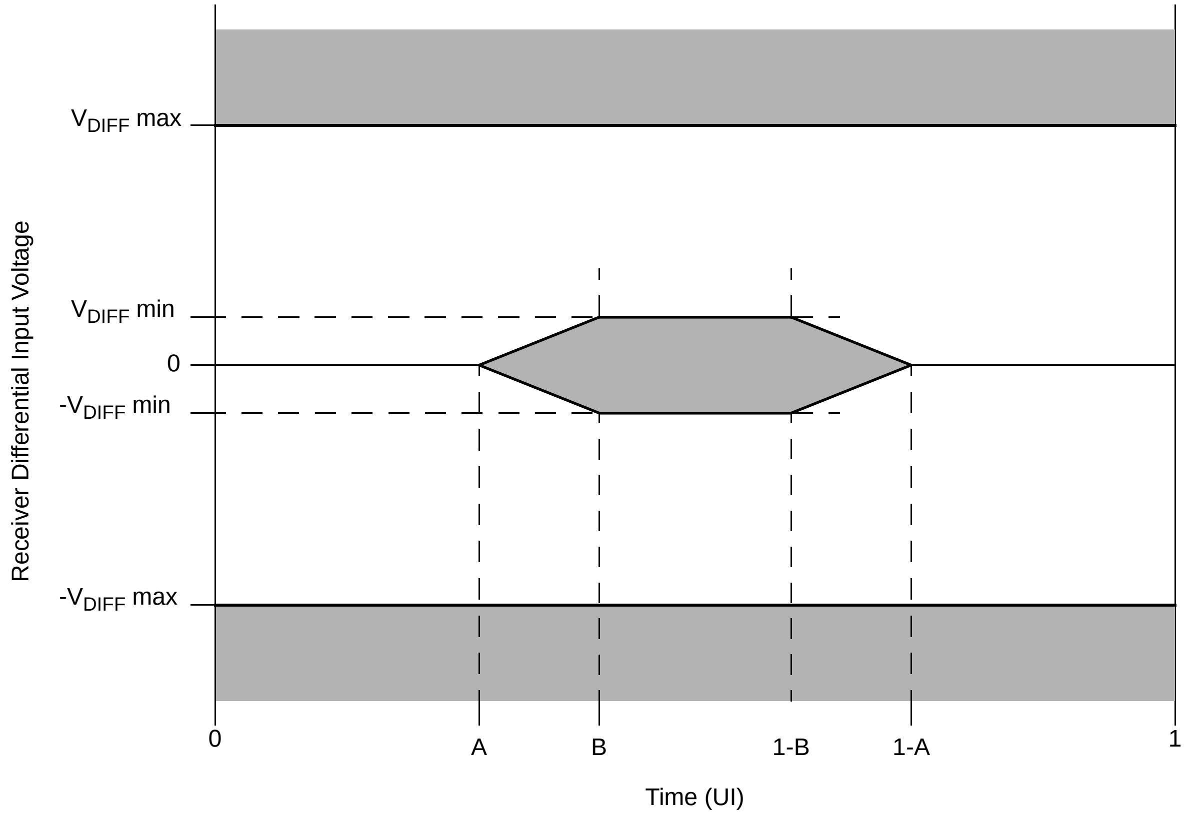


Figure 60. Receiver Input Compliance Mask

Table 75. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial

5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.

18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

Table 76. MPC8572E Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MDQ[0:63]	Data	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17	I/O	GV_{DD}	—
D1_MECC[0:7]	Error Correcting Code	M10, M7, R8, T11, L12, L11, P9, R10	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	P6	I	GV_{DD}	—
D1_MAPAR_OUT	Address Parity Out	W6	O	GV_{DD}	—
D1_MDM[0:8]	Data Mask	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11	O	GV_{DD}	—
D1_MDQS[0:8]	Data Strobe	A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS}}$[0:8]	Data Strobe	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	GV_{DD}	—
D1_MA[0:15]	Address	Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7	O	GV_{DD}	—
D1_MBA[0:2]	Bank Select	AA7, AA8, R7	O	GV_{DD}	—
$\overline{\text{D1\_MWE}}$	Write Enable	AC12	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_GTX_CLK	Transmit Clock Out	AE17	O	TV_{DD}	
TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK	Receive Clock	AF17	I	TV_{DD}	1
TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV	Receive Data Valid	AG14	I	TV_{DD}	1
TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER	Receive Error	AH15	I	TV_{DD}	1
TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK	Transmit Clock In	AF16	I	TV_{DD}	1
TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN	Transmit Enable	AJ18	O	TV_{DD}	1, 22
Three-Speed Ethernet Controller 4					
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4]	Transmit Data	AD15, AC16, AC14, AB16	O	TV_{DD}	1, 5, 9
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4]	Receive Data	AE15, AF13, AE14, AH14	I	TV_{DD}	1
TSEC4_GTX_CLK	Transmit Clock Out	AB14	O	TV_{DD}	—
TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC	Receive Clock	AG13	I	TV_{DD}	1
TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC	Receive Data Valid	AD13	I/O	TV_{DD}	1, 23
TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER	Transmit Enable	AB15	O	TV_{DD}	1, 22
DUART					
$\overline{\text{UART\_CTS}}$[0:1]	Clear to Send	W30, Y27	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	Ready to Send	W31, Y30	O	OV_{DD}	5, 9
UART_SIN[0:1]	Receive Data	Y26, W29	I	OV_{DD}	—
UART_SOUT[0:1]	Transmit Data	Y25, W26	O	OV_{DD}	5, 9
I^2C Interface					
IIC1_SCL	Serial Clock	AC30	I/O	OV_{DD}	4, 20
IIC1_SDA	Serial Data	AB30	I/O	OV_{DD}	4, 20
IIC2_SCL	Serial Clock	AD30	I/O	OV_{DD}	4, 20
IIC2_SDA	Serial Data	AD29	I/O	OV_{DD}	4, 20
SerDes (x10) PCIe, SRIO					

Figure 62 shows the PLL power supply filter circuits.

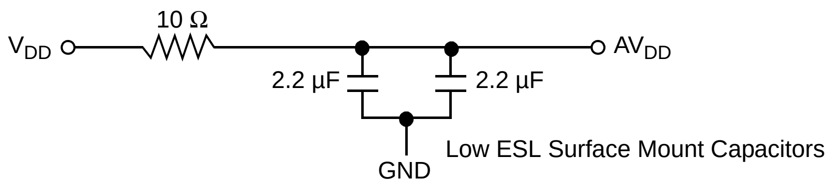
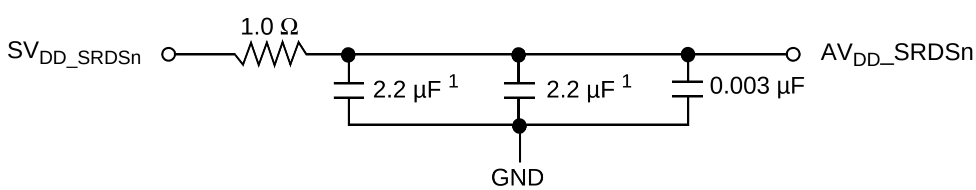


Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD}_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

AV_{DD}_SRDSn should be a filtered version of SV_{DD}_SRDS*n*.

NOTE

Signals on the SerDesn interface are fed from the XV_{DD}_SRDS*n* power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.