# E·XFL



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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxarld

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
  - Shared by both cores.
  - Flexible configuration and individually configurable per core.
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and Flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be Flash cleared separately.
  - Per-way allocation of cache region to a given processor.
  - SRAM features include the following:
    - 1, 2, 4, or 8 ways can be configured as SRAM.
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
  - Twelve local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.



Overview

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
  - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1<sup>TM</sup> virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision



- Three PCI Express controllers
  - PCI Express 1.0a compatible
  - Supports x8, x4, x2, and x1 link widths (see following bullet for specific width configuration options)
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Full 64-bit decode with 36-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
  - Single x8/x4/x2/x1 PCI Express
  - Dual x4/x2/x1 PCI Express
  - Single x4/x2/x1 PCI Express and dual x2/x1 PCI Express
  - Single 1x/4x Serial RapidIO and single x4/x2/x1 PCI Express
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, that automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the eight counters
  - Supports duration and quantity threshold counting
  - Permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1<sup>™</sup> compatible, JTAG boundary scan
- 1023 FC-PBGA package



Electrical Characteristics

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV <sub>DD</sub> = 3.3 V BV <sub>DD</sub> = 2.5 V	1
	45(default) 45(default) 125	BV <sub>DD</sub> = 3.3 V BV <sub>DD</sub> = 2.5 V BV <sub>DD</sub> = 1.8 V	
DDR2 signal	18 36 (half strength mode)	GV <sub>DD</sub> = 1.8 V	2
DDR3 signal	20 40 (half strength mode)	GV <sub>DD</sub> = 1.5 V	2
eTSEC/10/100 signals	45	L/TV <sub>DD</sub> = 2.5/3.3 V	—
DUART, system control, JTAG	45	OV <sub>DD</sub> = 3.3 V	_
12C	150	OV <sub>DD</sub> = 3.3 V	

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at  $T_i = 105^{\circ}C$  and at  $GV_{DD}$  (min).

# 2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

- 1. V<sub>DD</sub>, AV<sub>DD</sub>\_*n*, BV<sub>DD</sub>, LV<sub>DD</sub>, OV<sub>DD</sub>, SV<sub>DD</sub>\_SRDS1 and SV<sub>DD</sub>\_SRDS2, TV<sub>DD</sub>, XV<sub>DD</sub>\_SRDS1 and XV<sub>DD</sub>\_SRDS2
- 2. GV<sub>DD</sub>

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for  $GV_{DD}$  is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for  $GV_{DD}$  is not required.



# 4 Input Clocks

# 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

#### Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with  $OV_{DD}$  of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f <sub>SYSCLK</sub>	33	—	133	MHz	1
SYSCLK cycle time	t <sub>SYSCLK</sub>	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t <sub>KHK</sub> /tsysclk	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

- 2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{CCB}$ , and minimum clock low time is  $2 \times t_{CCB}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.



**RESET** Initialization

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with  $OV_{DD}$  of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	_			+/- 150	ps	4, 5, 6

Notes:

- 1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
- 2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

## 4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

## 4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

# 5 **RESET** Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

#### **Table 9. RESET Initialization Timing Specifications**

Parameter/Condition	Min	Мах	Unit	Notes
Required assertion time of HRESET	100	—	μs	2
Minimum assertion time for SRESET	3	—	SYSCLKs	1



# Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t <sub>DDKHAX</sub>			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCS[n] output setup with respect to MCK	t <sub>DDKHCS</sub>			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t <sub>DDKHCS</sub>	1.95	_	ns	3
MCS[n] output hold with respect to MCK	t <sub>DDKHCX</sub>			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t <sub>DDKHMH</sub>			ns	4
800 MHz		-0.375	0.375		
<= 667 MHz		-0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t <sub>DDKHDS,</sub> t <sub>DDKLDS</sub>			ps	5
800 MHz		375	_		
667 MHz		450	_		
533 MHz		538	_		
400 MHz		700	_		
MDQ/MECC/MDM output hold with respect to MDQS	t <sub>DDKHDX,</sub> t <sub>DDKLDX</sub>			ps	5
800 MHz		375	—		
667 MHz		450	_		



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

### 8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 24. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV <sub>DD</sub> TV <sub>DD</sub>	3.13	3.47	V	1, 2
Output high voltage $(LV_{DD}/TV_{DD} = Min, IOH = -4.0 mA)$	VOH	2.40	LV <sub>DD</sub> /TV <sub>DD</sub> + 0.3	V	—
Output low voltage $(LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)$	VOL	GND	0.50	V	—
Input high voltage	V <sub>IH</sub>	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V <sub>IL</sub>	-0.3	0.90	V	—
Input high current $(V_{IN} = LV_{DD}, V_{IN} = TV_{DD})$	IIH	_	40	μΑ	1, 2,3
Input low current (V <sub>IN</sub> = GND)	Ι <sub>ΙL</sub>	-600	_	μA	3

Table 23.	GMII.	MII. RMII.	and TBI DC	Electrical	Characteristics
	<b>.</b> ,	,		Liootiioui	0114140101101100

#### Notes:

<sup>1</sup> LV<sub>DD</sub> supports eTSECs 1 and 2.

 $^{2}$  TV<sub>DD</sub> supports eTSECs 3 and 4 or FEC.

 $^{3}$  The symbol V<sub>IN</sub>, in this case, represents the LV<sub>IN</sub> and TV<sub>IN</sub> symbols referenced in Table 1.

#### Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV <sub>DD/</sub> TV <sub>DD</sub>	2.37	2.63	V	1,2
Output high voltage ( $LV_{DD}/TV_{DD} = Min, IOH = -1.0 mA$ )	V <sub>OH</sub>	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ( $LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA$ )	V <sub>OL</sub>	GND – 0.3	0.40	V	—
Input high voltage	V <sub>IH</sub>	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V <sub>IL</sub>	-0.3	0.70	V	—



Table 25. FIFO Mode Transmit AC Timing Specification (continued)

At recommended operating conditions with LV\_{DD}/TV\_{DD} of 2.5V  $\pm\,5\%$ 

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
TX_CLK, GTX_CLK peak-to-peak jitter	t <sub>FITJ</sub>	—	_	250	ps
Rise time TX_CLK (20%–80%)	t <sub>FITR</sub>	—	_	0.75	ns
Fall time TX_CLK (80%–20%)	t <sub>FITF</sub>	—	_	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t <sub>FITDV</sub>	2.0	_	_	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t <sub>FITDX</sub>	0.5	_	3.0	ns

Notes:

1. The minimum cycle period (or maximum frequency) of the TX\_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

#### Table 26. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with  $LV_{DD}/TV_{DD}$  of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period <sup>1</sup>	t <sub>FIR</sub>	5.3	8.0	100	ns
RX_CLK duty cycle	t <sub>FIRH</sub> /t <sub>FIR</sub>	45	50	55	%
RX_CLK peak-to-peak jitter	t <sub>FIRJ</sub>	—	—	250	ps
Rise time RX_CLK (20%–80%)	t <sub>FIRR</sub>	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t <sub>FIRF</sub>	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>FIRDV</sub>	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>FIRDX</sub>	0.5	—	—	ns

1. The minimum cycle period (or maximum frequency) of the RX\_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Figure 7 and Figure 8 show the FIFO timing diagrams.



Figure 7. FIFO Transmit AC Timing Diagram



#### Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Figure 14 shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram

### 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

#### Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV\_{DD}/TV\_{DD} of 2.5/ 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t <sub>TTKHDV</sub>	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t <sub>TTKHDX</sub>	1.0	—	—	ns
GTX_CLK rise (20%-80%)	t <sub>TTXR</sub> <sup>2</sup>	_	—	1.0	ns
GTX_CLK fall time (80%–20%)	t <sub>TTXF</sub> <sup>2</sup>	_	_	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t<sub>(first two letters of functional block)(signal)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TTKHDV</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TTX</sub> represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.



Table 51. Local Bus General Timing Parameters (BV<sub>DD</sub> = 1.8 V DC)—PLL Enabled (continued)

At recommended operating conditions with  $\mathsf{BV}_{\mathsf{DD}}$  of 1.8 V ± 5% (continued)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.1	_	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t <sub>lbotot</sub>	1.2	_	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	_	3.2	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	_	3.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	_	3.2	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	_	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.9	_	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.9		ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.6	ns	5

Note:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t<sub>(First two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one(1). Also, t<sub>LBKHOX</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from BV<sub>DD</sub>/2 of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 1.8-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.



Figure 29. Local Bus AC Test Load





Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



# **11** Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

# 12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

Table 53. JTAG	AC Timina	Specifications	(Independent	t of SYSCLK)	1
	/ · · · · · · · · · · · · · · · · · · ·	opeenieanene	(		

At recommended operating conditions with  $OV_{DD}$  of 3.3 V ± 5%.

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f <sub>JTG</sub>	0	33.3	MHz	—
JTAG external clock cycle time	t <sub>JTG</sub>	30	_	ns	—
JTAG external clock pulse width measured at 1.4 V	t <sub>JTKHKL</sub>	15	—	ns	—
JTAG external clock rise and fall times	t <sub>JTGR</sub> & t <sub>JTGF</sub>	0	2	ns	6
TRST assert time	t <sub>trst</sub>	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t <sub>JTDVKH</sub> t <sub>JTIVKH</sub>	4 0		ns	4
Input hold times: Boundary-scan data TMS, TDI	t <sub>JTDXKH</sub> t <sub>JTIXKH</sub>	20 25		ns	4
Valid times: Boundary-scan data TDO	t <sub>jtkldv</sub> t <sub>jtklov</sub>	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	t <sub>jtkldx</sub> t <sub>jtklox</sub>	30 30		ns	5



Symbol	Parameter	Min	Nominal	Max	Units	Comments
V <sub>TX-DC-CM</sub>	The TX DC Common Mode Voltage	0	_	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
I <sub>TX-SHORT</sub>	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
T <sub>TX-IDLE-MIN</sub>	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	_		20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	_		20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
RL <sub>TX-DIFF</sub>	Differential Return Loss	12	—	_	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL <sub>TX-CM</sub>	Common Mode Return Loss	6	—	_	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
Z <sub>TX-DIFF-DC</sub>	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z <sub>TX-DC</sub>	Transmitter DC Impedance	40	_		Ω	Required TX D+ as well as D- DC Impedance during all states
L <sub>TX-SKEW</sub>	Lane-to-Lane Output Skew	_	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C <sub>TX</sub>	AC Coupling Capacitor	75	_	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.



Serial RapidIO

Characteristic	Symbol	Range		Unit	Notos	
	Symbol	Min	Мах	Unit	Notes	
Differential Input Voltage	V <sub>IN</sub>	200	1600	mV p-p	Measured at receiver	
Deterministic Jitter Tolerance	J <sub>D</sub>	0.37	—	UI p-p	Measured at receiver	
Combined Deterministic and Random Jitter Tolerance	J <sub>DR</sub>	0.55	—	UI p-p	Measured at receiver	
Total Jitter Tolerance <sup>1</sup>	J <sub>T</sub>	0.65	_	UI p-p	Measured at receiver	
Multiple Input Skew	S <sub>MI</sub>	_	22	ns	Skew at the receiver input between lanes of a multilane link	
Bit Error Rate	BER	—	10 <sup>-12</sup>	—	—	
Unit Interval	UI	320	320	ps	+/- 100 ppm	

#### Table 74. Receiver AC Timing Specifications—3.125 GBaud

#### Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes				
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	0	BV <sub>DD</sub>	5, 9				
LGPL1/LFALE	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	0	BV <sub>DD</sub>	5, 9				
LGPL2/LOE/LFRE	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	0	BV <sub>DD</sub>	5, 8, 9				
LGPL3/LFWP	UPM General Purpose Line 3 / Flash Write Protect	K16	0	BV <sub>DD</sub>	5, 9				
LGPL4/LGTA/LUPWAIT/LPBSE /LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV <sub>DD</sub>	_				
LGPL5	UPM General Purpose Line 5 / Amux	B26	0	BV <sub>DD</sub>	5, 9				
LCLK[0:2]	Local Bus Clock	F17, F16, A23	0	BV <sub>DD</sub>	_				
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV <sub>DD</sub>	_				
LSYNC_OUT	Local Bus DLL Synchronization	A21	0	BV <sub>DD</sub>	_				
DMA									
DMA1_DACK[0:1]	DMA Acknowledge	W25, U30	0	OV <sub>DD</sub>	21				
DMA2_DACK[0]	DMA Acknowledge	AA26	0	OV <sub>DD</sub>	5, 9				
DMA1_DREQ[0:1]	DMA Request	Y29, V27	I	OV <sub>DD</sub>					
DMA2_DREQ[0]	DMA Request	V29	I	OV <sub>DD</sub>					
DMA1_DDONE[0:1]	DMA Done	Y28, V30	0	OV <sub>DD</sub>	5, 9				
DMA2_DDONE[0]	DMA Done	AA28	0	OV <sub>DD</sub>	5, 9				
DMA2_DREQ[2]	DMA Request	M23	I	BV <sub>DD</sub>	_				
	Programmable Inter	rupt Controller							
UDE0	Unconditional Debug Event Processor 0	AC25	I	OV <sub>DD</sub>	_				
UDE1	Unconditional Debug Event Processor 1	AA25	Ι	OV <sub>DD</sub>					
MCP0	Machine Check Processor 0	M28	I	OV <sub>DD</sub>	—				
MCP1	Machine Check Processor 1	L28	I	OV <sub>DD</sub>					
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV <sub>DD</sub>	_				

#### Table 76. MPC8572E Pinout Listing (continued)



Table 76. MPC8572E Pinout Listing (continued)
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Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes			
MSRCID[0:1]	Memory Debug Source Port ID	U27, T29	0	OV <sub>DD</sub>	5, 9, 30			
MSRCID[2:4]	Memory Debug Source Port ID	U28, W24, W28	0	OV <sub>DD</sub>	21			
MDVAL	Memory Debug Data Valid	V26	0	OV <sub>DD</sub>	2, 21			
CLK_OUT	Clock Out	U32	0	OV <sub>DD</sub>	11			
	Clock	(						
RTC	Real Time Clock	V25	I	OV <sub>DD</sub>	—			
SYSCLK	System Clock	Y32	I	OV <sub>DD</sub>	_			
DDRCLK	DDR Clock	AA29	I	OV <sub>DD</sub>	31			
JTAG								
тск	Test Clock	T28	I	OV <sub>DD</sub>				
TDI	Test Data In	T27	I	OV <sub>DD</sub>	12			
TDO	Test Data Out	T26	0	OV <sub>DD</sub>	—			
TMS	Test Mode Select	U26	I	OV <sub>DD</sub>	12			
TRST	Test Reset	AA32	I	OV <sub>DD</sub>	12			
	DFT							
L1_TSTCLK	L1 Test Clock	V32	I	OV <sub>DD</sub>	18			
L2_TSTCLK	L2 Test Clock	V31	I	OV <sub>DD</sub>	18			
LSSD_MODE	LSSD Mode	N24	I	OV <sub>DD</sub>	18			
TEST_SEL	Test Select 0	K28	I	OV <sub>DD</sub>	18			
	Power Mana	gement						
ASLEEP	Asleep	P28	0	OV <sub>DD</sub>	9, 15, 21			



# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

# 21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio." The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

# 21.2 Power Supply Design

### 21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins  $(AV_{DD}PLAT, AV_{DD}CORE0, AV_{DD}CORE1, AV_{DD}DDR, AV_{DD}LBIU, AV_{DD}SRDS1 and AV_{DD}SRDS2 respectively).$  The AV<sub>DD</sub> level should always be equivalent to V<sub>DD</sub>, and preferably these voltages are derived directly from V<sub>DD</sub> through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 62, one to each of the  $AV_{DD}$  pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific  $AV_{DD}$  pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.



Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R <sub>N</sub>	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z <sub>0</sub>	Ω
R <sub>P</sub>	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z <sub>0</sub>	Ω

Table 85. Impedance Characteristics

**Note:** Nominal supply voltages. See Table 1,  $T_i = 105^{\circ}C$ .

# 21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform /system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

# 21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The  $\overline{\text{TRST}}$  signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires  $\overline{\text{TRST}}$  to be asserted during power-on reset flow to ensure that the JTAG boundary



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