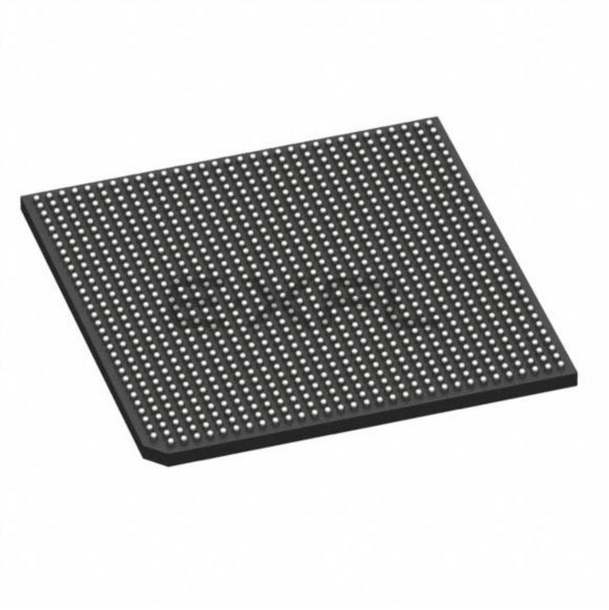

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxaulb

  - Multiplexed 32-bit address and data bus operating at up to 150 MHz
  - Eight chip selects support eight external slaves
  - Up to 8-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Three protocol engines available on a per-chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Parity support
  - Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision

Figure 1 shows the MPC8572E block diagram.

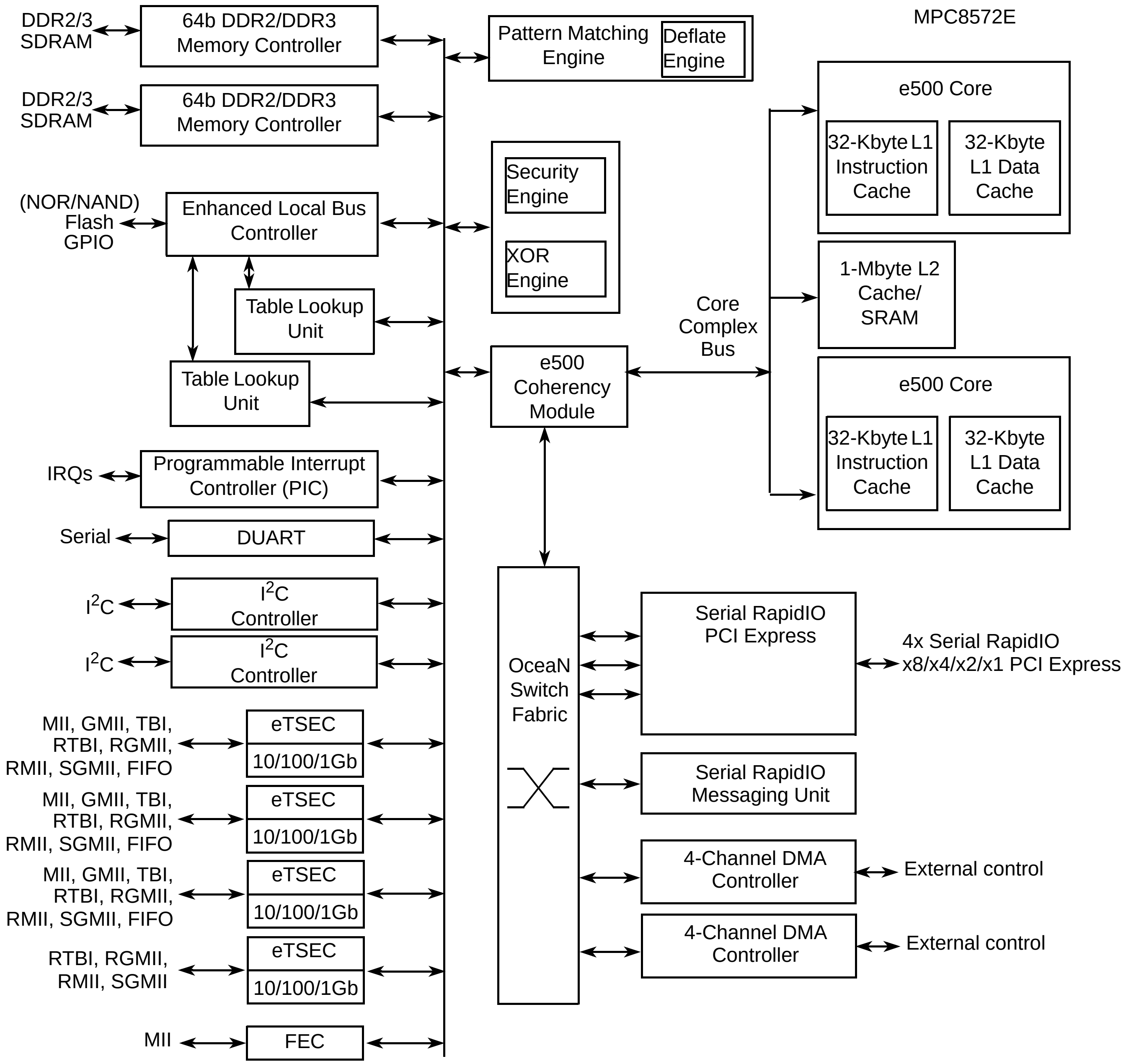


Figure 1. MPC8572E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t_{DDKHCS}	1.95	—	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
<= 667 MHz		–0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		375	—		
667 MHz		450	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	—		

Figure 4 shows the DDR2 and DDR3 SDRAM Interface output timing for the MCK to MDQS skew measurement (tDDKHMH).

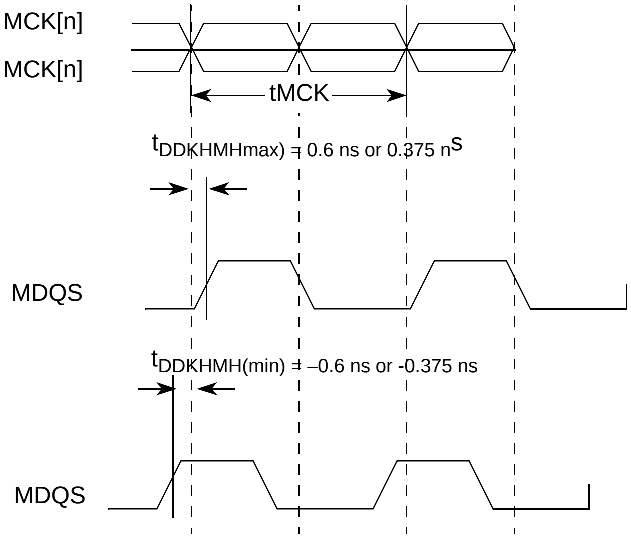


Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR2 and DDR3 SDRAM Interface output timing diagram.

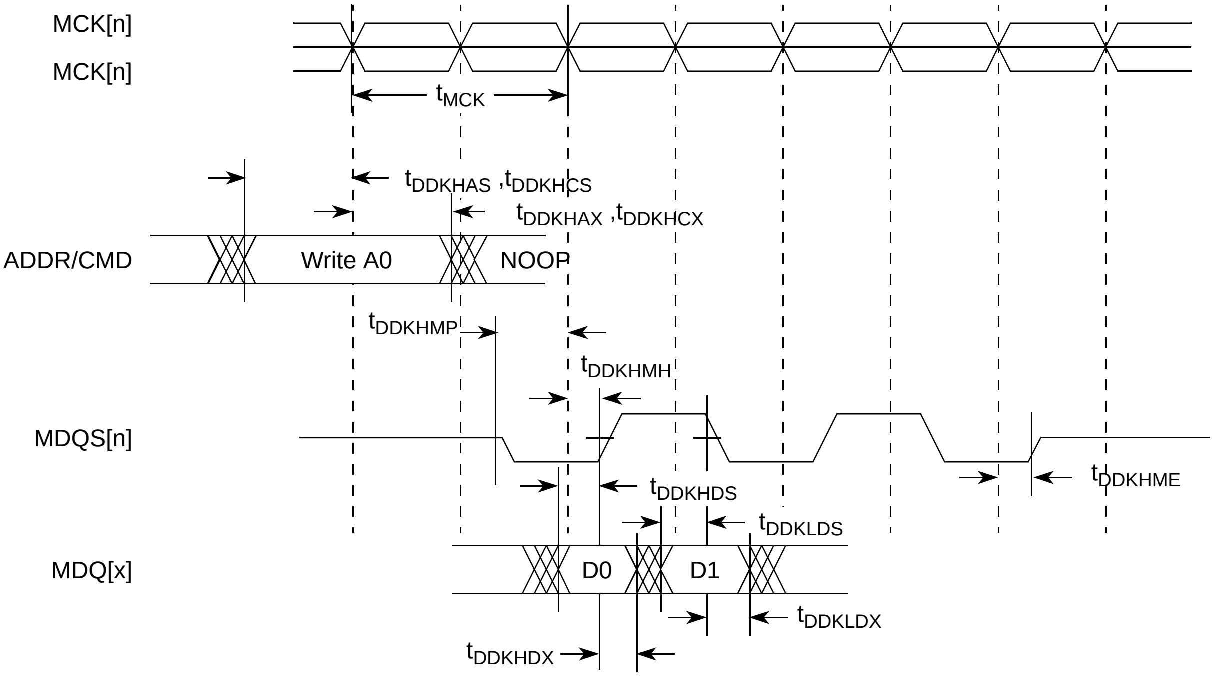


Figure 5. DDR2 and DDR3 SDRAM Interface Output Timing Diagram

Figure 12 shows the MII transmit AC timing diagram.

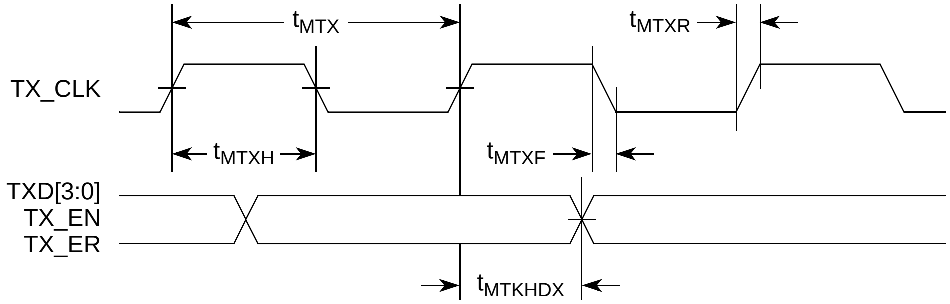


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

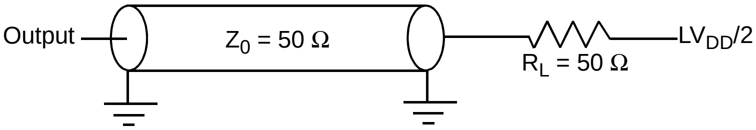


Figure 13. eTSEC AC Test Load

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 1.8 V ± 5% (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.

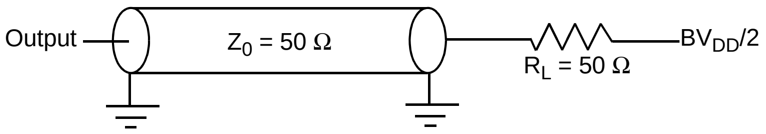


Figure 29. Local Bus AC Test Load

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data	t_{JTDVKH}	4	—		4
TMS, TDI	t_{JTIVKH}	0	—		
Input hold times:				ns	
Boundary-scan data	t_{JTDXKH}	20	—		4
TMS, TDI	t_{JTIXKH}	25	—		
Valid times:				ns	
Boundary-scan data	t_{JTKLDV}	4	20		5
TDO	t_{JTKLOV}	4	25		
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	30	—		5
TDO	t_{JTKLOX}	30	—		

6. **Differential Waveform**

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

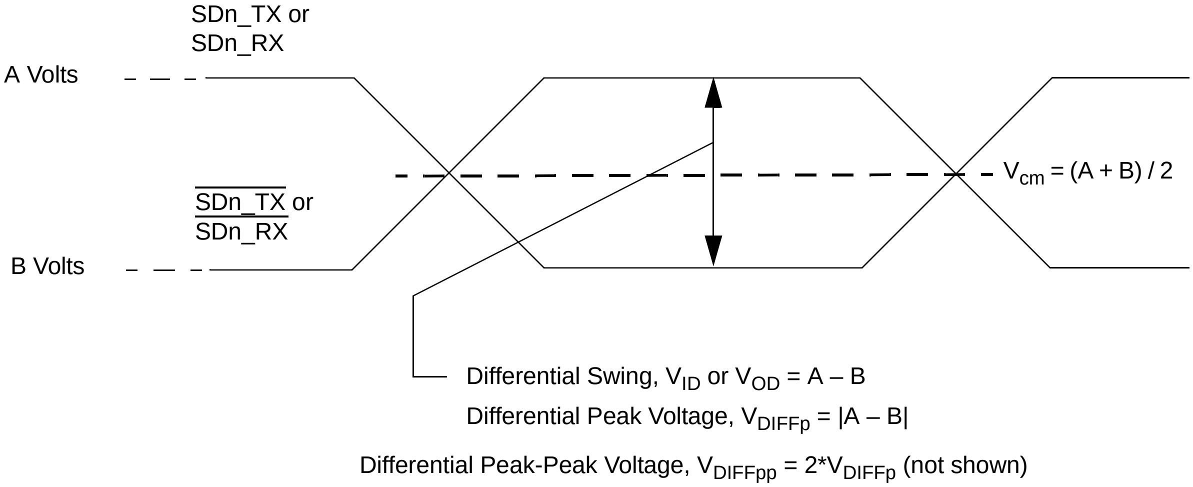


Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.

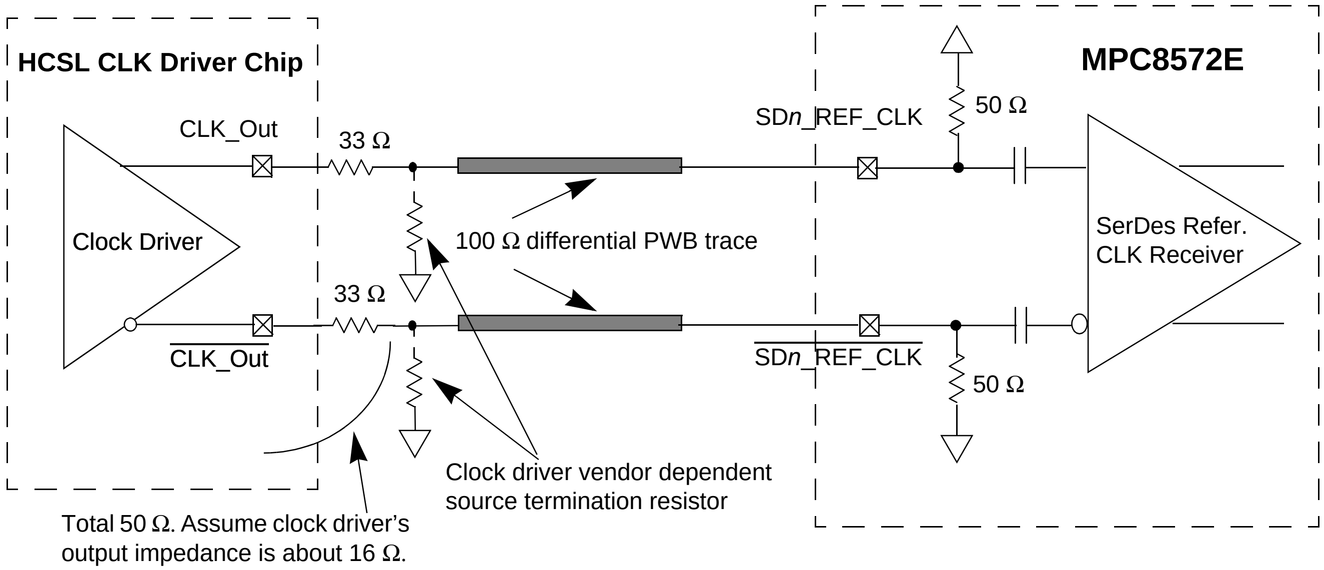


Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Table 62. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{\text{TX-DIFFp-p}}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{\text{TX-DIFFp-p}} = 2*\lvert V_{\text{TX-D+}} - V_{\text{TX-D-}}\rvert$ See Note 2.
$V_{\text{TX-DE-RATIO}}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	-4.0	dB	Ratio of the $V_{\text{TX-DIFFp-p}}$ of the second and following bits after a transition divided by the $V_{\text{TX-DIFFp-p}}$ of the first bit after a transition. See Note 2.
$T_{\text{TX-EYE}}$	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{\text{TX-MAX-JITTER}} = 1 - T_{\text{TX-EYE}} = 0.3$ UI. See Notes 2 and 3.
$T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{\text{TX-DIFFp-p}} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{\text{TX-RISE}}$, $T_{\text{TX-FALL}}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{\text{TX-CM-ACp}}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{\text{TX-CM-ACp}} = \text{RMS}(\lvert V_{\text{TXD+}} + V_{\text{TXD-}}\rvert/2 - V_{\text{TX-CM-DC}})$ $V_{\text{TX-CM-DC}} = \text{DC}_{(avg)}$ of $\lvert V_{\text{TX-D+}} + V_{\text{TX-D-}}\rvert/2$ See Note 2
$V_{\text{TX-CM-DC-ACTIVE-IDLE-DELTA}}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$\lvert V_{\text{TX-CM-DC (during L0)}} - V_{\text{TX-CM-Idle-DC (During Electrical Idle)}}\rvert <= 100$ mV $V_{\text{TX-CM-DC}} = \text{DC}_{(avg)}$ of $\lvert V_{\text{TX-D+}} + V_{\text{TX-D-}}\rvert/2$ [L0] $V_{\text{TX-CM-Idle-DC}} = \text{DC}_{(avg)}$ of $\lvert V_{\text{TX-D+}} + V_{\text{TX-D-}}\rvert/2$ [Electrical Idle] See Note 2.
$V_{\text{TX-CM-DC-LINE-DELTA}}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$\lvert V_{\text{TX-CM-DC-D+}} - V_{\text{TX-CM-DC-D-}}\rvert <= 25$ mV $V_{\text{TX-CM-DC-D+}} = \text{DC}_{(avg)}$ of $\lvert V_{\text{TX-D+}}\rvert$ $V_{\text{TX-CM-DC-D-}} = \text{DC}_{(avg)}$ of $\lvert V_{\text{TX-D-}}\rvert$ See Note 2.
$V_{\text{TX-IDLE-DIFFp}}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{\text{TX-IDLE-DIFFp}} = \lvert V_{\text{TX-IDLE-D+}} - V_{\text{TX-IDLE-D-}}\rvert <= 20$ mV See Note 2.
$V_{\text{TX-RCV-DETECT}}$	The amount of voltage change allowed during Receiver Detection		—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{crosslink}$	Crosslink Random Timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 57 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 55.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 57). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 57 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
8. MPC8572E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

16.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 55 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

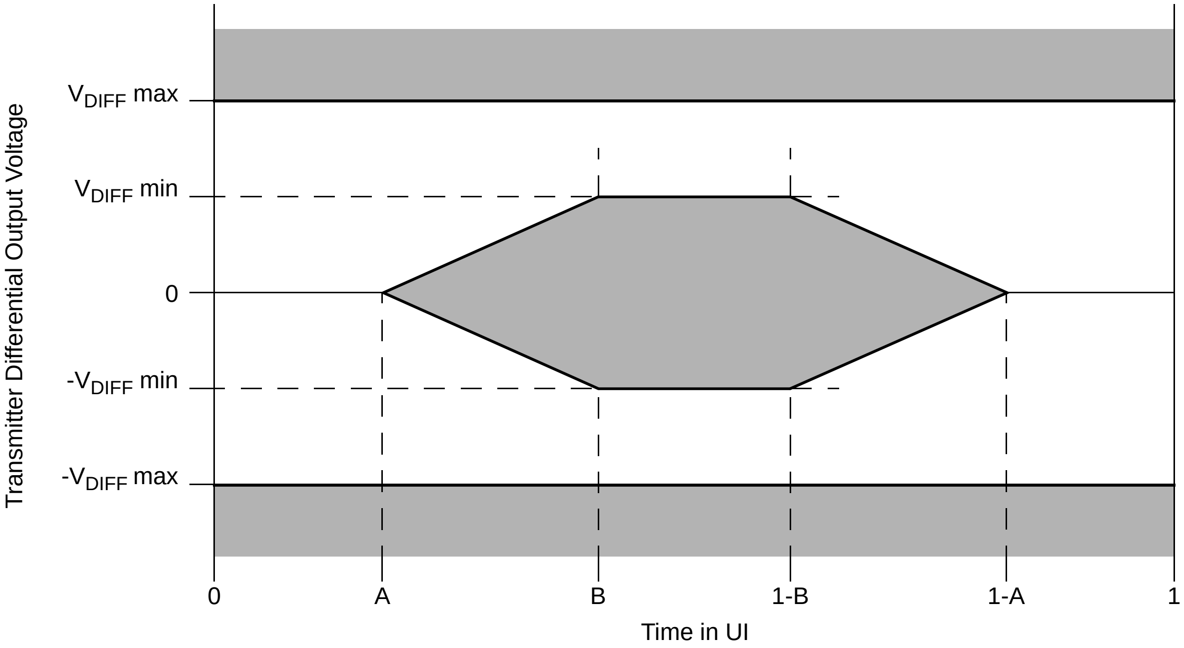


Figure 58. Transmitter Output Compliance Mask

Table 71. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

17.6 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25-Ω resistive for common mode.

5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.

18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

Table 76. MPC8572E Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MDQ[0:63]	Data	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17	I/O	GV_{DD}	—
D1_MECC[0:7]	Error Correcting Code	M10, M7, R8, T11, L12, L11, P9, R10	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	P6	I	GV_{DD}	—
D1_MAPAR_OUT	Address Parity Out	W6	O	GV_{DD}	—
D1_MDM[0:8]	Data Mask	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11	O	GV_{DD}	—
D1_MDQS[0:8]	Data Strobe	A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS}}$[0:8]	Data Strobe	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	GV_{DD}	—
D1_MA[0:15]	Address	Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7	O	GV_{DD}	—
D1_MBA[0:2]	Bank Select	AA7, AA8, R7	O	GV_{DD}	—
$\overline{\text{D1\_MWE}}$	Write Enable	AC12	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0]	Receive Data Valid	AL24	I	LV_{DD}	1
TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1]	Receive Data Error	AM29	I	LV_{DD}	1
TSEC1_TX_CLK/FIFO1_TX_CLK	Transmit Clock In	AB20	I	LV_{DD}	1
TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0]	Transmit Enable	AJ24	O	LV_{DD}	1, 22
TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1]	Transmit Error	AK25	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 2					
TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8]	Receive Data	AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20	I	LV_{DD}	1
TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8]	Transmit Data	AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18	O	LV_{DD}	1, 5, 9, 24
TSEC2_COL/FIFO2_TX_FC	Collision Detect/Flow Control	AE19	I	LV_{DD}	1
TSEC2_CRS/FIFO2_RX_FC	Carrier Sense/Flow Control	AJ20	I/O	LV_{DD}	1, 16
TSEC2_GTX_CLK	Transmit Clock Out	AE18	O	LV_{DD}	—
TSEC2_RX_CLK/FIFO2_RX_CLK	Receive Clock	AL23	I	LV_{DD}	1
TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2]	Receive Data Valid	AJ22	I	LV_{DD}	1
TSEC2_RX_ER/FIFO2_RX_ER	Receive Data Error	AD19	I	LV_{DD}	1
TSEC2_TX_CLK/FIFO2_TX_CLK	Transmit Clock In	AC19	I	LV_{DD}	1
TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2]	Transmit Enable	AB19	O	LV_{DD}	1, 22
TSEC2_TX_ER/FIFO2_TX_ERR	Transmit Error	AB17	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 3					
TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0]	Transmit Data	AG18, AG17, AH17, AH19	O	TV_{DD}	1, 5, 9
TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0]	Receive Data	AG16, AK19, AD16, AJ19	I	TV_{DD}	1

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_RX[7:0]	Receive Data (positive)	P32, N30, M32, L30, G30, F32, E30, D32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_RX}}$[7:0]	Receive Data (negative)	P31, N29, M31, L29, G29, F31, E29, D31	I	XV_{DD_SRDS1}	—
SD1_TX[7]	PCIe1 Tx Data Lane 7 / SRIO or PCIe2 Tx Data Lane 3 / PCIe3 TX Data Lane 1	M26	O	XV_{DD_SRDS1}	—
SD1_TX[6]	PCIe1 Tx Data Lane 6 / SRIO or PCIe2 Tx Data Lane 2 / PCIe3 TX Data Lane 0	L24	O	XV_{DD_SRDS1}	—
SD1_TX[5]	PCIe1 Tx Data Lane 5 / SRIO or PCIe2 Tx Data Lane 1	K26	O	XV_{DD_SRDS1}	—
SD1_TX[4]	PCIe1 Tx Data Lane 4 / SRIO or PCIe2 Tx Data Lane 0	J24	O	XV_{DD_SRDS1}	—
SD1_TX[3]	PCIe1 Tx Data Lane 3	G24	O	XV_{DD_SRDS1}	—
SD1_TX[2]	PCIe1 Tx Data Lane 2	F26	O	XV_{DD_SRDS1}	—
SD1_TX[1]	PCIe1 Tx Data Lane 1]	E24	O	XV_{DD_SRDS1}	—
SD1_TX[0]	PCIe1 Tx Data Lane 0	D26	O	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_TX}}$[7:0]	Transmit Data (negative)	M27, L25, K27, J25, G25, F27, E25, D27	O	XV_{DD_SRDS1}	—
SD1_PLL_TPD	PLL Test Point Digital	J32	O	XV_{DD_SRDS1}	17
SD1_REF_CLK	PLL Reference Clock	H32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference Clock Complement	H31	I	XV_{DD_SRDS1}	—
Reserved	—	C29, K32	—	—	26
Reserved	—	C30, K31	—	—	27
Reserved	—	C24, C25, H26, H27	—	—	28
Reserved	—	AL20, AL21	—	—	29
SerDes (x4) SGMII					
SD2_RX[3:0]	Receive Data (positive)	AK32, AJ30, AF30, AE32	I	XV_{DD_SRDS2}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD2\_RX}}$[3:0]	Receive Data (negative)	AK31, AJ29, AF29, AE31	I	XV_{DD_SRDS2}	—
SD2_TX[3]	SGMII Tx Data eTSEC4	AH26	O	XV_{DD_SRDS2}	—
SD2_TX[2]	SGMII Tx Data eTSEC3	AG24	O	XV_{DD_SRDS2}	—
SD2_TX[1]	SGMII Tx Data eTSEC2	AE24	O	XV_{DD_SRDS2}	—
SD2_TX[0]	SGMII Tx Data eTSEC1	AD26	O	XV_{DD_SRDS2}	—
$\overline{\text{SD2\_TX}}$[3:0]	Transmit Data (negative)	AH27, AG25, AE25, AD27	O	XV_{DD_SRDS2}	—
SD2_PLL_TPD	PLL Test Point Digital	AH32	O	XV_{DD_SRDS2}	17
SD2_REF_CLK	PLL Reference Clock	AG32	I	XV_{DD_SRDS2}	—
$\overline{\text{SD2\_REF\_CLK}}$	PLL Reference Clock Complement	AG31	I	XV_{DD_SRDS2}	—
Reserved	—	AF26, AF27	—	—	28
General-Purpose Input/Output					
GPINOUT[0:7]	General Purpose Input / Output	B27, A28, B31, A32, B30, A31, B28, B29	I/O	BV_{DD}	—
System Control					
$\overline{\text{HRESET}}$	Hard Reset	AC31	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	Hard Reset Request	L23	O	OV_{DD}	21
$\overline{\text{SRESET}}$	Soft Reset	P24	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN0}}$	Checkstop In Processor 0	N26	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN1}}$	Checkstop In Processor 1	N25	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT0}}$	Checkstop Out Processor 0	U29	O	OV_{DD}	2, 4
$\overline{\text{CKSTP\_OUT1}}$	Checkstop Out Processor 1	T25	O	OV_{DD}	2, 4
Debug					
TRIG_IN	Trigger In	P26	I	OV_{DD}	—
TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$	Trigger Out / Ready Processor 0/ Quiesce	P25	O	OV_{DD}	21
READY_P1	Ready Processor 1	N28	O	OV_{DD}	5, 9

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MSRCID[0:1]	Memory Debug Source Port ID	U27, T29	O	OV_{DD}	5, 9, 30
MSRCID[2:4]	Memory Debug Source Port ID	U28, W24, W28	O	OV_{DD}	21
MDVAL	Memory Debug Data Valid	V26	O	OV_{DD}	2, 21
CLK_OUT	Clock Out	U32	O	OV_{DD}	11
Clock					
RTC	Real Time Clock	V25	I	OV_{DD}	—
SYSCLK	System Clock	Y32	I	OV_{DD}	—
DDRCLK	DDR Clock	AA29	I	OV_{DD}	31
JTAG					
TCK	Test Clock	T28	I	OV_{DD}	
TDI	Test Data In	T27	I	OV_{DD}	12
TDO	Test Data Out	T26	O	OV_{DD}	—
TMS	Test Mode Select	U26	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test Reset	AA32	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 Test Clock	V32	I	OV_{DD}	18
L2_TSTCLK	L2 Test Clock	V31	I	OV_{DD}	18
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	N24	I	OV_{DD}	18
$\overline{\text{TEST\_SEL}}$	Test Select 0	K28	I	OV_{DD}	18
Power Management					
ASLEEP	Asleep	P28	O	OV_{DD}	9, 15, 21

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA\_DACK}[0:1]}$, EC5_MDC, $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$, MSRCID[2:4], MDVAL, and ASLEEP. The $\overline{\text{TEST\_SEL}}$ pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

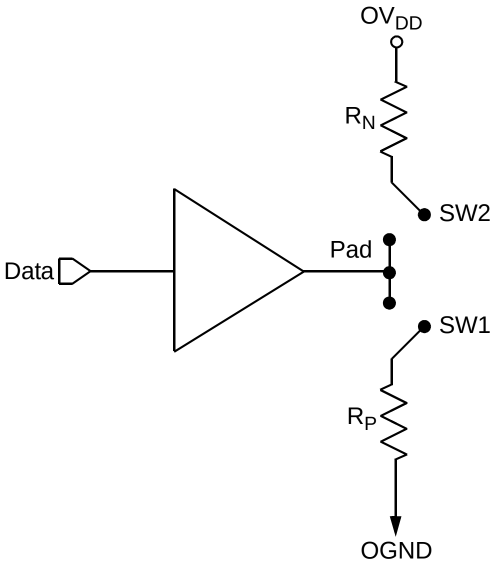


Figure 64. Driver Impedance Measurement

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

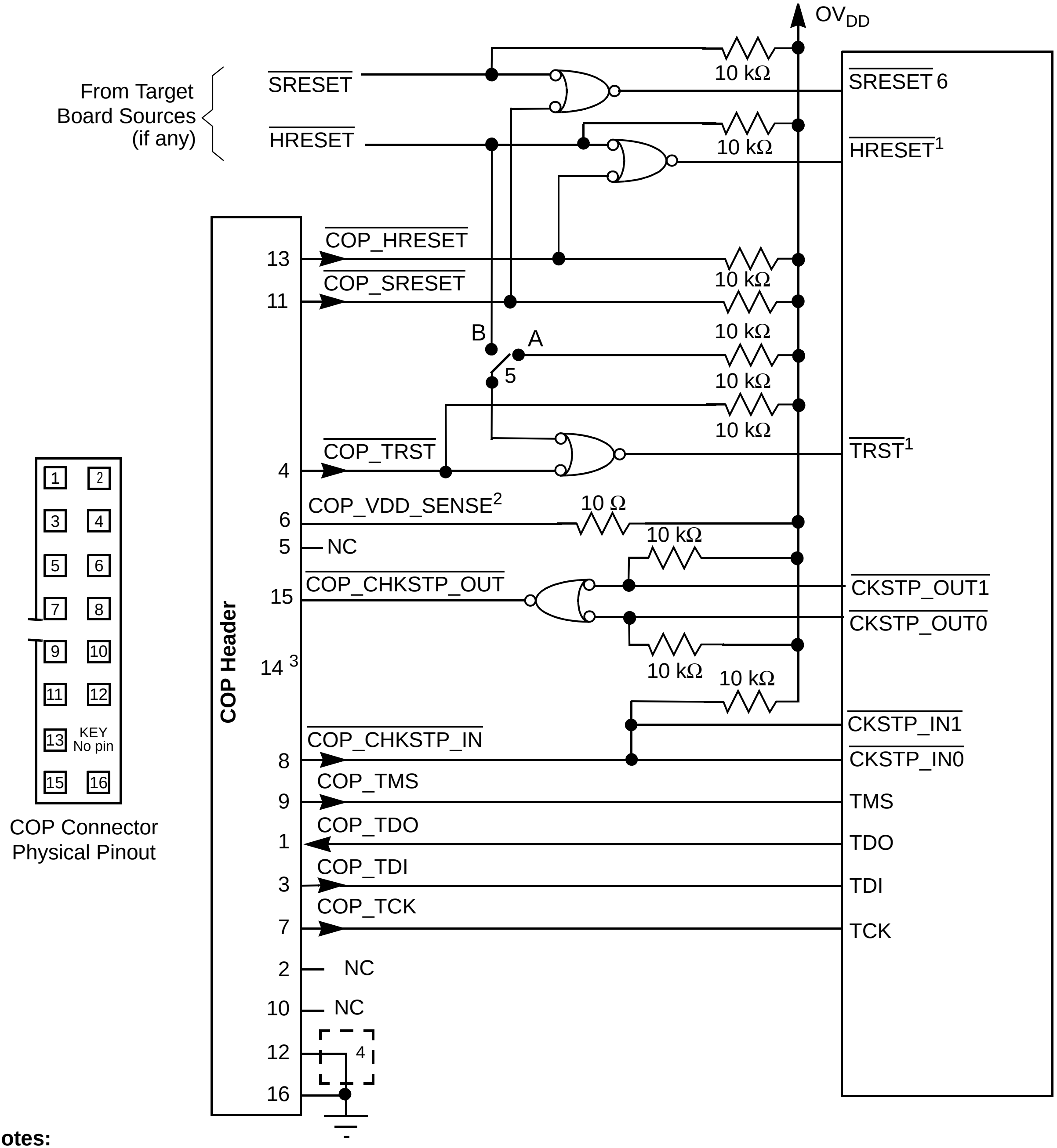
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.



Notes:

1. The COP port and target board should be able to independently assert HRESET and TRST to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 cores.