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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxauld

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- 10/100 Fast Ethernet controller (FEC) management interface
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
 - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
 - Four DMA channels per controller
 - All channels accessible by the local masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
 - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins (DMA2_DREQ[2]) is made available

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	$1.1\text{ V} \pm 55\text{ mV}$	V	—
PLL supply voltage		AV_{DD}	$1.1\text{ V} \pm 55\text{ mV}$	V	1
Core power supply for SerDes transceivers		SV_{DD}	$1.1\text{ V} \pm 55\text{ mV}$	V	—
Pad power supply for SerDes transceivers		XV_{DD}	$1.1\text{ V} \pm 55\text{ mV}$	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	$1.8\text{ V} \pm 90\text{ mV}$	V	—
	DDR3 SDRAM Interface		$1.5\text{ V} \pm 75\text{ mV}$		—
Three-speed Ethernet I/O voltage		LV_{DD}	$3.3\text{ V} \pm 165\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	4
		TV_{DD}	$3.3\text{ V} \pm 165\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$		4
DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	$3.3\text{ V} \pm 165\text{ mV}$	V	3
Local bus and GPIO I/O voltage		BV_{DD}	$3.3\text{ V} \pm 165\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$ $1.8\text{ V} \pm 90\text{ mV}$	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR2 and DDR3 SDRAM Interface reference	$MV_{REF}/1$	$GV_{DD}/2 \pm 1\%$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus and GPIO signals	BV_{IN}	GND to BV_{DD}	V	—
	Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_J	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in [Section 21.2.1, “PLL Power Supply Filtering,”](#) and not necessarily the voltage at the AV_{DD} pin, that may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN}/TV_{IN} must not exceed LV_{DD}/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Table 14 provides the current draw characteristics for MV_{REFn} .

Table 14. Current Draw Characteristics for MV_{REFn}

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for MV_{REFn}	DDR2 SDRAM	$I_{MV_{REFn}}$	—	1500	μA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for MV_{REFn} must be able to supply up to 1500 μA or 1250 μA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V $\pm$ 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≥ 667 MHz	V_{ILAC}	—	$MV_{REFn} - 0.20$	V	—
	≤ 533 MHz		—	$MV_{REFn} - 0.25$		
AC input high voltage	≥ 667 MHz	V_{IHAC}	$MV_{REFn} + 0.20$	—	V	—
	≤ 533 MHz		$MV_{REFn} + 0.25$	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V $\pm$ 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REFn} - 0.175$	V	—
AC input high voltage	V_{IHAC}	$MV_{REFn} + 0.175$	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V $\pm$ 5% for DDR2 or 1.5 V $\pm$ 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6
800 MHz		$-0.5 \times t_{MCK} - 0.375$	$-0.5 \times t_{MCK} + 0.375$		
≤ 667 MHz		$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$		
MDQS epilogue end	t_{DDKHME}			ns	6
800 MHz		-0.375	0.375		
≤ 667 MHz	t_{DDKHME}	-0.6	0.6	ns	6

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{MCK}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

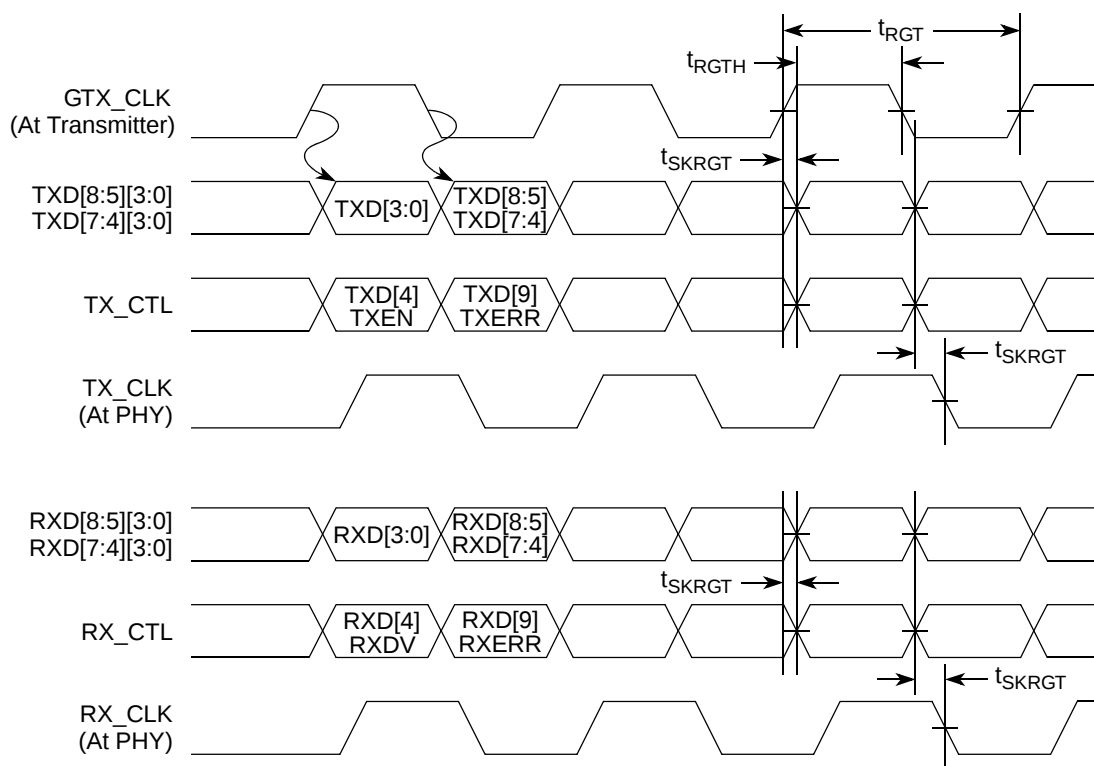


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/TV_{DD} of 2.5/ 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTE}	1.0	—	2.0	ns

Figure 30 through Figure 35 show the local bus signals.

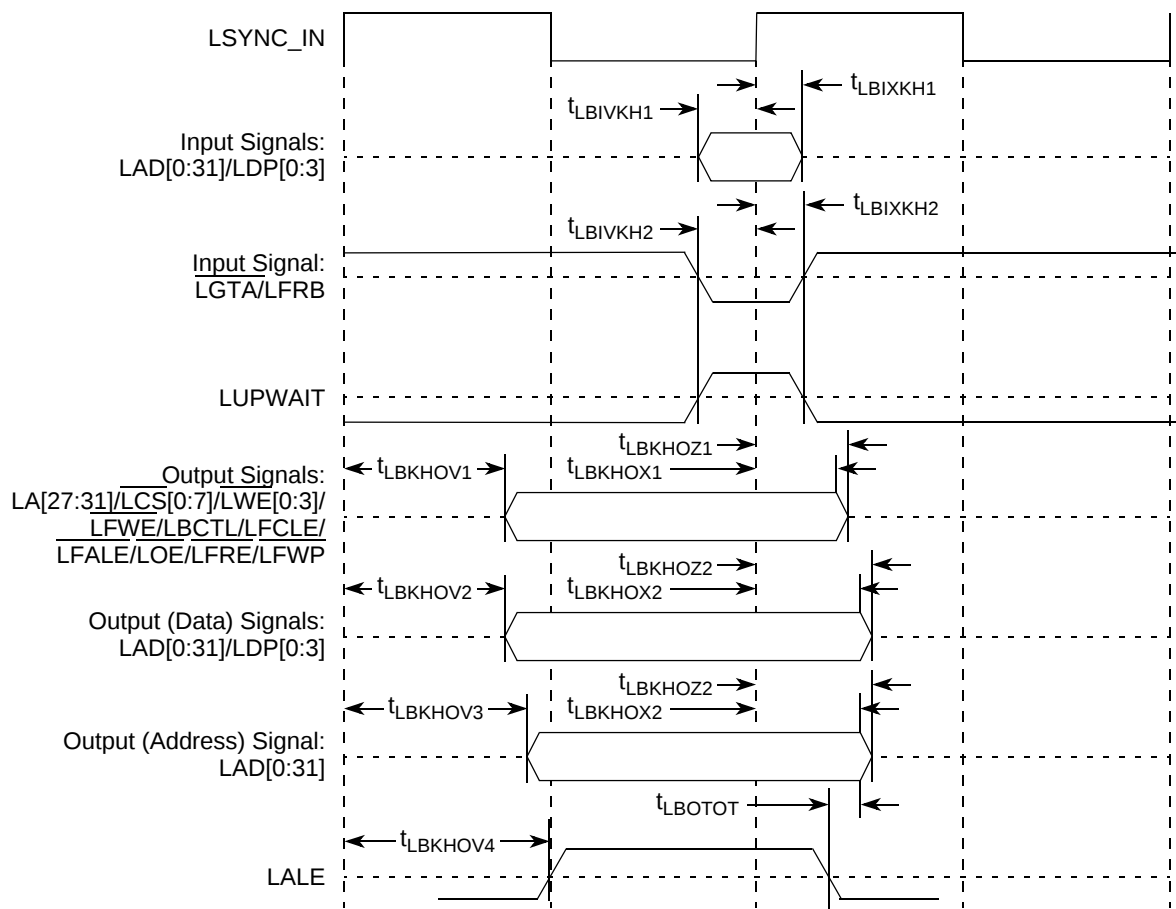


Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

Table 52 describes the general timing parameters of the local bus interface at $BV_{DD} = 3.3 \text{ V DC}$ with PLL disabled.

Table 52. Local Bus General Timing Parameters—PLL Bypassed

At recommended operating conditions with BV_{DD} of $3.3 \text{ V} \pm 5\%$

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHK1}	2.3	4.0	ns	—
Input setup to local bus clock (except LGTA/LUPWAIT)	$t_{LBIVKH1}$	5.8	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.7	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	$t_{LBIXKH1}$	-1.3	—	ns	4, 5

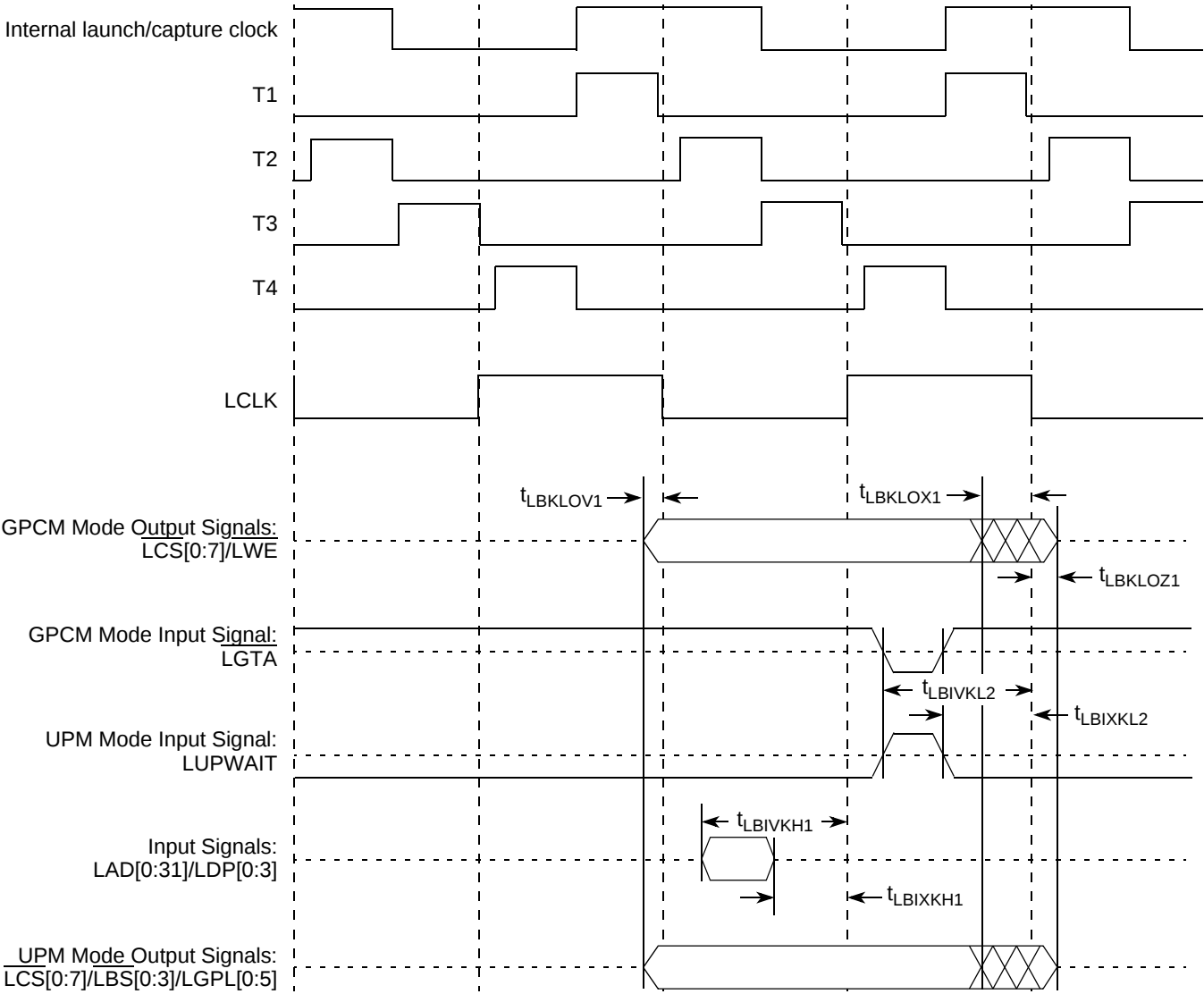


Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{SDn_TX}$) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A Volts and B Volts where $A > B$.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of $A - B$ Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |A - B|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 * |V_{OD}|$.

- To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SDn_REF_CLK}}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

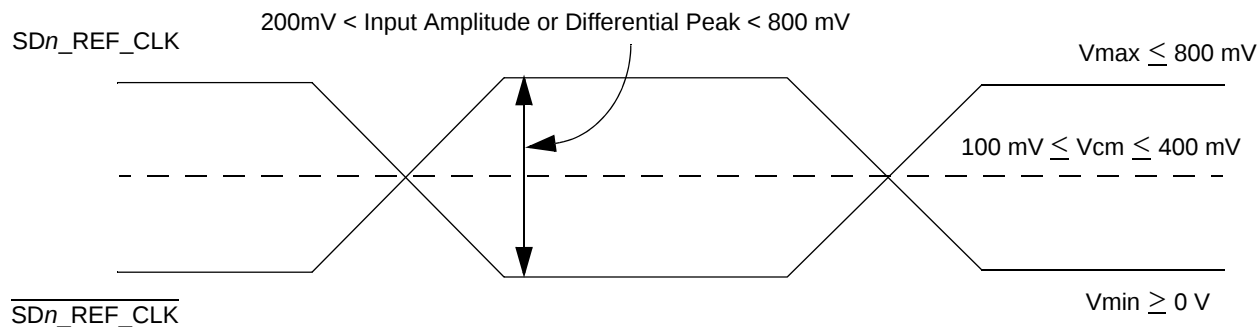


Figure 45. Differential Reference Clock Input DC Requirements (External DC-Coupled)

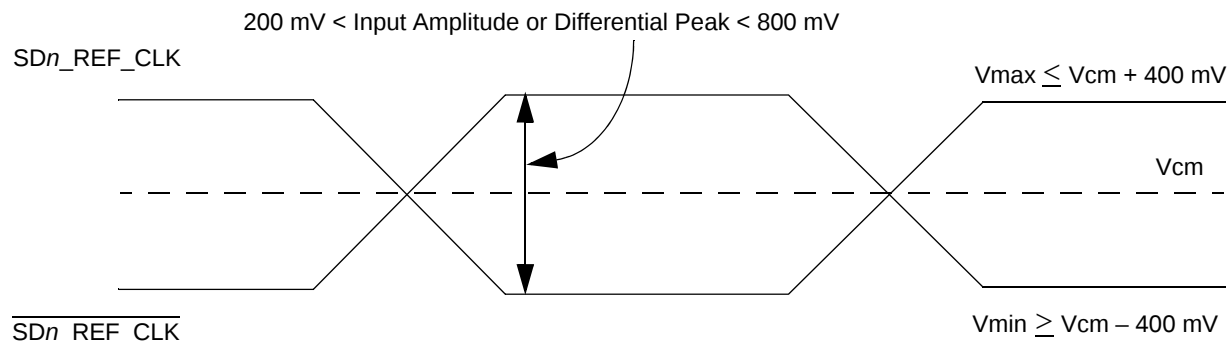


Figure 46. Differential Reference Clock Input DC Requirements (External AC-Coupled)

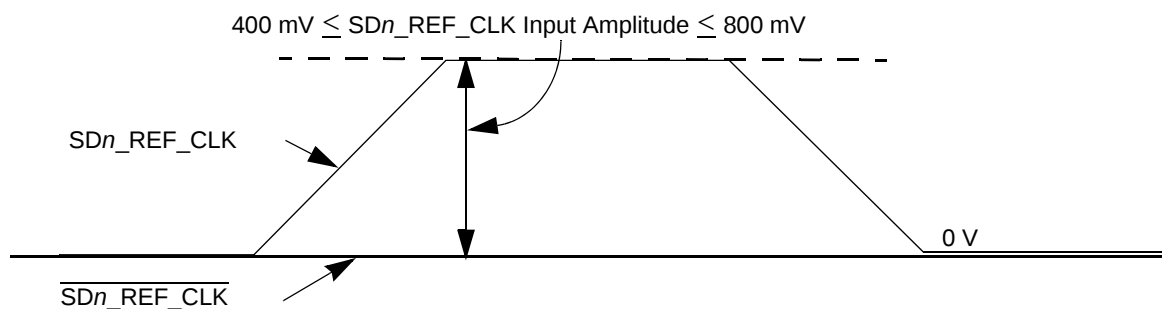


Figure 47. Single-Ended Reference Clock Input DC Requirements

Table 62. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $ See Note 2.
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} + V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$ V_{TX-CM-DC} \text{ (during L0)} - V_{TX-CM-Idle-DC} \text{ (During Electrical Idle)} \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $ V_{TX-D-} $ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection		—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

Table 74. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 59](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω (±1%) to GND	—
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	O	AVDD_S RDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	I	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	I	100Ω (±1%) to GND	—
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	O	AVDD_S RDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	—	internal diode	14
No Connection Pins					

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

Table 77. MPC8572E Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1067 MHz		1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Notes:

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) [Section 19.3, “e500 Core PLL Ratio,”](#) and [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
- The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. [Table 78](#) provides the clocking specifications for the memory bus.

This noise must be prevented from reaching other components in the MPC8572E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SV_{DD_SRDSn} and XV_{DD_SRDSn}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- μF ceramic chip capacitor from each SerDes supply (SV_{DD_SRDSn} and XV_{DD_SRDSn}) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10- μF , low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μF , low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , and GND pins of the device.

Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 85. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z_0	Ω
R_P	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z_0	Ω

Note: Nominal supply voltages. See Table 1, $T_j = 105^\circ\text{C}$.

21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 66](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in [Figure 65](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

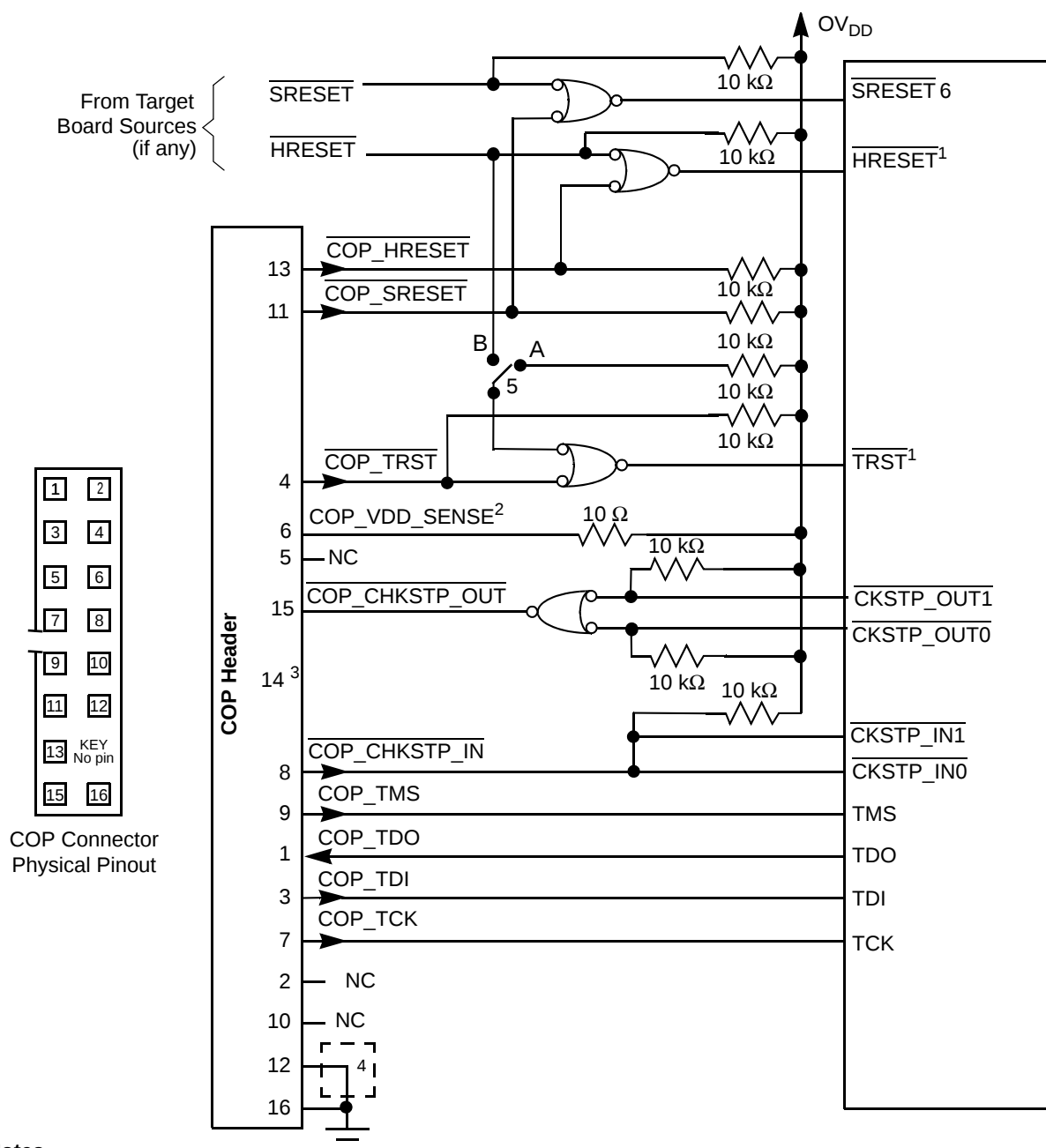
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 65](#) is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 66](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 cores.

22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 22.1, “Part Numbers Fully Addressed by this Document.”](#)

22.1 Part Numbers Fully Addressed by this Document

[Table 86](#) through [Table 88](#) provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 86. Part Numbering Nomenclature—Rev 2.2.1

MPC	nnnn	e	t	l	pp	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = –40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA ⁴ VJ = Fully Pb-free FC-PBGA ⁵	AVN = 1500-MHz processor; 800 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included
		Blank = Not included				AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included

Notes:

- ¹ MPC stands for “Qualified.”
PPC stands for “Prototype”
- ² See [Section 18, “Package Description,”](#) for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- ⁴ The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.
- ⁵ The VJ part number is entirely lead-free. This includes the C4 die bumps.