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Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxavnb

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency $\leq$ platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency $\leq$ platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

[Table 9](#) describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	2
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1

Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/ $\overline{\text{MDQS}}$ and MCK/ $\overline{\text{MCK}}$ when in DDR3 mode.

Table 20. DDR3 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V_{IN}	—	—	mV	—
DC Differential Input Voltage	V_{ID}	—	—	mV	—
AC Differential Input Voltage	V_{IDAC}	—	—	mV	—
DC Differential Output Voltage	V_{OH}	—	—	mV	—
AC Differential Output Voltage	V_{OHAC}	—	—	mV	—
AC Differential Cross-point Voltage	V_{IXAC}	—	—	mV	—
Input Midpoint Voltage	V_{MP}	—	—	mV	—

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	$OV_{\text{DD}} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current ($V_{\text{IN}}^1 = 0 \text{ V}$ or $V_{\text{IN}} = V_{\text{DD}}$)	I_{IN}	—	±5	μA
High-level output voltage ($OV_{\text{DD}} = \text{min}$, $I_{\text{OH}} = -2 \text{ mA}$)	V_{OH}	2.4	—	V
Low-level output voltage ($OV_{\text{DD}} = \text{min}$, $I_{\text{OL}} = 2 \text{ mA}$)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in [Table 24](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -4.0 \text{ mA}$)	VOH	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 4.0 \text{ mA}$)	VOL	GND	0.50	V	—
Input high voltage	VIH	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	VIL	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	40	μA	1, 2,3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-600	—	μA	3

Notes:

¹ LV_{DD} supports eTSECs 1 and 2.

² TV_{DD} supports eTSECs 3 and 4 or FEC.

³ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#).

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -1.0 \text{ mA}$)	VOH	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 1.0 \text{ mA}$)	VOL	GND - 0.3	0.40	V	—
Input high voltage	VIH	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	VIL	-0.3	0.70	V	—

Figure 9 shows the GMII transmit AC timing diagram.

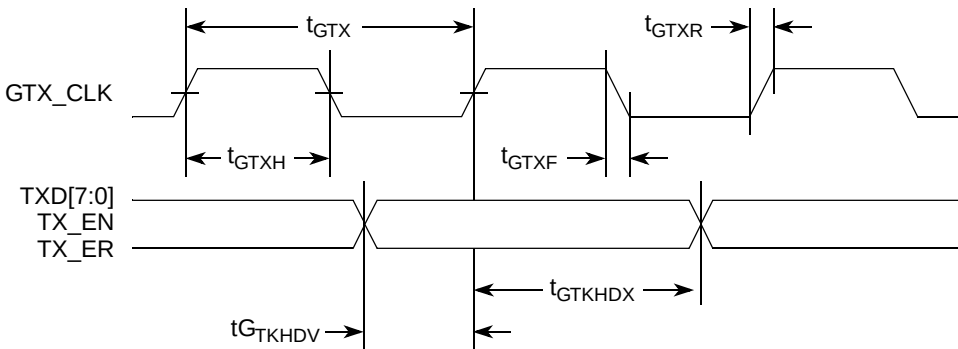


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}^2	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

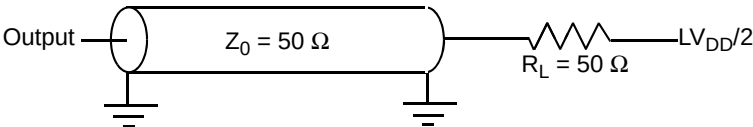


Figure 10. eTSEC AC Test Load

Figure 17 shows the TBI receive the timing diagram.

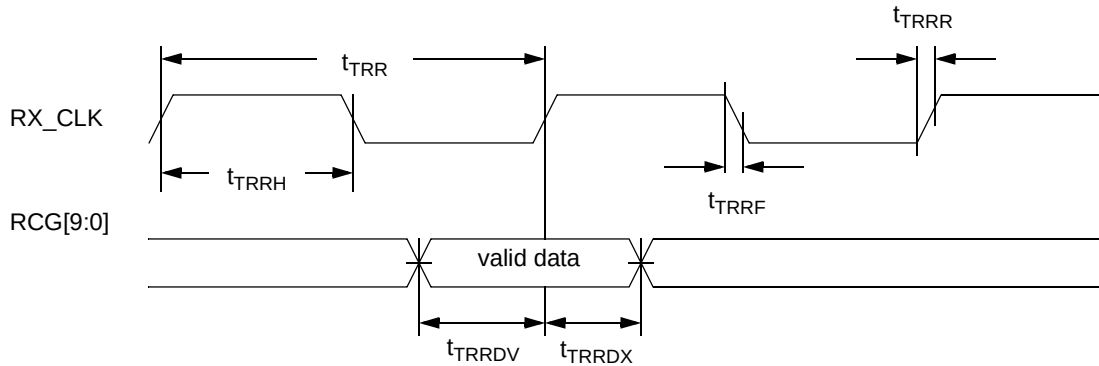


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	-500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock period ³	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 4}	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

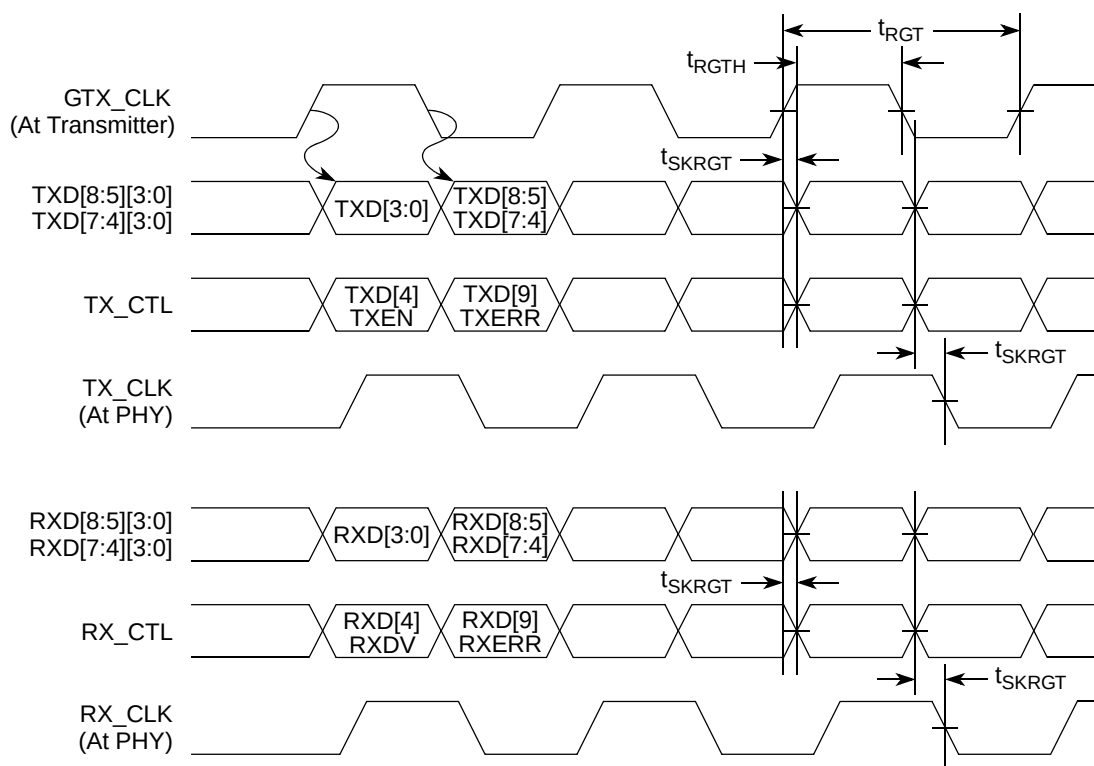


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/TV_{DD} of 2.5/ 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTE}	1.0	—	2.0	ns

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=3.3 V) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV _{DD} /TV _{DD} = Max, V _{IN} = 0.5 V)	I _{IL}	−600	—	μA	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbol referenced in [Table 1](#).

Table 44. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=2.5 V)

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.37	2.63	V	1,2
Output high voltage (LV _{DD} /TV _{DD} = Min, I _{OH} = −1.0 mA)	V _{OH}	2.00	LV _{DD} /TV _{DD} + 0.3	V	—
Output low voltage (LV _{DD} /TV _{DD} = Min, I _{OL} = 1.0 mA)	V _{OL}	GND − 0.3	0.40	V	—
Input high voltage	V _{IH}	1.70	LV _{DD} /TV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	−0.3	0.70	V	—
Input high current (V _{IN} = LV _{DD} , V _{IN} = TV _{DD})	I _{IH}	—	10	μA	1, 2,3
Input low current (V _{IN} = GND)	I _{IL}	−15	—	μA	3

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on TV_{DD}.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#).

9.2 MII Management AC Electrical Specifications

[Table 45](#) provides the MII management AC timing specifications. There are three sets of Ethernet management signals (EC1_MDC and EC1_MDIO, EC3_MDC and EC3_MDIO, EC5_MDC and EC5_MDIO). These are not explicitly shown in the table or in the figure following.

Table 45. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
ECn_MDC frequency	f _{MDC}	0.9	2.5	9.3	MHz	2, 3
ECn_MDC period	t _{MDC}	107.5	—	1120	ns	—
ECn_MDC clock pulse width high	t _{MDCH}	32	—	—	ns	—
ECn_MDC to ECn_MDIO delay	t _{MDKHDX}	10	—	16*t _{plb_clk}	ns	5

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with V_{DD}/TV_{DD} of 3.3 V $\pm$ 5% or 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
ECn_MDIO to ECn_MDC setup time	t_{MDDVKH}	5	—	—	ns	—
ECn_MDIO to ECn_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
ECn_MDC rise time	t_{MDCR}	—	—	10	ns	4
ECn_MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIIMCFG[MgmtClk] encoding selection). For example, if MIIMCFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3$ MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
- The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
- Guaranteed by design.
- t_{plb_clk} is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.

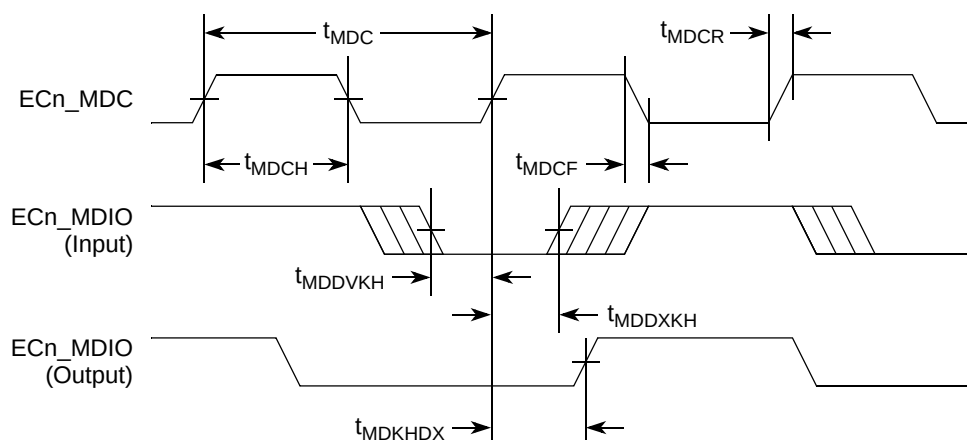


Figure 28. MII Management Interface Timing Diagram

Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)

At recommended operating conditions with BV_{DD} of 3.3 V $\pm$ 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-1.3	—	ns	4, 5
LAL output negation to high impedance for LAD/LDP (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LAL)	$t_{LBKLOV1}$	—	-0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	-0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0.0	ns	4
Local bus clock to LAL assertion	$t_{LBKLOV4}$	—	0.0	ns	4
Output hold from local bus clock (except LAD/LDP and LAL)	$t_{LBKLOX1}$	-3.3	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-3.3	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LAL)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT} .
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
- All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to 0.4 x BV_{DD} of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LAL and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of $\overline{LGTA}/LUPWAIT$ (which is captured on the rising edge of the internal clock).

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 3.3$ V DC.

Table 56. GPIO DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($BV_{IN}^1 = 0$ V or $BV_{IN} = BV_{DD}$)	I_{IN}	—	± 5	μA
High-level output voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2$ mA)	V_{OH}	$BV_{DD} - 0.2$	—	V
Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.2	V

Note:

- Note that the symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 2.5$ V DC.

Table 57. GPIO DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.7	V
Input current ($BV_{IN}^1 = 0$ V or $BV_{IN} = BV_{DD}$)	I_{IH}	—	10	μA
	I_{IL}		-15	
High-level output voltage ($BV_{DD} = \text{min}$, $I_{OH} = -1$ mA)	V_{OH}	2.0	$BV_{DD} + 0.3$	V
Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 1$ mA)	V_{OL}	GND - 0.3	0.4	V

Note:

- The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{SDn_TX}$) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A Volts and B Volts where $A > B$.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of $A - B$ Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |A - B|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 * |V_{OD}|$.

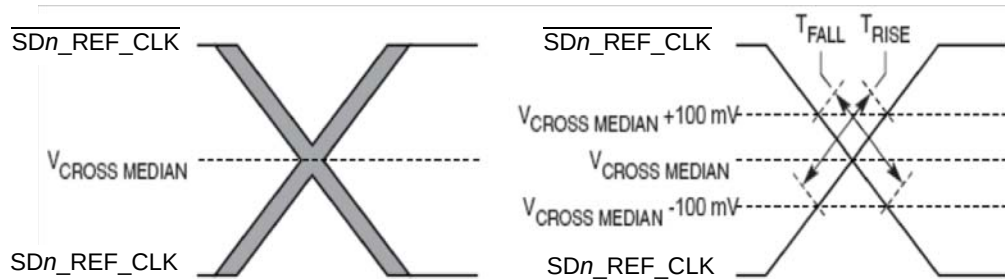


Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- [Section 8.3.2, “AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK”](#)
- [Section 16.2, “AC Requirements for PCI Express SerDes Reference Clocks”](#)
- [Section 17.2, “AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK”](#)

15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/SD1_REF_CLK are designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/SD2_REF_CLK are not to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane’s transmitter and receiver.

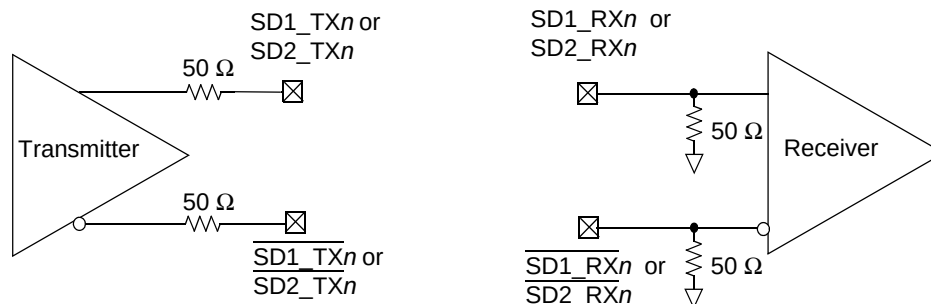


Figure 54. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- [Section 8.3, “SGMII Interface Electrical Characteristics”](#)
- [Section 16, “PCI Express”](#)

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 56](#) is specified using the passive compliance/test measurement load (see [Figure 57](#)) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 57](#)) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in [Figure 56](#)) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see [Figure 57](#)). Note that the series capacitors, CTX, are optional for the return loss measurement.

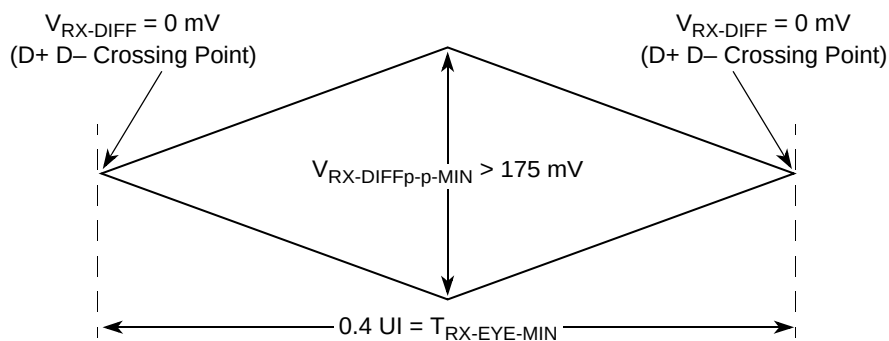


Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification

Table 66. Short Run Transmitter AC Timing Specifications—2.5 Gbaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 67. Short Run Transmitter AC Timing Specifications—3.125 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

Table 68. Long Run Transmitter AC Timing Specifications—1.25 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

18.2 Mechanical Dimensions of the MPC8572E FC-PBGA

Figure 61 shows the mechanical dimensions of the MPC8572E FC-PBGA package with full lid.

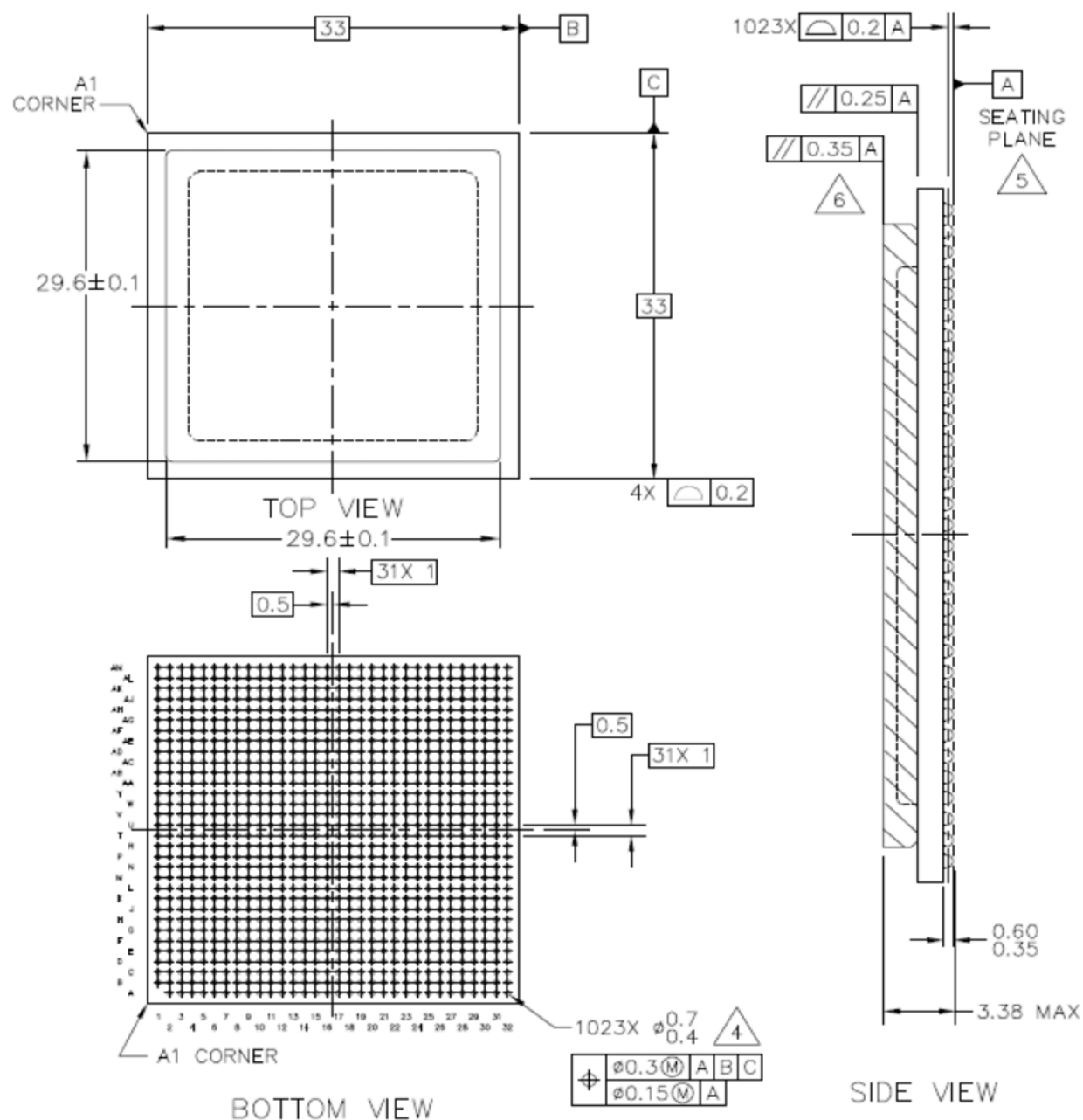


Figure 61. Mechanical Dimensions of the MPC8572E FC-PBGA with Full Lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_GTX_CLK	Transmit Clock Out	AE17	O	TV _{DD}	
TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK	Receive Clock	AF17	I	TV _{DD}	1
TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV	Receive Data Valid	AG14	I	TV _{DD}	1
TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER	Receive Error	AH15	I	TV _{DD}	1
TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK	Transmit Clock In	AF16	I	TV _{DD}	1
TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN	Transmit Enable	AJ18	O	TV _{DD}	1, 22
Three-Speed Ethernet Controller 4					
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4]	Transmit Data	AD15, AC16, AC14, AB16	O	TV _{DD}	1, 5, 9
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4]	Receive Data	AE15, AF13, AE14, AH14	I	TV _{DD}	1
TSEC4_GTX_CLK	Transmit Clock Out	AB14	O	TV _{DD}	—
TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC	Receive Clock	AG13	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC	Receive Data Valid	AD13	I/O	TV _{DD}	1, 23
TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER	Transmit Enable	AB15	O	TV _{DD}	1, 22
DUART					
UART_CTS[0:1]	Clear to Send	W30, Y27	I	OV _{DD}	—
UART_RTS[0:1]	Ready to Send	W31, Y30	O	OV _{DD}	5, 9
UART_SIN[0:1]	Receive Data	Y26, W29	I	OV _{DD}	—
UART_SOUT[0:1]	Transmit Data	Y25, W26	O	OV _{DD}	5, 9
I²C Interface					
IIC1_SCL	Serial Clock	AC30	I/O	OV _{DD}	4, 20
IIC1_SDA	Serial Data	AB30	I/O	OV _{DD}	4, 20
IIC2_SCL	Serial Clock	AD30	I/O	OV _{DD}	4, 20
IIC2_SDA	Serial Data	AD29	I/O	OV _{DD}	4, 20
SerDes (x10) PCIe, SRIO					

Table 78. Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, "CCB/SYSCLK PLL Ratio,"](#) [Section 19.3, "e500 Core PLL Ratio,"](#) and [Section 19.4, "DDR/DDRCLK PLL Ratio,"](#) for ratio settings.
- The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn_MCK}}[0:5]$ output clocks, running at half of the DDR data rate.
- In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to [Section 19.4, "DDR/DDRCLK PLL Ratio."](#) The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in [Table 80](#) and [Table 81](#);
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from [Table 79](#);
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from [Table 82](#). Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in [Table 79](#):

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

Thermal

$$V_f > 0.40 \text{ V}$$

$$V_f < 0.90 \text{ V}$$

Operating range 2–300 μA

Diode leakage < 10 nA @ 125°C

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n \frac{KT}{q} \left[\ln \frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron ($1.6 \times 10^{-19} \text{ C}$)

n = Ideality factor (normally 1.0)

K = Boltzman's constant ($1.38 \times 10^{-23} \text{ Joules/K}$)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T , the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 19.2, “CCB/SYSCLK PLL Ratio.”](#) The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 19.3, “e500 Core PLL Ratio.”](#)
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

21.2 Power Supply Design

21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CORE0} , AV_{DD_CORE1} , AV_{DD_DDR} , AV_{DD_LBIU} , AV_{DD_SRDS1} and AV_{DD_SRDS2} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 62](#), one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.

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