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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572pxavnd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

- Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
  - Supports RapidIO Interconnect Specification, Revision 1.2
  - Both 1x and 4x LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
  - Auto-detection of 1x- and 4x-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO\_READ\_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO–compliant message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox
  - Single inbound doorbell message structure
  - Facility to accept port-write messages



Table 14 provides the current draw characteristics for  $MV_{REF}n$ .

Parameter / Cond	lition	Symbol	Min	Max	Unit	Note
Current draw for MV <sub>REF</sub> n	DDR2 SDRAM	I <sub>MVREF</sub> n	—	1500	μA	1
	DDR3 SDRAM			1250		

Table 14. Current Draw Characteristics for MV<sub>REF</sub> n

1. The voltage regulator for MV<sub>RFF</sub>n must be able to supply up to 1500 μA or 1250 uA current for DDR2 or DDR3, respectively.

## 6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

### 6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

# Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%

Paramet	er	Symbol	Min	Мах	Unit	Notes
AC input low voltage	>=667 MHz	V <sub>ILAC</sub>	—	$MV_{REF}n - 0.20$	V	—
	<= 533 MHz		—	MV <sub>REF</sub> <i>n</i> -0.25		
AC input high voltage	>=667 MHz	V <sub>IHAC</sub>	$MV_{REF}n + 0.20$	—	V	—
_	<= 533 MHz		$MV_{REF}n + 0.25$	—		

### Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV<sub>DD</sub> of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V <sub>ILAC</sub>	—	MV <sub>REF</sub> <i>n</i> – 0.175	V	—
AC input high voltage	V <sub>IHAC</sub>	$MV_{REF}n + 0.175$	_	V	_



Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/ $\overline{MDQS}$  and MCK/ $\overline{MCK}$  when in DDR3 mode.

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V <sub>IN</sub>	—	_	mV	_
DC Differential Input Voltage	V <sub>ID</sub>	—	_	mV	_
AC Differential Input Voltage	V <sub>IDAC</sub>	—	_	mV	_
DC Differential Output Voltage	V <sub>OH</sub>	—	_	mV	_
AC Differential Output Voltage	V <sub>OHAC</sub>	—	_	mV	_
AC Differential Cross-point Voltage	V <sub>IXAC</sub>	—	_	mV	_
Input Midpoint Voltage	V <sub>MP</sub>	—	_	mV	

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

# 7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

 Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV <sub>DD</sub>	3.13	3.47	V
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD})$	I <sub>IN</sub>		±5	μA
High-level output voltage (OV <sub>DD</sub> = min, I <sub>OH</sub> = -2 mA)	V <sub>OH</sub>	2.4	—	V
Low-level output voltage (OV <sub>DD</sub> = min, I <sub>OL</sub> = 2 mA)	V <sub>OL</sub>		0.4	V

### Note:

1. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1.

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Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

### 8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

### Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV\_{DD}/TV\_{DD} of 2.5/ 3.3 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RX_CLK clock period	t <sub>GRX</sub>	_	8.0	_	ns
RX_CLK duty cycle	t <sub>GRXH</sub> /t <sub>GRX</sub>	40	_	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>GRDVKH</sub>	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>GRDXKH</sub>	0	_	_	ns
RX_CLK clock rise (20%-80%)	t <sub>GRXR</sub> 2	_	_	1.0	ns
RX_CLK clock fall time (80%-20%)	t <sub>GRXF</sub> 2			1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t<sub>(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>GRDVKH</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>RX</sub> clock reference (K) going to the high state (H) or setup time. Also, t<sub>GRDXKL</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>GRX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>GRX</sub> represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub></sub>

2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.



MPC8572E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 7



Figure 15 shows the TBI transmit AC timing diagram.



Figure 15. TBI Transmit AC Timing Diagram

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

### Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with LV<sub>DD</sub>/TV<sub>DD</sub> of 2.5/ 3.3 V  $\pm$  5%.

Parameter/Condition <sup>3</sup>	Symbol <sup>1</sup>	Min	Тур	Max	Unit
Clock period for TBI Receive Clock 0, 1	t <sub>TRX</sub>	_	16.0	_	ns
Skew for TBI Receive Clock 0, 1	t <sub>SKTRX</sub>	7.5	—	8.5	ns
Duty cycle for TBI Receive Clock 0, 1	t <sub>TRXH</sub> /t <sub>TRX</sub>	40	—	60	%
RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1	t <sub>TRDVKH</sub>	2.5	—	—	ns
RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1	t <sub>TRDXKH</sub>	1.5	—	—	ns
Clock rise time (20%-80%) for TBI Receive Clock 0, 1	t <sub>TRXR</sub> <sup>2</sup>	0.7	—	2.4	ns
Clock fall time (80%-20%) for TBI Receive Clock 0, 1	t <sub>TRXF</sub> <sup>2</sup>	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t<sub>(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).</sub>

2. Guaranteed by design.

3. The signals "TBI Receive Clock 0" and "TBI Receive Clock 1" refer to TSECn\_RX\_CLK and TSECn\_TX\_CLK pins respectively. These two clock signals are also referred as PMA\_RX\_CLK[0:1].



### Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Figure 16 shows the TBI receive AC timing diagram.



Figure 16. TBI Receive AC Timing Diagram

### 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV\_{DD}/TV\_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
RX_CLK clock period	t <sub>TRRX</sub>	7.5	8.0	8.5	ns
RX_CLK duty cycle	t <sub>TRRH</sub> /t <sub>TRRX</sub>	40	50	60	%
RX_CLK peak-to-peak jitter	t <sub>TRRJ</sub>	_	_	250	ps
Rise time RX_CLK (20%-80%)	t <sub>TRRR</sub>	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t <sub>TRRF</sub>	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t <sub>TRRDVKH</sub>	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t <sub>TRRDXKH</sub>	1.0		_	ns



Figure 17 shows the TBI receive the timing diagram.



Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

### 8.2.6 **RGMII and RTBI AC Timing Specifications**

Table 34 presents the RGMII and RTBI AC timing specifications.

### Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with  $\text{LV}_{\text{DD}}/\text{TV}_{\text{DD}}$  of 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
Data to clock output skew (at transmitter)	t <sub>SKRGT</sub>	-500	0	500	ps
Data to clock input skew (at receiver) <sup>2</sup>	t <sub>SKRGT</sub>	1.0	—	2.8	ns
Clock period <sup>3</sup>	t <sub>RGT</sub>	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 4</sup>	t <sub>RGTH</sub> /t <sub>RGT</sub>	40	50	60	%
Rise time (20%–80%)	t <sub>rgtr</sub>	—	—	0.75	ns
Fall time (20%–80%)	t <sub>RGTF</sub>	_	_	0.75	ns

### Notes:

- 1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t<sub>RGT</sub> represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t<sub>RGT</sub> of the lowest speed transitioned between.





Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



Local Bus Controller (eLBC)



Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)









Figure 39. Boundary-Scan Timing Diagram

# 13 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the I<sup>2</sup>C interfaces of the MPC8572E.

# 13.1 I<sup>2</sup>C DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the  $I^2C$  interfaces.

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Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V <sub>IH</sub>	$0.7  imes OV_{DD}$	OV <sub>DD</sub> + 0.3	V	—
Input low voltage level	V <sub>IL</sub>	-0.3	$0.3  imes OV_{DD}$	V	—
Low level output voltage	V <sub>OL</sub>	0	0.4	V	1
Pulse width of spikes which must be suppressed by the input filter	t <sub>I2KHKL</sub>	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1\times OV_{DD}$ and $0.9\times OV_{DD}(max)$	I	-10	10	μA	3



High-Speed Serial Interfaces (HSSI)

SD1\_REF\_CLK for PCI Express and Serial RapidIO, or SD2\_REF\_CLK and SD2\_REF\_CLK for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

## **15.2.1 SerDes Reference Clock Receiver Characteristics**

Figure 44 shows a receiver reference diagram of the SerDes reference clocks. Characteristics are as follows:

- The supply voltage requirements for  $XV_{DD SRDS2}$  are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SDn\_REF\_CLK and SDn\_REF\_CLK are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SDn\_REF\_CLK or SDn\_REF\_CLK) has on-chip 50-Ω termination to SGND\_SRDSn (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND\_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*\_REF\_CLK and  $\overline{\text{SD}n_\text{REF}\text{-}\text{CLK}}$  inputs cannot drive 50  $\Omega$  to SGND\_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.



## 15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND\_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

### NOTE

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.



Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features  $50-\Omega$  termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is  $50\Omega$ . R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from  $140\Omega$  to  $240\Omega$  depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's  $50-\Omega$  termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 =  $25\Omega$ . Consult



Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
T <sub>crosslink</sub>	Crosslink Random Timeout	0	_	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

### Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 57 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 55.)
- 3. A T<sub>TX-EYE</sub> = 0.70 UI provides for a total sum of deterministic and random jitter budget of T<sub>TX-JITTER-MAX</sub> = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The T<sub>TX-EYE-MEDIAN-to-MAX-JITTER</sub> median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 57). Note that the series capacitors C<sub>TX</sub> is optional for the return loss measurement.
- 5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 57 for both V<sub>TX-D+</sub> and V<sub>TX-D-</sub>.
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
- 8. MPC8572E SerDes transmitter does not have C<sub>TX</sub> built-in. An external AC Coupling capacitor is required.

### 16.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 55 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

### NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).



Serial RapidIO

# 17.1 <u>DC Requirements</u> for Serial RapidIO SD1\_REF\_CLK and SD1\_REF\_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

# 17.2 <u>AC Requirements</u> for Serial RapidIO SD1\_REF\_CLK and SD1\_REF\_CLK

Figure 64lists the AC requirements.

Table 64. SD <i>n</i> _	_REF_CL	K and SD <i>n</i> _	_REF_0	CLK AC	Requirements

Symbol	Parameter Description	Min	Typical	Мах	Units	Comments
t <sub>REF</sub>	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t <sub>REFCJ</sub>	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	_	—	80	ps	_
t <sub>REFPJ</sub>	Phase jitter. Deviation in edge location with respect to mean edge location	-40	-	40	ps	_

# 17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

# 17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.





# 17.5 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- -10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$  for  $625 \text{ MHz} \le \text{Freq}(f) \le \text{Baud}$  Frequency

The reference impedance for the differential return loss measurements is  $100 \Omega$  resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Characteristic	Symbol	Range		Unit	Notos	
Gharacteristic	Min Max		Мах	Onic	NOLES	
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair	
Differential Output Voltage	V <sub>DIFFPP</sub>	500	1000	mV p-p	_	
Deterministic Jitter	J <sub>D</sub>	—	0.17	UI p-p	—	
Total Jitter	J <sub>T</sub>	—	0.35	UI p-p	—	
Multiple output skew	S <sub>MO</sub>	—	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit Interval	UI	800	800	ps	+/- 100 ppm	

### Table 65. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notes	
	Symbol	Min	Max	Onic		
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair	
Differential Output Voltage	V <sub>DIFFPP</sub>	500	1000	mV p-p	—	
Deterministic Jitter	J <sub>D</sub>	—	0.17	UI p-p	—	
Total Jitter	J <sub>T</sub>	—	0.35	UI p-p	_	



Serial RapidIO



Figure 60. Receiver Input Compliance Mask

Table 75.	Receiver Ir	nput Compliance	Mask Parameters	Exclusive of	of Sinusoidal Jitte
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Receiver Type	V <sub>DIFF</sub> min (mV)	V <sub>DIFF</sub> max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

# 17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

# 17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial



Table 76	MPC8572E	Pinout I	istina (	(continued)	`
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Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_RX[7:0]	Receive Data (positive)	P32, N30, M32, L30, G30, F32, E30, D32	I	XV <sub>DD_SR</sub> DS1	_
SD1_RX[7:0]	Receive Data (negative)	P31, N29, M31, L29, G29, F31, E29, D31	I	XV <sub>DD_SR</sub> DS1	_
SD1_TX[7]	PCIe1 Tx Data Lane 7 / SRIO or PCIe2 Tx Data Lane 3 / PCIe3 TX Data Lane 1	M26	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[6]	PCIe1 Tx Data Lane 6 / SRIO or PCIe2 Tx Data Lane 2 / PCIe3 TX Data Lane 0	L24	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[5]	PCIe1 Tx Data Lane 5 / SRIO or PCIe2 Tx Data Lane 1	K26	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[4]	PCIe1 Tx Data Lane 4 / SRIO or PCIe2 Tx Data Lane 0	J24	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[3]	PCIe1 Tx Data Lane 3	G24	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[2]	PCIe1 Tx Data Lane 2	F26	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[1]	PCIe1 Tx Data Lane 1]	E24	0	XV <sub>DD_SR</sub> DS1	—
SD1_TX[0]	PCIe1 Tx Data Lane 0	D26	0	XV <sub>DD_SR</sub> DS1	_
SD1_TX[7:0]	Transmit Data (negative)	M27, L25, K27, J25, G25, F27, E25, D27	0	XV <sub>DD_SR</sub> DS1	_
SD1_PLL_TPD	PLL Test Point Digital	J32	0	XV <sub>DD_SR</sub> DS1	17
SD1_REF_CLK	PLL Reference Clock	H32	I	XV <sub>DD_SR</sub> DS1	_
SD1_REF_CLK	PLL Reference Clock Complement	H31	I	XV <sub>DD_SR</sub> DS1	_
Reserved	—	C29, K32	_	—	26
Reserved	—	C30, K31		—	27
Reserved	—	C24, C25, H26, H27	_	—	28
Reserved	_	AL20, AL21		—	29
	SerDes (x4)	SGMII			
SD2_RX[3:0]	Receive Data (positive)	AK32, AJ30, AF30, AE32	Ι	XV <sub>DD_SR</sub> DS2	—



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS1	SerDes Transceiver Core Logic GND (xcorevss)	C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32	_	_	_
SGND_SRDS2	SerDes Transceiver Core Logic GND (xcorevss)	AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32	_	_	_
AGND_SRDS1	SerDes PLL GND	J31		—	
AGND_SRDS2	SerDes PLL GND	AH31	_	—	_
OVDD	General I/O Supply	U31, V24, V28, Y31, AA27, AB25, AB29	_	OVDD	_
LVDD	TSEC 1&2 I/O Supply	AC18, AC21, AG21, AL27	_	LVDD	_
TVDD	TSEC 3&4 I/O Supply	AC15, AE16, AH18		TVDD	
GVDD	SSTL_1.8 DDR Supply	B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2		GVDD	
BVDD	Local Bus and GPIO Supply	A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20	—	BVDD	—



System Design Information

# 21.10.3 SerDes 2 Interface (SGMII) Entirely Unused

If the high-speed SerDes 2 interface (SGMII) is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2\_TX[3:0]
- <u>SD2\_TX[3:0]</u>
- Reserved pins: AF26, AF27

The following pins must be connected to XGND\_SRDS2:

- SD2\_RX[3:0]
- $\overline{\text{SD2}_RX}[3:0]$
- SD2\_REF\_CLK
- SD2\_REF\_CLK

The POR configuration pin cfg\_srds\_sgmii\_en on UART\_RTS[1] can be used to power down SerDes 2 block for power saving. Note that both SVDD\_SRDS2 and XVDD\_SRDS2 must remain powered.

# 21.10.4 SerDes 2 Interface (SGMII) Partly Unused

If only part of the high speed SerDes 2 interface (SGMII) pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2\_TX[3:0]
- <u>SD2\_TX[3:0]</u>
- Reserved pins: AF26, AF27

The following pins must be connected to XGND\_SRDS2:

- SD2\_RX[3:0]
- <u>SD2\_RX</u>[3:0]