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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572vtatlb

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- 10/100 Fast Ethernet controller (FEC) management interface
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
 - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
 - Four DMA channels per controller
 - All channels accessible by the local masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
 - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins (DMA2_DREQ[2]) is made available

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Range	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface	—	–0.3 to 1.65	—	—
Three-speed Ethernet I/O, FEC management interface, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2)	–0.3 to 3.63 –0.3 to 2.75	V	2
		TV_{DD} (for eTSEC3 and eTSEC4, FEC)	–0.3 to 3.63 –0.3 to 2.75	—	2
DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus and GPIO I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV_{IN}	–0.3 to ($GV_{DD} + 0.3$)	V	3
	DDR2 and DDR3 SDRAM interface reference	MV_{REF}^n	–0.3 to ($GV_{DD}/2 + 0.3$)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to ($LV_{DD} + 0.3$) –0.3 to ($TV_{DD} + 0.3$)	V	3
	Local bus and GPIO signals	BV_{IN}	–0.3 to ($BV_{DD} + 0.3$)	—	—
	DUART, SYSCCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	–0.3 to ($OV_{DD} + 0.3$)	V	3
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

- Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
- (M,L,O) V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$	1
	45(default) 45(default) 125	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$ $BV_{DD} = 1.8\text{ V}$	
DDR2 signal	18 36 (half strength mode)	$GV_{DD} = 1.8\text{ V}$	2
DDR3 signal	20 40 (half strength mode)	$GV_{DD} = 1.5\text{ V}$	2
eTSEC/10/100 signals	45	$L/TV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, JTAG	45	$OV_{DD} = 3.3\text{ V}$	—
I2C	150	$OV_{DD} = 3.3\text{ V}$	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j = 105^\circ\text{C}$ and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD} , AV_{DD-n} , BV_{DD} , LV_{DD} , OV_{DD} , SV_{DD_SRDS1} and SV_{DD_SRDS2} , TV_{DD} , XV_{DD_SRDS1} and XV_{DD_SRDS2}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for GV_{DD} is not required.

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KH}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) and [Section 19.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver.
Peak-to-peak noise on MV_{REFn} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to MV_{REFn} . This rail should track variations in the DC level of MV_{REFn} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for $GV_{DD}(typ) = 1.5\text{ V}$

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	MV_{REFn}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
Input high voltage	V_{IH}	$MV_{REFn} + 0.100$	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REFn} - 0.100$	V	—
Output leakage current	I_{OZ}	–50	50	μA	3

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver.
Peak-to-peak noise on MV_{REFn} may not exceed $\pm 1\%$ of the DC value.
3. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for $GV_{DD}(typ)=1.8\text{ V}$ and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$ (for DDR2), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. $GV_{DD} = 1.5\text{ V} \pm 0.075\text{ V}$ (for DDR3), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.175 V.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}[n]$) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2_RX}}[n]$) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XV_{DD_SRDS2} = 1.1V \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	1
V _{OD} fall time (80%-20%)	t _{fall}	50	—	120	ps	—
V _{OD} rise time (20%-80%)	t _{rise}	50	—	120	ps	—

Notes:

- Each UI is 800 ps $\pm$ 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XV_{DD_SRDS2} = 1.1V \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10 ⁻¹²	—	—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C _{TX}	5	—	200	nF	3

Notes:

- Measured at receiver.
- Each UI is 800 ps $\pm$ 100 ppm.
- The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
- See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

Table 49. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%. (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
8. Guaranteed by design.

Table 50 describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V DC.

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 2.5 V ± 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	6.67	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.9	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.4	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	6.67	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.

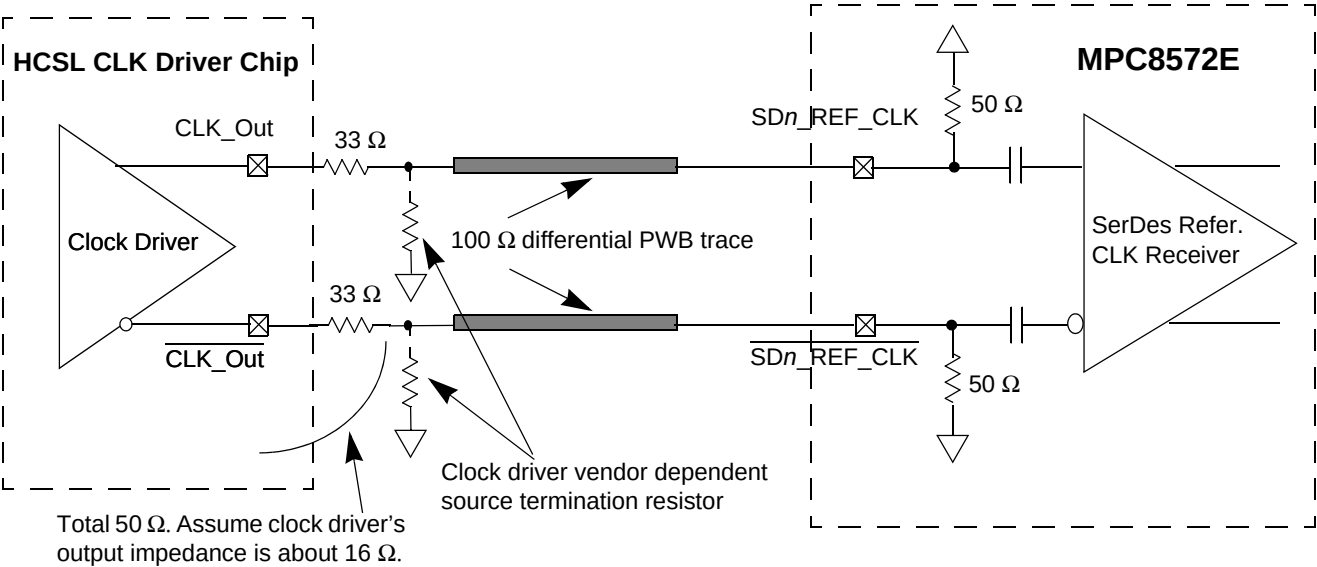


Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

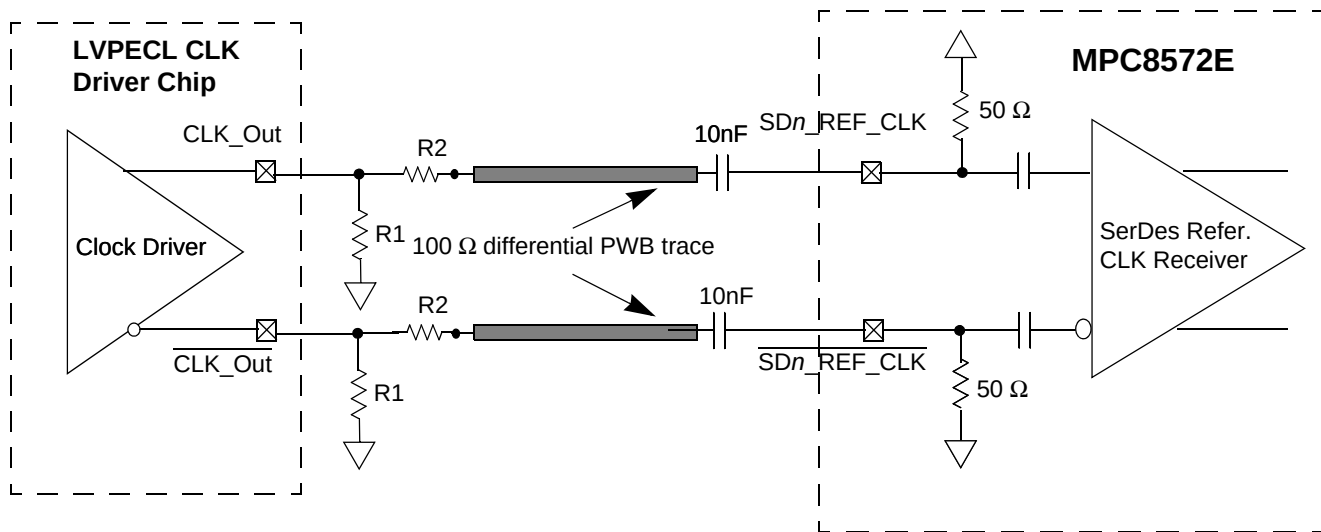


Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

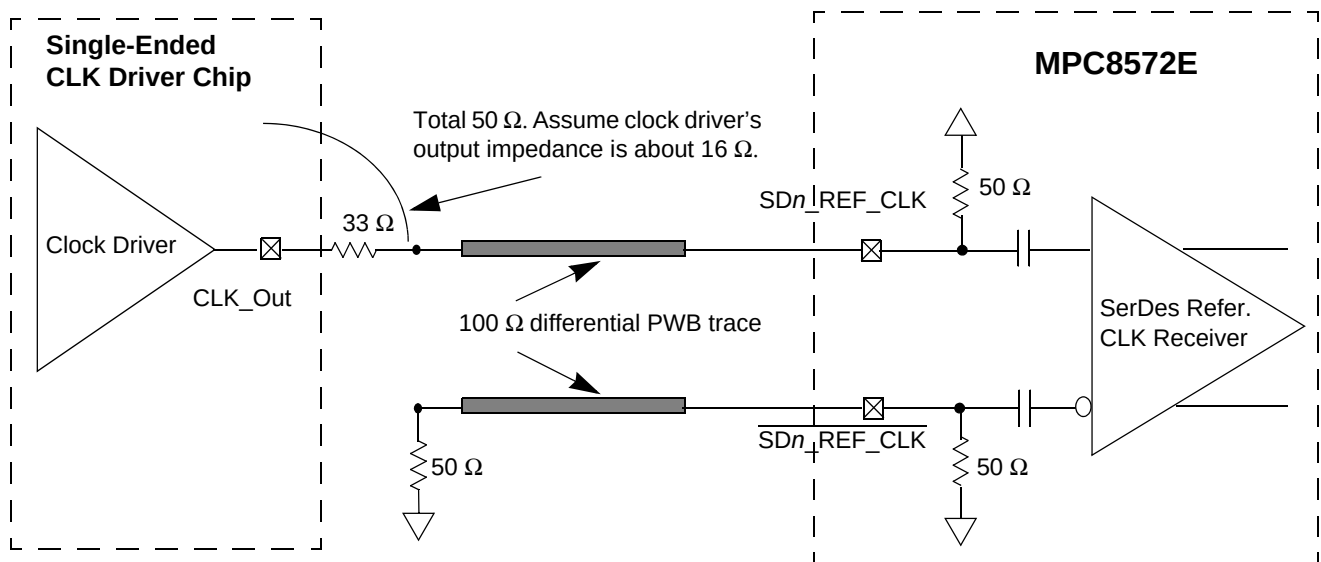


Figure 51. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

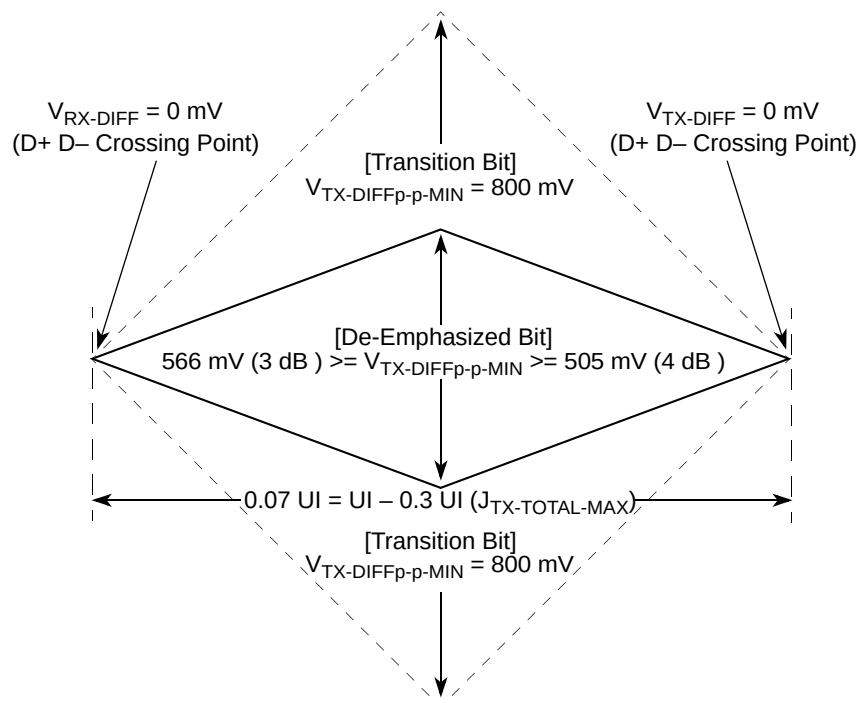


Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications

16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 63. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 56](#) is specified using the passive compliance/test measurement load (see [Figure 57](#)) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 57](#)) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in [Figure 56](#)) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see [Figure 57](#)). Note that the series capacitors, CTX, are optional for the return loss measurement.

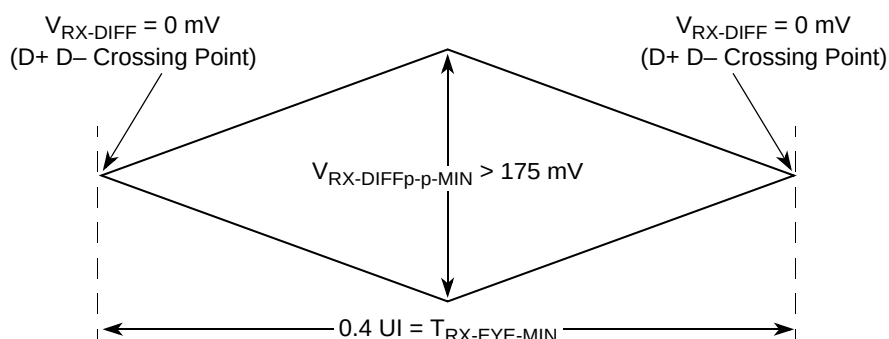


Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see [Section 15.2, “SerDes Reference Clocks.”](#)

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64 lists the AC requirements.

Table 64. SD_n_REF_CLK and $\overline{\text{SD}}_n$ _REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in [Section 8.1, “Enhanced Three-Speed Ethernet Controller \(eTSEC\) \(10/100/1000 Mbps\)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.”](#) The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Table 66. Short Run Transmitter AC Timing Specifications—2.5 Gbaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 67. Short Run Transmitter AC Timing Specifications—3.125 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

Table 68. Long Run Transmitter AC Timing Specifications—1.25 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

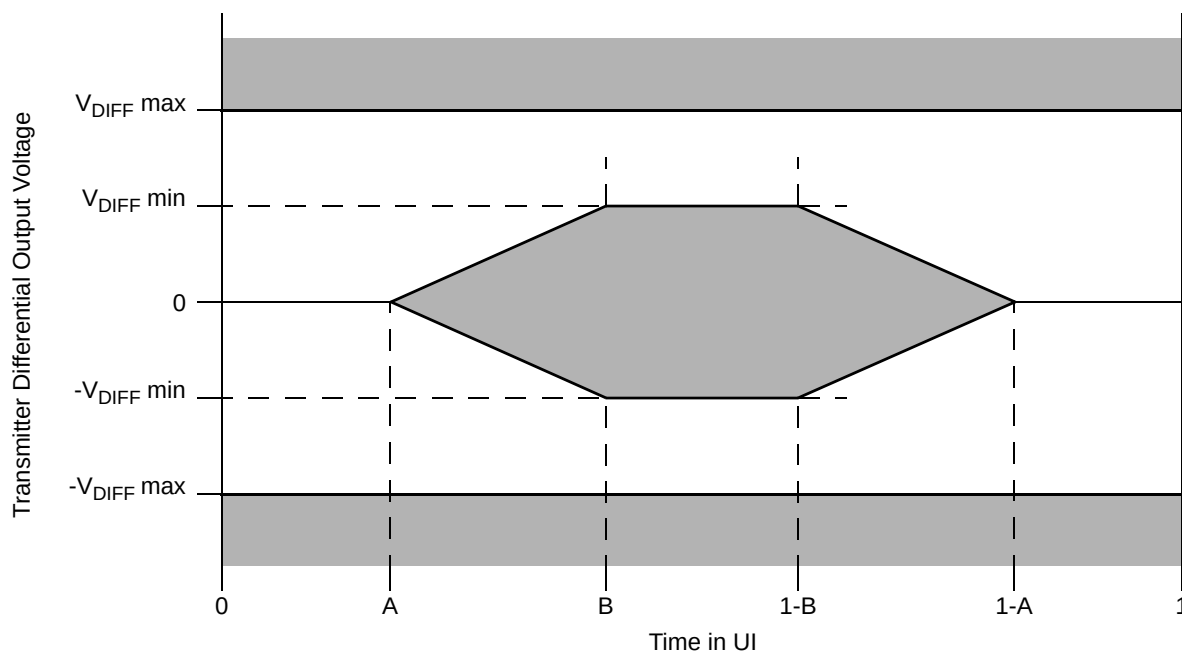


Figure 58. Transmitter Output Compliance Mask

Table 71. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V _{DIFFmin} (mV)	V _{DIFFmax} (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

17.6 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times (\text{Baud Frequency})$. This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25-Ω resistive for common mode.

Table 74. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 59](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV/FIFO1_RX_D V/FIFO1_RXC[0]	Receive Data Valid	AL24	I	LV _{DD}	1
TSEC1_RX_ER/FIFO1_RX_E R/FIFO1_RXC[1]	Receive Data Error	AM29	I	LV _{DD}	1
TSEC1_TX_CLK/FIFO1_TX_C LK	Transmit Clock In	AB20	I	LV _{DD}	1
TSEC1_TX_EN/FIFO1_TX_EN /FIFO1_TXC[0]	Transmit Enable	AJ24	O	LV _{DD}	1, 22
TSEC1_TX_ER/FIFO1_TX_ER R/FIFO1_TXC[1]	Transmit Error	AK25	O	LV _{DD}	1, 5, 9
Three-Speed Ethernet Controller 2					
TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8]	Receive Data	AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20	I	LV _{DD}	1
TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8]	Transmit Data	AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18	O	LV _{DD}	1, 5, 9, 24
TSEC2_COL/FIFO2_TX_FC	Collision Detect/Flow Control	AE19	I	LV _{DD}	1
TSEC2_CRS/FIFO2_RX_FC	Carrier Sense/Flow Control	AJ20	I/O	LV _{DD}	1, 16
TSEC2_GTX_CLK	Transmit Clock Out	AE18	O	LV _{DD}	—
TSEC2_RX_CLK/FIFO2_RX_C LK	Receive Clock	AL23	I	LV _{DD}	1
TSEC2_RX_DV/FIFO2_RX_D V/FIFO1_RXC[2]	Receive Data Valid	AJ22	I	LV _{DD}	1
TSEC2_RX_ER/FIFO2_RX_E R	Receive Data Error	AD19	I	LV _{DD}	1
TSEC2_TX_CLK/FIFO2_TX_C LK	Transmit Clock In	AC19	I	LV _{DD}	1
TSEC2_TX_EN/FIFO2_TX_EN /FIFO1_TXC[2]	Transmit Enable	AB19	O	LV _{DD}	1, 22
TSEC2_TX_ER/FIFO2_TX_ER R	Transmit Error	AB17	O	LV _{DD}	1, 5, 9
Three-Speed Ethernet Controller 3					
TSEC3_TXD[3:0]/FEC_TXD[3: 0]/FIFO3_TXD[3:0]	Transmit Data	AG18, AG17, AH17, AH19	O	TV _{DD}	1, 5, 9
TSEC3_RXD[3:0]/FEC_RXD[3: 0]/FIFO3_RXD[3:0]	Receive Data	AG16, AK19, AD16, AJ19	I	TV _{DD}	1

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals					
GND	Ground	A18, A25, A29, C3, C6, C9, C12, C15, C20, C22, E5, E8, E11, E14, F3, G7, G10, G13, G16, H5, H21, J3, J9, J12, J18, K7, L5, L13, L15, L16, L21, M3, M9, M12, M14, M16, M18, N7, N13, N15, N17, N19, N21, N23, P5, P12, P14, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, R26, T7, T12, T14, T16, T18, T20, T22, T30, U5, U11, U13, U15, U16, U17, U19, U21, U23, U25, V3, V9, V12, V14, V16, V18, V20, V22, W7, W11, W13, W15, W17, W19, W21, W27, W32, Y5, Y12, Y14, Y16, Y18, Y20, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA30, AB7, AB26, AC5, AC11, AC13, AD3, AD9, AD14, AD17, AD22, AE7, AE13, AF5, AF11, AG3, AG9, AG15, AG19, AH7, AH13, AH22, AJ5, AJ11, AJ17, AK3, AK9, AK15, AK24, AL7, AL13, AL19, AL26	—	—	—
XGND_SRDS1	SerDes Transceiver Pad GND (xpadvss)	C23, C27, D23, D25, E23, E26, F23, F24, G23, G27, H23, H25, J23, J26, K23, K24, L27, M25	—	—	—
XGND_SRDS2	SerDes Transceiver Pad GND (xpadvss)	AD23, AD25, AE23, AE27, AF23, AF24, AG23, AG26, AH23, AH25, AJ27	—	—	—

Table 79. CCB Clock Ratio

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	8:1
100	10:1
101	12:1
110	Reserved
111	Reserved

19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

[Table 80](#) describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ at power up, as shown in [Table 80](#).

Table 80. e500 Core0 to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)