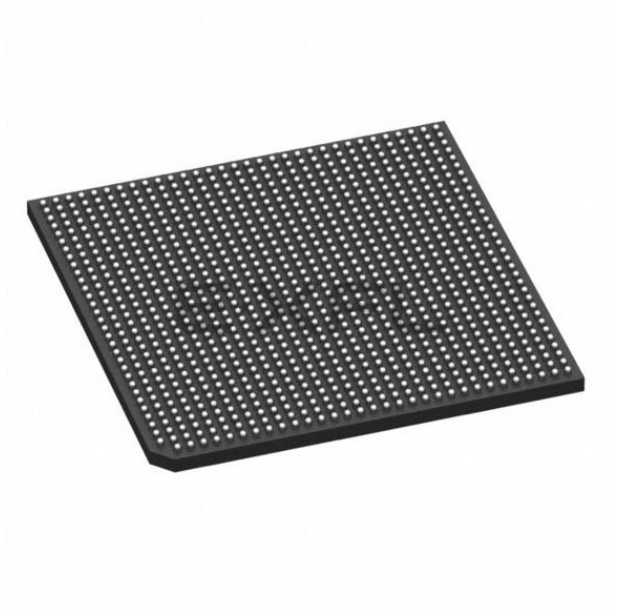

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572vtaulb

  - Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification, Revision 1.2*
  - Both 1x and 4x LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
  - Auto-detection of 1x- and 4x-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO–compliant message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox
  - Single inbound doorbell message structure
  - Facility to accept port-write messages

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/– 150	ps	4, 5, 6

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	2
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1

Table 25. FIFO Mode Transmit AC Timing Specification (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Notes:

1. The minimum cycle period (or maximum frequency) of the TX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Table 26. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period[1]	t_{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Figure 7 and Figure 8 show the FIFO timing diagrams.

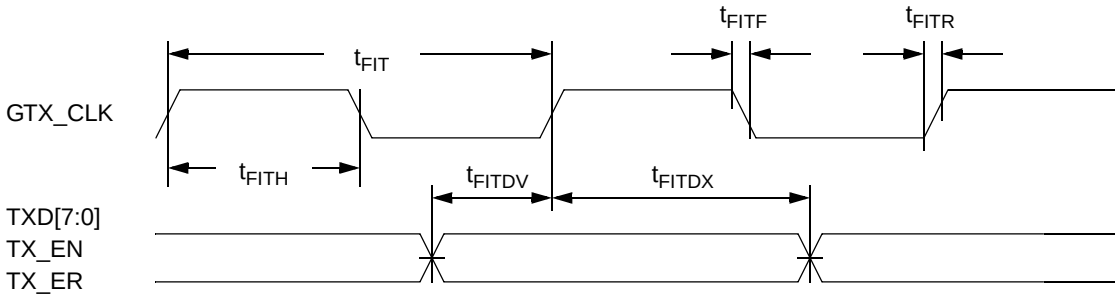

Figure 7. FIFO Transmit AC Timing Diagram

Figure 11 shows the GMII receive AC timing diagram.

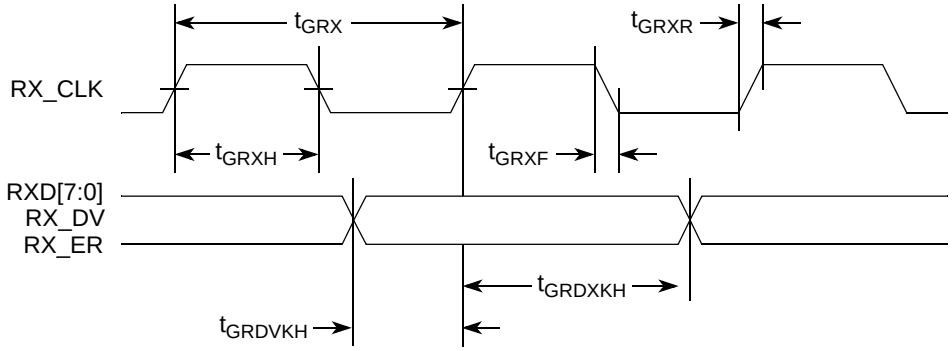

Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI receive AC timing diagram.

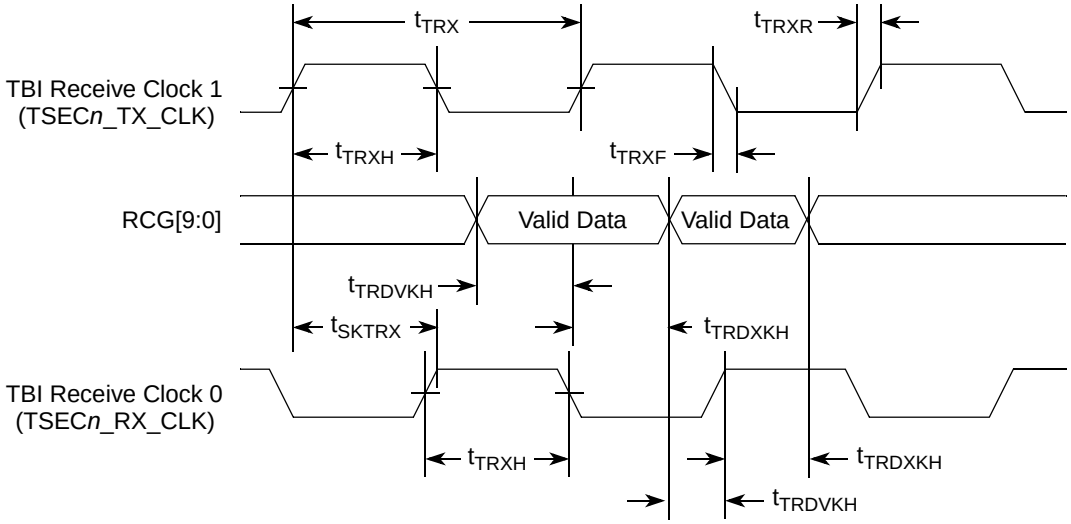

Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	—	—	ns

described in Section 21.5, “Connection Recommendations,” as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ pins.

8.3.1 DC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, “High-Speed Serial Interfaces (HSSI).”

8.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

Table 37 lists the SGMII SerDes reference clock AC requirements. Note that SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 37. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Note:
1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected through cfg_srds_sgmii_refclk during POR.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Notes:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2*t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.
2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

Table 43. MII Management DC Electrical Characteristics (LV_{DD}/TV_{DD}=3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	LV_{DD}/TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD}/TV_{DD} = Max, V_{IN} [3] = 2.1 V)	I_{IH}	—	40	µA	—

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	6.67	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	2.4	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 1.8 V ± 5% (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.

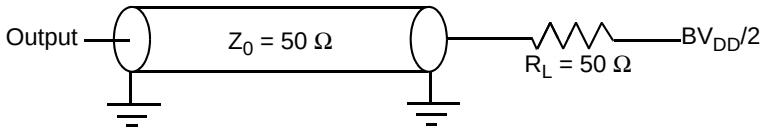

Figure 29. Local Bus AC Test Load

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. Differential Waveform

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = $(V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2$ = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

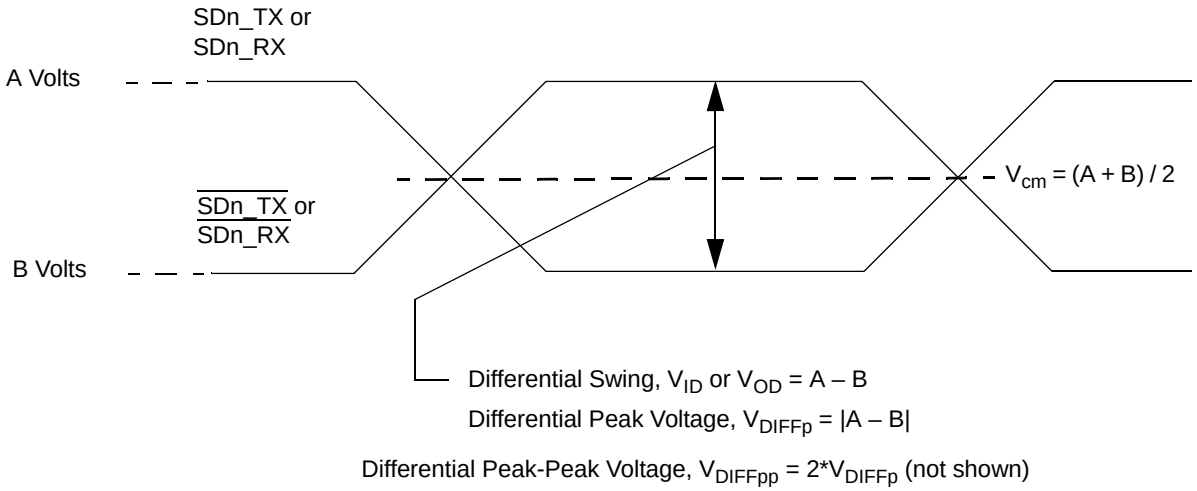

Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 72. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 73. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

17.8.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

17.8.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

17.8.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 17.6, “Receiver Specifications,” and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 60 and Table 75. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 17.6, “Receiver Specifications,” is then added to the signal and the test load is replaced by the receiver being tested.

18 Package Description

This section describes package parameters, pin assignments, and dimensions.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	O	BV_{DD}	5, 9
LGPL1/$\overline{\text{LFALE}}$	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	O	BV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O	BV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose Line 3 / Flash Write Protect	K16	O	BV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV_{DD}	—
LGPL5	UPM General Purpose Line 5 / Amux	B26	O	BV_{DD}	5, 9
LCLK[0:2]	Local Bus Clock	F17, F16, A23	O	BV_{DD}	—
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV_{DD}	—
LSYNC_OUT	Local Bus DLL Synchronization	A21	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DACK}}$[0:1]	DMA Acknowledge	W25, U30	O	OV_{DD}	21
$\overline{\text{DMA2\_DACK}}$[0]	DMA Acknowledge	AA26	O	OV_{DD}	5, 9
$\overline{\text{DMA1\_DREQ}}$[0:1]	DMA Request	Y29, V27	I	OV_{DD}	—
$\overline{\text{DMA2\_DREQ}}$[0]	DMA Request	V29	I	OV_{DD}	—
$\overline{\text{DMA1\_DDONE}}$[0:1]	DMA Done	Y28, V30	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DDONE}}$[0]	DMA Done	AA28	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DREQ}}$[2]	DMA Request	M23	I	BV_{DD}	—
Programmable Interrupt Controller					
$\overline{\text{UDE0}}$	Unconditional Debug Event Processor 0	AC25	I	OV_{DD}	—
$\overline{\text{UDE1}}$	Unconditional Debug Event Processor 1	AA25	I	OV_{DD}	—
$\overline{\text{MCP0}}$	Machine Check Processor 0	M28	I	OV_{DD}	—
$\overline{\text{MCP1}}$	Machine Check Processor 1	L28	I	OV_{DD}	—
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MSRCID[0:1]	Memory Debug Source Port ID	U27, T29	O	OV_{DD}	5, 9, 30
MSRCID[2:4]	Memory Debug Source Port ID	U28, W24, W28	O	OV_{DD}	21
MDVAL	Memory Debug Data Valid	V26	O	OV_{DD}	2, 21
CLK_OUT	Clock Out	U32	O	OV_{DD}	11
Clock					
RTC	Real Time Clock	V25	I	OV_{DD}	—
SYSCLK	System Clock	Y32	I	OV_{DD}	—
DDRCLK	DDR Clock	AA29	I	OV_{DD}	31
JTAG					
TCK	Test Clock	T28	I	OV_{DD}	
TDI	Test Data In	T27	I	OV_{DD}	12
TDO	Test Data Out	T26	O	OV_{DD}	—
TMS	Test Mode Select	U26	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test Reset	AA32	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 Test Clock	V32	I	OV_{DD}	18
L2_TSTCLK	L2 Test Clock	V31	I	OV_{DD}	18
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	N24	I	OV_{DD}	18
$\overline{\text{TEST\_SEL}}$	Test Select 0	K28	I	OV_{DD}	18
Power Management					
ASLEEP	Asleep	P28	O	OV_{DD}	9, 15, 21

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

Table 81. e500 Core1 to CCB Clock Ratio

Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Table 82. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1

This noise must be prevented from reaching other components in the MPC8572E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power (SV_{DD}_SRDSn and XV_{DD}_SRDSn) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (SV_{DD}_SRDSn and XV_{DD}_SRDSn) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND pins of the device.

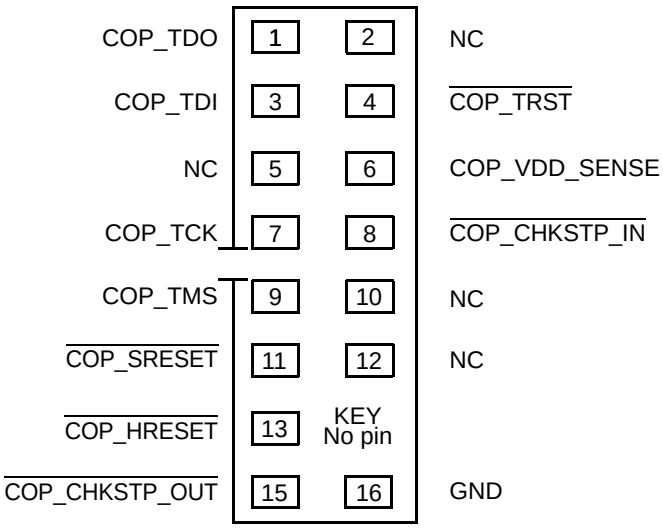

Figure 65. COP Connector Physical Pinout