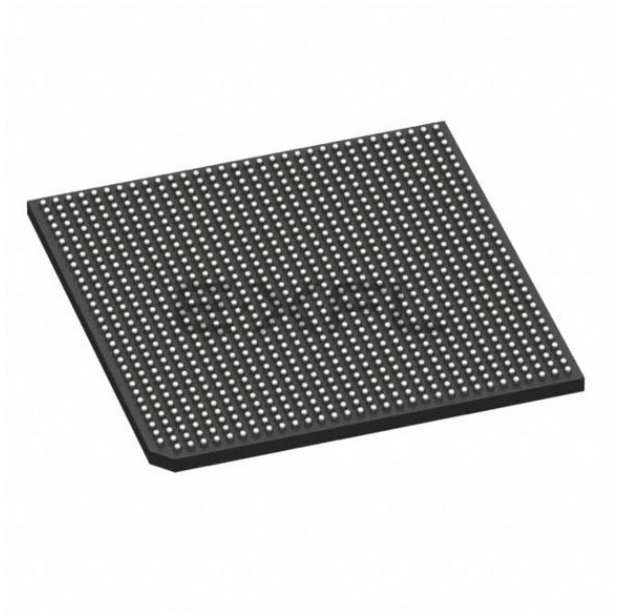

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.5GHz |
| Co-Processors/DSP | Signal Processing; SPE |
| RAM Controllers | DDR2, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 1023-BFBGA, FCBGA |
| Supplier Device Package | 1023-FCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572vtavnd |

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

— Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.

— Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.

— 36-bit real addressing

— Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.

— Enhanced hardware and software debug support

— Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
  — Shared by both cores.
  — Flexible configuration and individually configurable per core.
  — Full ECC support on 64-bit boundary in both cache and SRAM modes
  — Cache mode supports instruction caching, data caching, or both.
  — External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    – 1, 2, or 4 ways can be configured for stashing only.
  — Eight-way set-associative cache organization (32-byte cache lines)
  — Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  — Global locking and Flash clearing done through writes to L2 configuration registers
  — Instruction and data locks can be Flash cleared separately.
  — Per-way allocation of cache region to a given processor.
  — SRAM features include the following:
    – 1, 2, 4, or 8 ways can be configured as SRAM.
    – I/O devices access SRAM regions by marking transactions as snoopable (global).
    – Regions can reside at any aligned location in the memory map.
    – Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
  — Twelve local access windows define mapping within local 36-bit address space.
  — Inbound and outbound ATMUs map to larger external address spaces.

**NOTE**

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

# 3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

**Table 4. MPC8572E Power Dissipation [1]**

| CCB Frequency | Core Frequency | Typical-65[2] | Typical-105[3] | Maximum[4] | Unit |
|---|---|---|---|---|---|
| 533 | 1067 | 12.3 | 17.8 | 18.5 | W |
| 533 | 1200 | 12.3 | 17.8 | 18.5 | W |
| 533 | 1333 | 16.3 | 22.8 | 24.5 | W |
| 600 | 1500 | 17.3 | 23.9 | 25.9 | W |

**Notes:**

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/$XV_{DD}$ rails.
2. Typical-65 is based on $V_{DD}$ = 1.1 V, $T_j$ = 65 °C, running Dhrystone.
3. Typical-105 is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running Dhrystone.
4. Maximum is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

**Table 5. MPC8572EL Power Dissipation [1]**

| CCB Frequency | Core Frequency | Typical-65[2] | Typical-105[3] | Maximum[4] | Unit |
|---|---|---|---|---|---|
| 533 | 1067 | 12 | 15 | 15.8 | W |
| 533 | 1200 | 12 | 15.5 | 16.3 | W |
| 533 | 1333 | 12 | 15.9 | 16.9 | W |
| 600 | 1500 | 13 | 18.7 | 20.0 | W |

**Notes:**

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/$XV_{DD}$ rails.
2. Typical-65 is based on $V_{DD}$ = 1.1 V, $T_j$ = 65 °C, running Dhrystone.
3. Typical-105 is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running Dhrystone.
4. Maximum is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running a smoke test.

**Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | µA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | µA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1 and 2.
2 $TV_{DD}$ supports eTSECs 3 and 4 or FEC.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

## 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

**Table 25. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period[1] | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |

Figure 16 shows the TBI receive AC timing diagram.

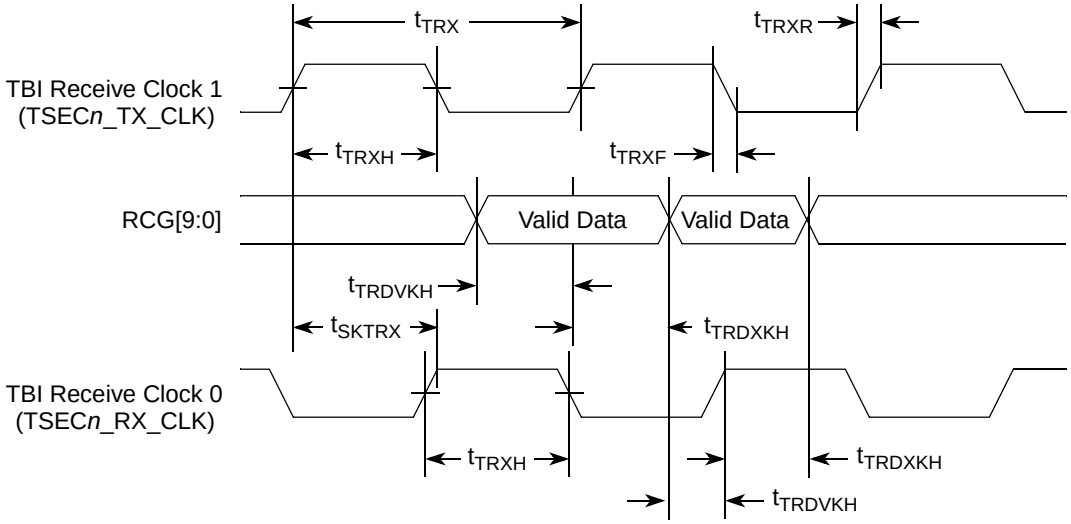


**Figure 16. TBI Receive AC Timing Diagram**

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

**Table 33. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRRX}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRRX}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

Figure 17 shows the TBI receive the timing diagram.

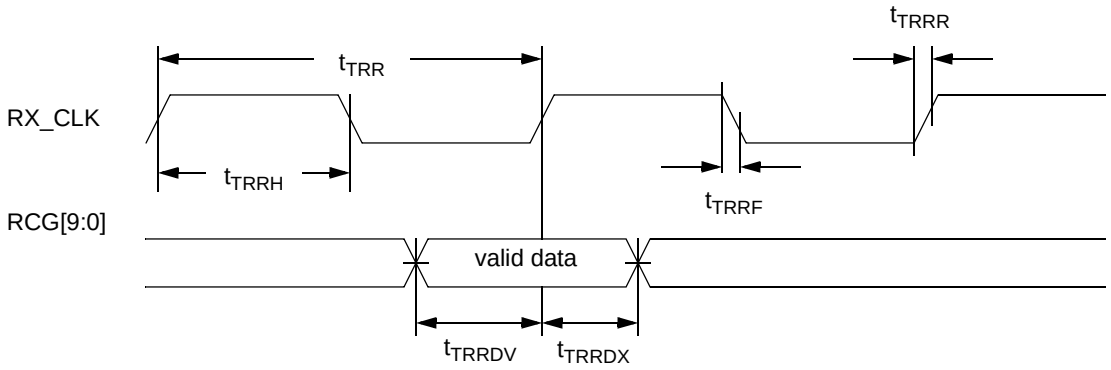


**Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

**Table 34. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock period [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 4] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.

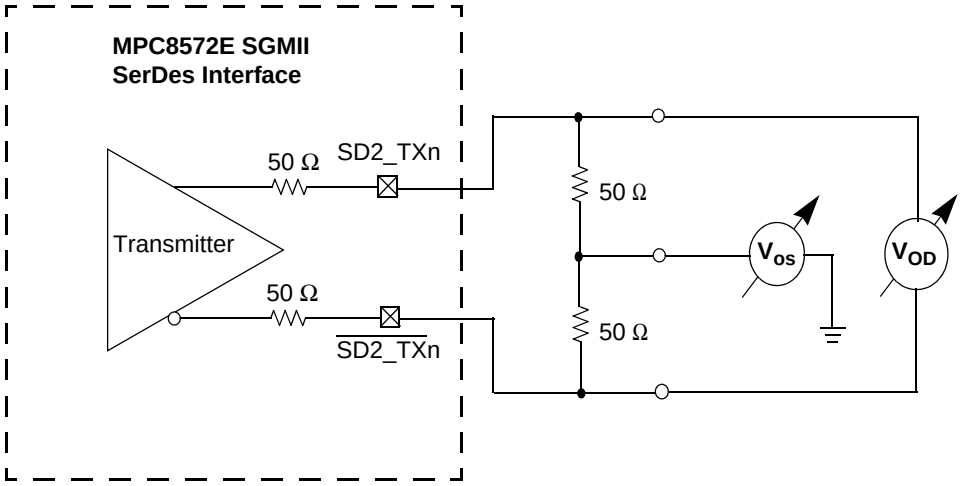


**Figure 23. SGMII Transmitter DC Measurement Circuit**

Table 39 lists the SGMII DC receiver electrical characteristics.

**Table 39. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $XV_{DD\_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX\_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM\_ACp-p}$ | | — | 100 | mV | 5 |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | | $Z_{RX\_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of MPC8572E's SerDes 2 Control Register.
5. $V_{CM\_ACp-p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

### 8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 25, respectively.

#### 8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

**Table 40. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $XV_{DD\_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| $V_{OD}$ fall time (80%-20%) | tfall | 50 | — | 120 | ps | — |
| $V_{OD}$ rise time (20%-80%) | $t_{rise}$ | 50 | — | 120 | ps | — |

**Notes:**
1. Each UI is 800 ps ± 100 ppm.

#### 8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

**Table 41. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $XV_{DD\_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal Jitter Tolerance | JSIN | 0.1 | — | — | UI p-p | 1 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC Coupling Capacitor | $C_{TX}$ | 5 | — | 200 | nF | 3 |

**Notes:**
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

Table 48 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 48. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | 0.65 x $BV_{DD}$ | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.35 x $BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | TBD | TBD | µA |
| High-level output voltage ($I_{OH}$ = –100 µA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| High-level output voltage ($I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.45 | — | V |
| Low-level output voltage ($I_{OL}$ = 100 µA) | $V_{OL}$ | — | 0.2 | V |
| Low-level output voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.45 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 10.2 Local Bus AC Electrical Specifications

Table 49 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC.

**Table 49. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7,8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.4 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | 3 |

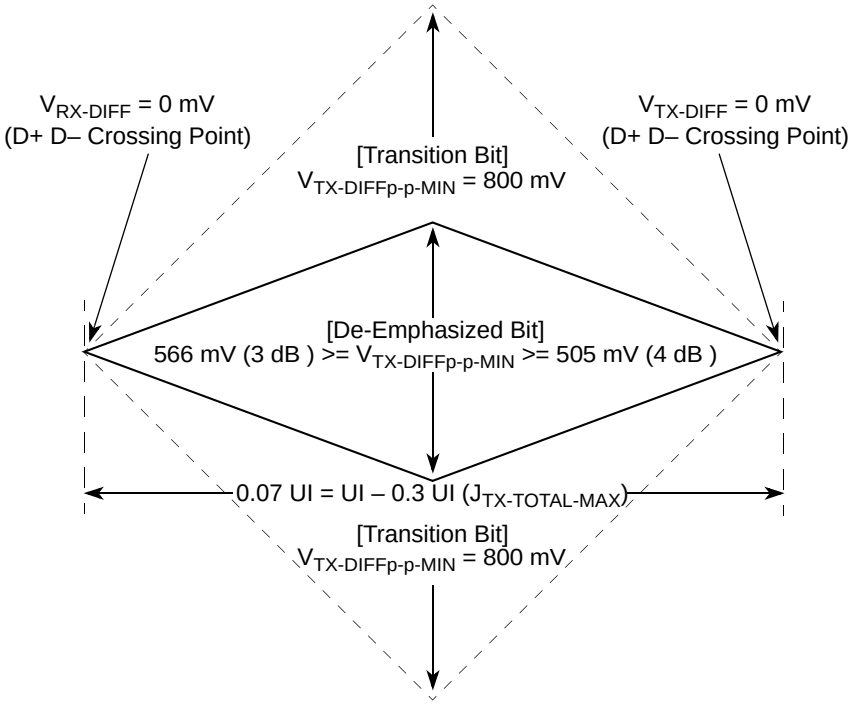


**Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

## 16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

**Table 63. Differential Receiver (RX) Input Specifications**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{RX-DIFFp-p}$ | Differential Input Peak-to-Peak Voltage | 0.175 | — | 1.200 | V | $V_{RX-DIFFp-p}$ = 2*\|$V_{RX-D+}$ - $V_{RX-D-}$\| See Note 2. |
| $T_{RX-EYE}$ | Minimum Receiver Eye Width | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - $T_{RX-EYE}$= 0.6 UI. See Notes 2 and 3. |

**Table 63. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $L_{RX-SKEW}$ | Total Skew | — | — | 20 | ns | Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 57 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 56). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 57). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

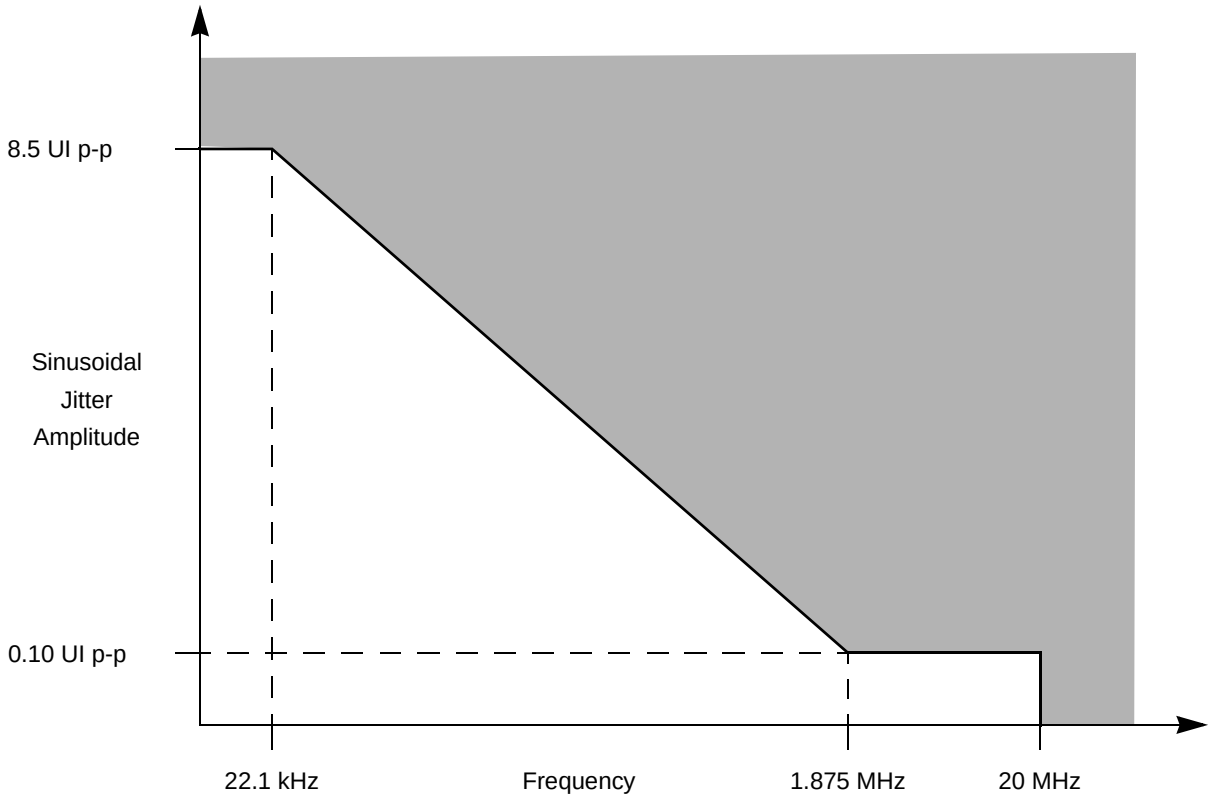


**Figure 59. Single Frequency Sinusoidal Jitter Limits**

## 17.7 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 72, Table 73, and Table 74) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 60 with the parameters specified in Table 75. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100-Ω +/– 5% differential resistive load.

link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than $10^{-12}$. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

### 17.8.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

### 17.8.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

### 17.8.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 17.6, “Receiver Specifications,” and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 60 and Table 75. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 17.6, “Receiver Specifications,” is then added to the signal and the test load is replaced by the receiver being tested.

# 18 Package Description

This section describes package parameters, pin assignments, and dimensions.

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| $\overline{\text{IRQ\_OUT}}$ | Interrupt Output | U24 | O | $OV_{DD}$ | 2, 4 |
| **1588** | | | | | |
| TSEC_1588_CLK | Clock In | AM22 | I | $LV_{DD}$ | — |
| TSEC_1588_TRIG_IN | Trigger In | AM23 | I | $LV_{DD}$ | — |
| TSEC_1588_TRIG_OUT | Trigger Out | AA23 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_CLK_OUT | Clock Out | AC23 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_PULSE_OUT1 | Pulse Out1 | AA22 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_PULSE_OUT2 | Pulse Out2 | AB23 | O | $LV_{DD}$ | 5, 9 |
| **Ethernet Management Interface 1** | | | | | |
| EC1_MDC | Management Data Clock | AL30 | O | $LV_{DD}$ | 5, 9 |
| EC1_MDIO | Management Data In/Out | AM25 | I/O | $LV_{DD}$ | — |
| **Ethernet Management Interface 3** | | | | | |
| EC3_MDC | Management Data Clock | AF19 | O | $TV_{DD}$ | 5, 9 |
| EC3_MDIO | Management Data In/Out | AF18 | I/O | $TV_{DD}$ | — |
| **Ethernet Management Interface 5** | | | | | |
| EC5_MDC | Management Data Clock | AF14 | O | $TV_{DD}$ | 21 |
| EC5_MDIO | Management Data In/Out | AF15 | I/O | $TV_{DD}$ | — |
| **Gigabit Ethernet Reference Clock** | | | | | |
| EC_GTX_CLK125 | Reference Clock | AM24 | I | $LV_{DD}$ | 32 |
| **Three-Speed Ethernet Controller 1** | | | | | |
| TSEC1_RXD[7:0]/FIFO1_RXD[7:0] | Receive Data | AM28, AL28, AM26, AK23, AM27, AK26, AL29, AM30 | I | $LV_{DD}$ | 1 |
| TSEC1_TXD[7:0]/FIFO1_TXD[7:0] | Transmit Data | AC20, AD20, AE22, AB22, AC22, AD21, AB21, AE21 | O | $LV_{DD}$ | 1, 5, 9 |
| TSEC1_COL/FIFO1_TX_FC | Collision Detect/Flow Control | AJ23 | I | $LV_{DD}$ | 1 |
| TSEC1_CRS/FIFO1_RX_FC | Carrier Sense/Flow Control | AM31 | I/O | $LV_{DD}$ | 1, 16 |
| TSEC1_GTX_CLK | Transmit Clock Out | AK27 | O | $LV_{DD}$ | |
| TSEC1_RX_CLK/FIFO1_RX_CLK | Receive Clock | AL25 | I | $LV_{DD}$ | 1 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0] | Receive Data Valid | AL24 | I | $LV_{DD}$ | 1 |
| TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1] | Receive Data Error | AM29 | I | $LV_{DD}$ | 1 |
| TSEC1_TX_CLK/FIFO1_TX_CLK | Transmit Clock In | AB20 | I | $LV_{DD}$ | 1 |
| TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0] | Transmit Enable | AJ24 | O | $LV_{DD}$ | 1, 22 |
| TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1] | Transmit Error | AK25 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 2** | | | | | |
| TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8] | Receive Data | AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20 | I | $LV_{DD}$ | 1 |
| TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8] | Transmit Data | AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18 | O | $LV_{DD}$ | 1, 5, 9, 24 |
| TSEC2_COL/FIFO2_TX_FC | Collision Detect/Flow Control | AE19 | I | $LV_{DD}$ | 1 |
| TSEC2_CRS/FIFO2_RX_FC | Carrier Sense/Flow Control | AJ20 | I/O | $LV_{DD}$ | 1, 16 |
| TSEC2_GTX_CLK | Transmit Clock Out | AE18 | O | $LV_{DD}$ | — |
| TSEC2_RX_CLK/FIFO2_RX_CLK | Receive Clock | AL23 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2] | Receive Data Valid | AJ22 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_ER/FIFO2_RX_ER | Receive Data Error | AD19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_CLK/FIFO2_TX_CLK | Transmit Clock In | AC19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2] | Transmit Enable | AB19 | O | $LV_{DD}$ | 1, 22 |
| TSEC2_TX_ER/FIFO2_TX_ERR | Transmit Error | AB17 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 3** | | | | | |
| TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0] | Transmit Data | AG18, AG17, AH17, AH19 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0] | Receive Data | AG16, AK19, AD16, AJ19 | I | $TV_{DD}$ | 1 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| MSRCID[0:1] | Memory Debug Source Port ID | U27, T29 | O | $OV_{DD}$ | 5, 9, 30 |
| MSRCID[2:4] | Memory Debug Source Port ID | U28, W24, W28 | O | $OV_{DD}$ | 21 |
| MDVAL | Memory Debug Data Valid | V26 | O | $OV_{DD}$ | 2, 21 |
| CLK_OUT | Clock Out | U32 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | | |
| RTC | Real Time Clock | V25 | I | $OV_{DD}$ | — |
| SYSCLK | System Clock | Y32 | I | $OV_{DD}$ | — |
| DDRCLK | DDR Clock | AA29 | I | $OV_{DD}$ | 31 |
| **JTAG** | | | | | |
| TCK | Test Clock | T28 | I | $OV_{DD}$ | |
| TDI | Test Data In | T27 | I | $OV_{DD}$ | 12 |
| TDO | Test Data Out | T26 | O | $OV_{DD}$ | — |
| TMS | Test Mode Select | U26 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | Test Reset | AA32 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | | |
| L1_TSTCLK | L1 Test Clock | V32 | I | $OV_{DD}$ | 18 |
| L2_TSTCLK | L2 Test Clock | V31 | I | $OV_{DD}$ | 18 |
| $\overline{\text{LSSD\_MODE}}$ | LSSD Mode | N24 | I | $OV_{DD}$ | 18 |
| $\overline{\text{TEST\_SEL}}$ | Test Select 0 | K28 | I | $OV_{DD}$ | 18 |
| **Power Management** | | | | | |
| ASLEEP | Asleep | P28 | O | $OV_{DD}$ | 9, 15, 21 |

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

**Table 81. e500 Core1 to CCB Clock Ratio**

| Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals | e500 Core1:CCB Clock Ratio | Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals | e500 Core1:CCB Clock Ratio |
|---|---|---|---|
| 000 | Reserved | 100 | 2:1 |
| 001 | Reserved | 101 | 5:2 (2.5:1) |
| 010 | Reserved | 110 | 3:1 |
| 011 | 3:2 (1.5:1) | 111 | 7:2 (3.5:1) |

## 19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

**Table 82. DDR Clock Ratio**

| Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals | DDR:DDRCLK Ratio |
|---|---|
| 000 | 3:1 |
| 001 | 4:1 |
| 010 | 6:1 |
| 011 | 8:1 |
| 100 | 10:1 |

in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

See Section 20.4, "1x/4x LP-Serial Signal Descriptions," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

# 20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, 1023 33 × 33 FC-PBGA.

The package uses a 29.6 × 29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

**Table 84. Package Thermal Characteristics**

| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Single-layer (1s) | $R_{\Theta JA}$ | 15 | °C/W | 1, 2 |
| Junction to ambient, natural convection | Four-layer (2s2p) | $R_{\Theta JA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (at 200 ft./min.) | Single-layer (1s) | $R_{\Theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (ar 200 ft./min.) | Four-layer (2s2p) | $R_{\Theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction to board | — | $R_{\Theta JB}$ | 4 | °C/W | 4 |
| Junction to case | — | $R_{\Theta JC}$ | 0.5 | °C/W | 5 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

## 20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

## 21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio." The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

## 21.2 Power Supply Design

### 21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_PLAT, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_DDR, $AV_{DD}$_LBIU, $AV_{DD}$_SRDS1 and $AV_{DD}$_SRDS2 respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 62, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

### 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

Figure 66. JTAG Interface Connection

## 21.10 Guidelines for High-Speed Interface Termination

### 21.10.1 SerDes 1 Interface Entirely Unused

If the high-speed SerDes 1 interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX}}$[7:0]
- Reserved pins C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1:

- SD1_RX[7:0]
- $\overline{\text{SD1\_RX}}$[7:0]
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

Pins K32 and C29 must be tied to $XV_{DD}$_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.

The POR configuration pin cfg_srds1_en on TSEC2_TXD[5] can be used to power down SerDes 1 block for power saving. Note that both SVDD_SRDS1 and XVDD_SRDS1 must remain powered.

### 21.10.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes 1 interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX}}$[7:0]
- Reserved pins: C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1 if not used:

- SD1_RX[7:0]
- $\overline{\text{SD1\_RX}}$[7:0]

Pins K32 and C29 must be tied to $XV_{DD}$_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.