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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8572epxarlc

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$	1
	45(default) 45(default) 125	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$ $BV_{DD} = 1.8\text{ V}$	
DDR2 signal	18 36 (half strength mode)	$GV_{DD} = 1.8\text{ V}$	2
DDR3 signal	20 40 (half strength mode)	$GV_{DD} = 1.5\text{ V}$	2
eTSEC/10/100 signals	45	$L/TV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, JTAG	45	$OV_{DD} = 3.3\text{ V}$	—
I2C	150	$OV_{DD} = 3.3\text{ V}$	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j = 105^\circ\text{C}$ and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD} , AV_{DD-n} , BV_{DD} , LV_{DD} , OV_{DD} , SV_{DD_SRDS1} and SV_{DD_SRDS2} , TV_{DD} , XV_{DD_SRDS1} and XV_{DD_SRDS2}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for GV_{DD} is not required.

Table 14 provides the current draw characteristics for MV_{REFn} .

Table 14. Current Draw Characteristics for MV_{REFn}

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for MV_{REFn}	DDR2 SDRAM	$I_{MV_{REFn}}$	—	1500	μA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for MV_{REFn} must be able to supply up to 1500 μA or 1250 μA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≥ 667 MHz	V_{ILAC}	—	$MV_{REFn} - 0.20$	V	—
	≤ 533 MHz		—	$MV_{REFn} - 0.25$		
AC input high voltage	≥ 667 MHz	V_{IHAC}	$MV_{REFn} + 0.20$	—	V	—
	≤ 533 MHz		$MV_{REFn} + 0.25$	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V \pm 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REFn} - 0.175$	V	—
AC input high voltage	V_{IHAC}	$MV_{REFn} + 0.175$	—	V	—

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6
800 MHz		$-0.5 \times t_{MCK} - 0.375$	$-0.5 \times t_{MCK} + 0.375$		
≤ 667 MHz		$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$		
MDQS epilogue end	t_{DDKHME}			ns	6
800 MHz		-0.375	0.375		
≤ 667 MHz	t_{DDKHME}	-0.6	0.6	ns	6

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the $MCK[n]$ clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the $TIMING_CFG_2$ register. This typically be set to the same delay as in $DDR_SDRAM_CLK_CNTL[CLK_ADJUST]$. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of $MCK[n]$ at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in [Table 24](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -4.0 \text{ mA}$)	VOH	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 4.0 \text{ mA}$)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	40	μA	1, 2,3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-600	—	μA	3

Notes:

¹ LV_{DD} supports eTSECs 1 and 2.

² TV_{DD} supports eTSECs 3 and 4 or FEC.

³ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#).

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1,2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOH = -1.0 \text{ mA}$)	VOH	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $IOL = 1.0 \text{ mA}$)	VOL	GND - 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.70	V	—

Figure 9 shows the GMII transmit AC timing diagram.

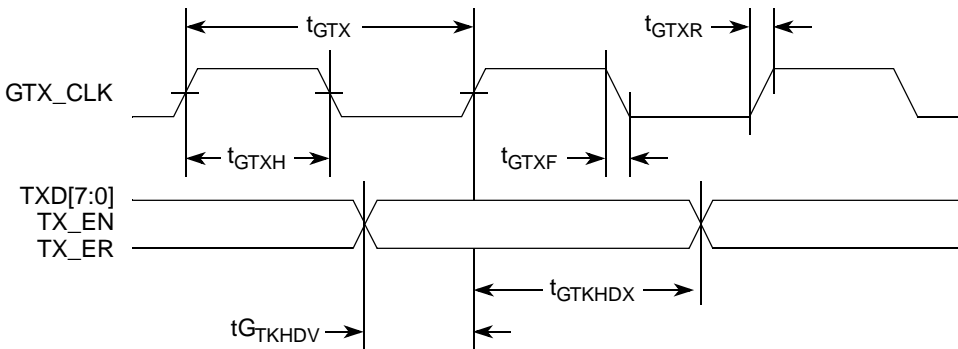


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}^2	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

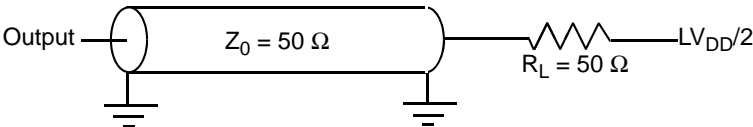


Figure 10. eTSEC AC Test Load

Figure 12 shows the MII transmit AC timing diagram.

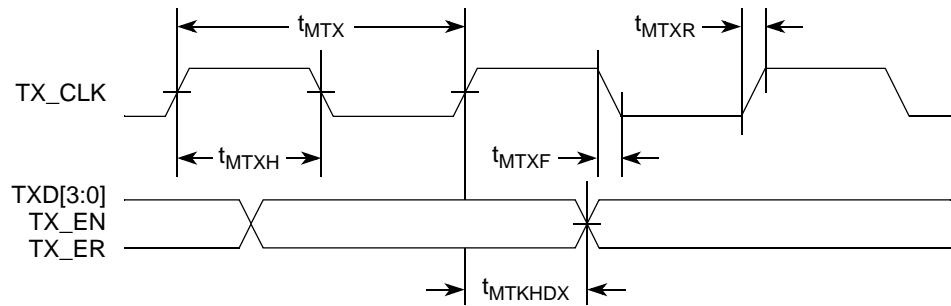


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of $2.5/3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}^2	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}^2	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

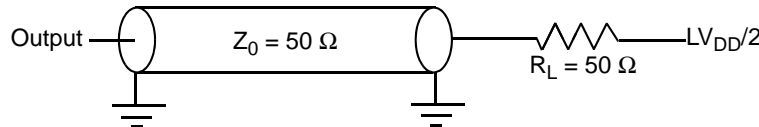


Figure 13. eTSEC AC Test Load

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

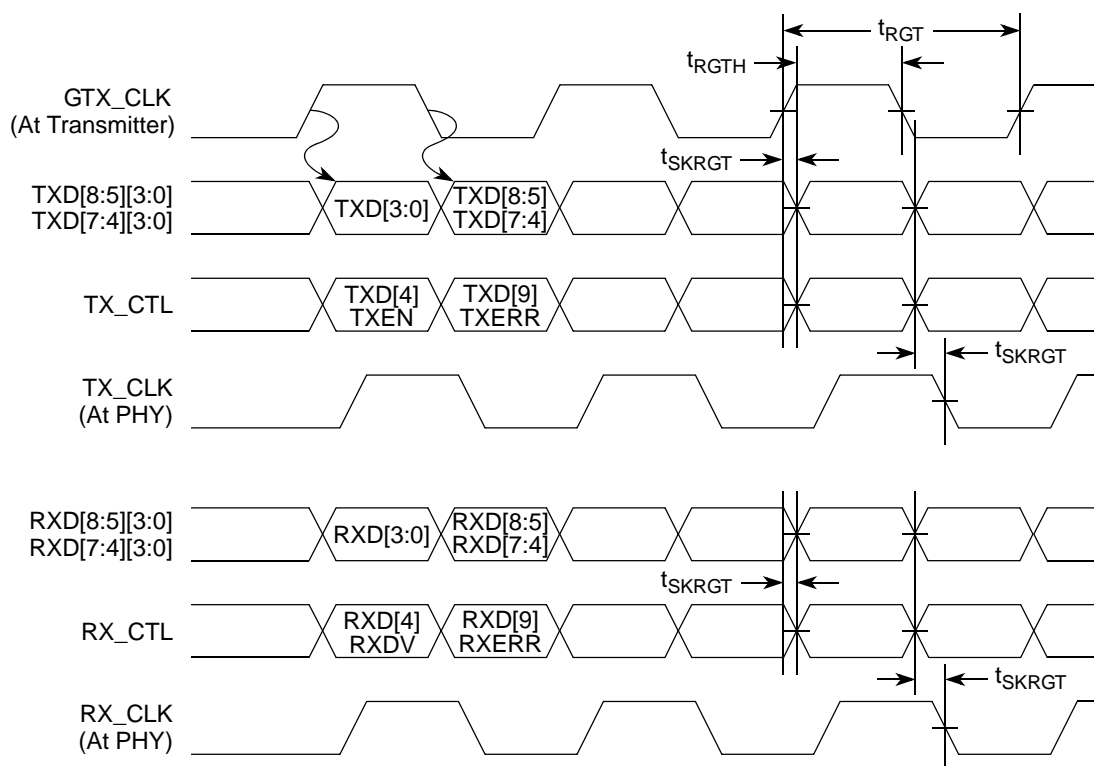


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/V_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTRF}	1.0	—	2.0	ns

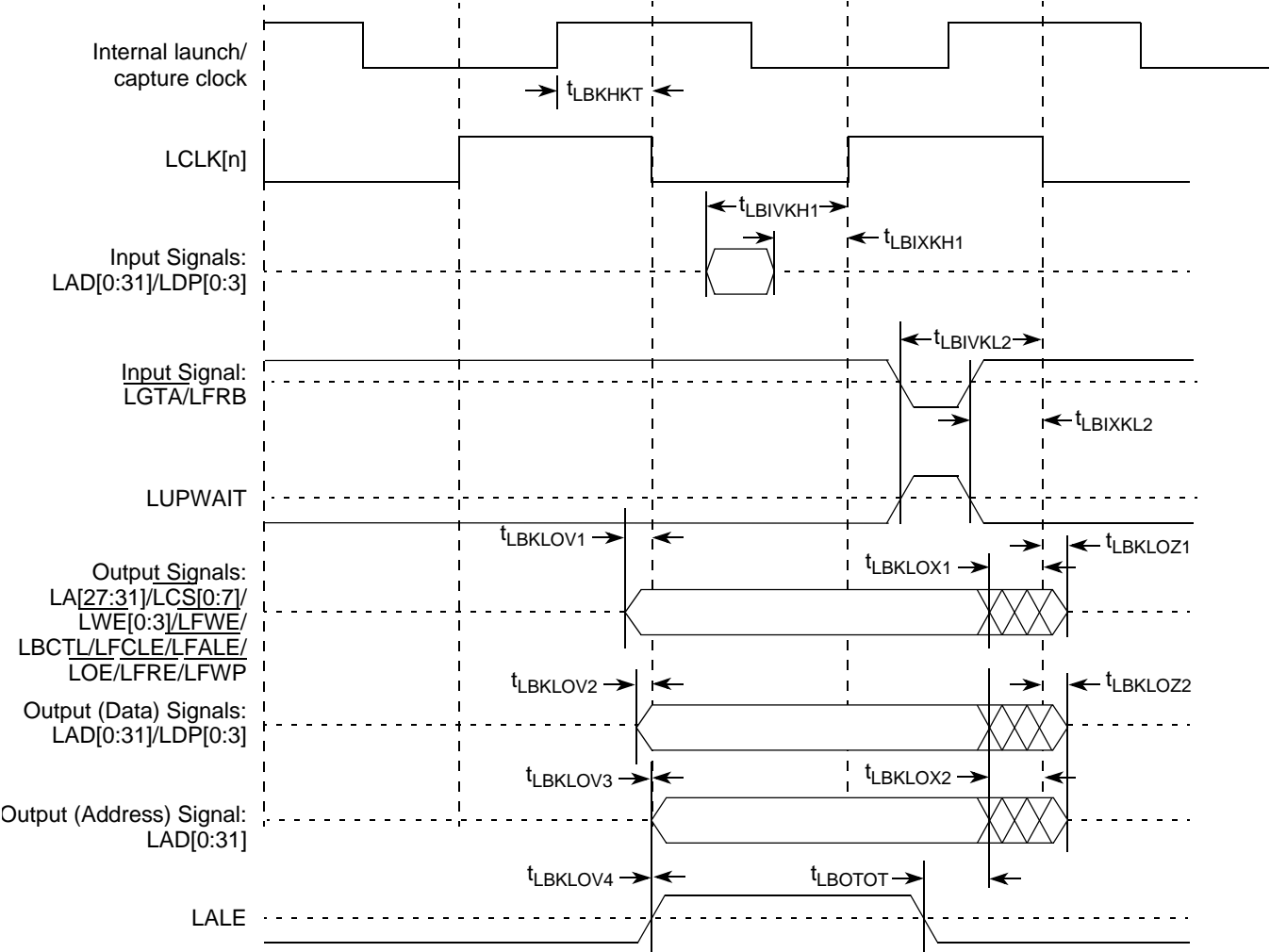


Figure 31. Local Bus Signals (PLL Bypass Mode)

6. Differential Waveform

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SDn_TX}}$, for example) from the non-inverting signal (SDn_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.
2. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{\text{cm_out}} = (\text{V}_{\text{SDn_TX}} + \text{V}_{\overline{\text{SDn_TX}}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

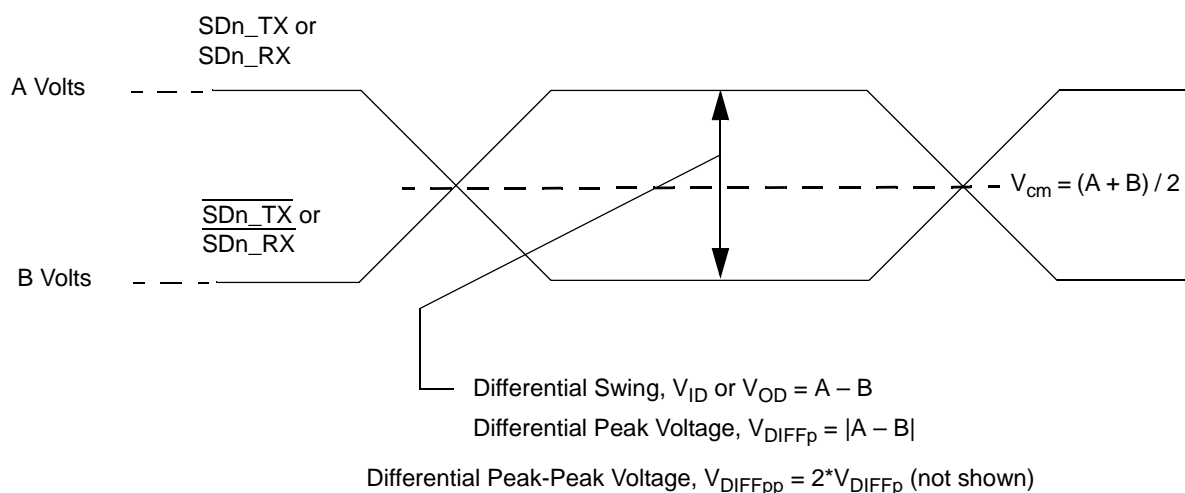


Figure 43. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{\text{DIFFp-p}}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

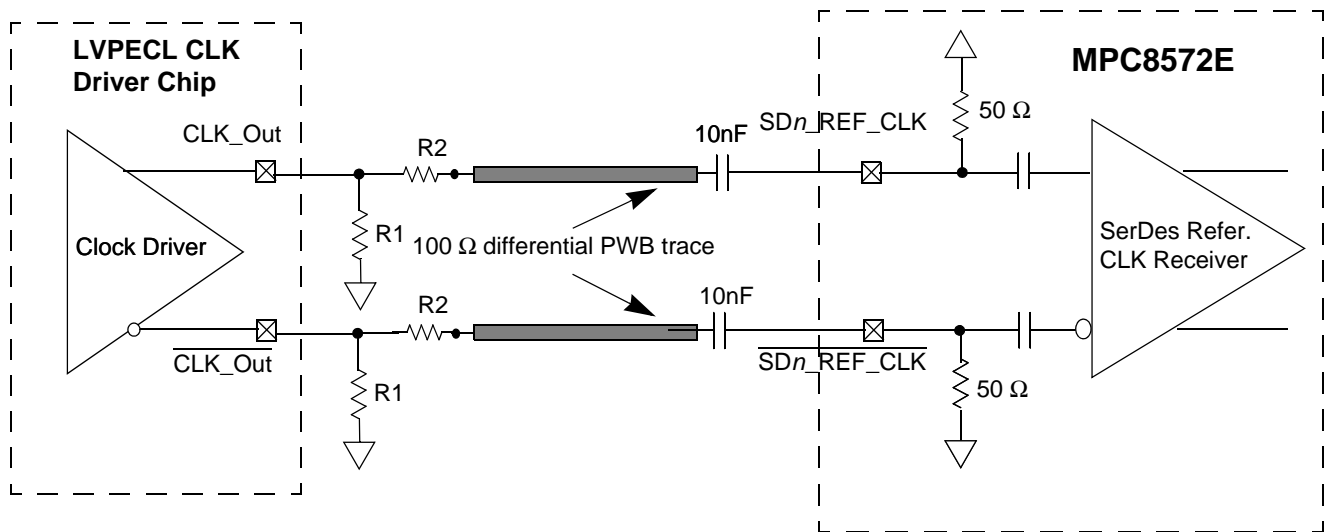


Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

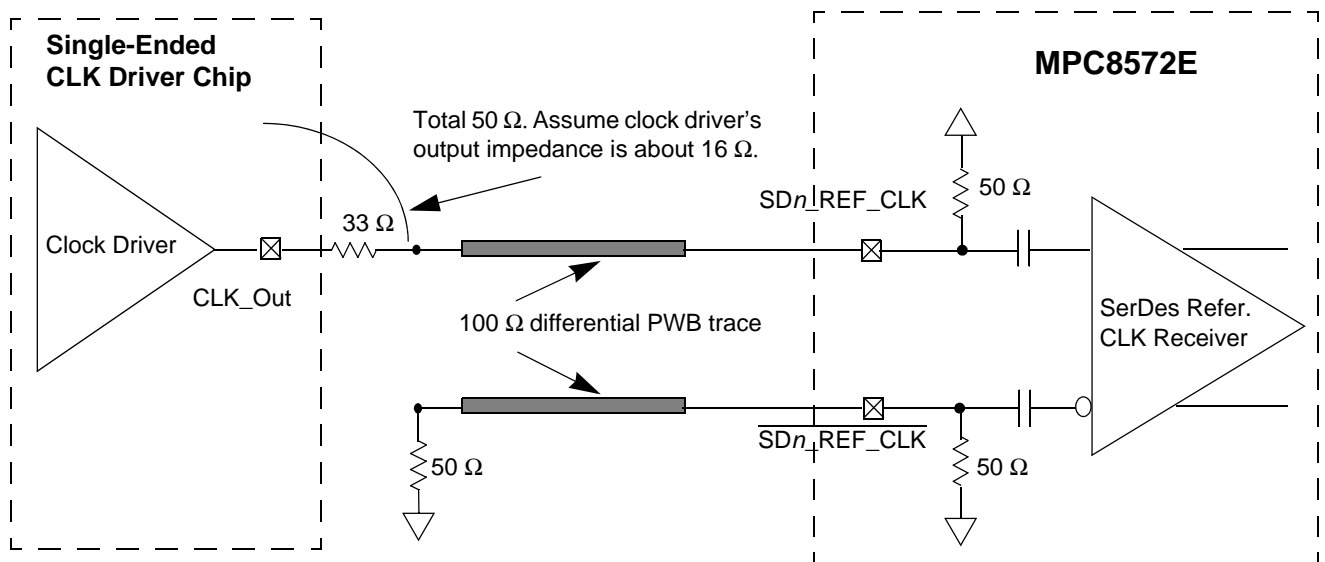


Figure 51. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

- [Section 17, “Serial RapidIO”](#)

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see [Section 15.2, “SerDes Reference Clocks.”](#)

16.2 AC Requirements for PCI Express SerDes Reference Clocks

[Table 61](#) lists AC requirements.

Table 61. SD1_REF_CLK and SD1_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:

1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

16.4.1 Differential Transmitter (TX) Output

[Table 62](#) defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 62. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit		—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = V_{RXD+} + V_{RXD-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $ V_{RX-D+} + V_{RX-D-} /2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance ($50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see [Section 15.2, “SerDes Reference Clocks.”](#)

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64 lists the AC requirements.

Table 64. SD n _REF_CLK and $\overline{\text{SD}n_REF_CLK}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in [Section 8.1, “Enhanced Three-Speed Ethernet Controller \(eTSEC\) \(10/100/1000 Mbps\)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.”](#) The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	O	GV _{DD}	—
D2_MWE	Write Enable	AA2	O	GV _{DD}	—
D2_MCAS	Column Address Strobe	AD1	O	GV _{DD}	—
D2_MRAS	Row Address Strobe	AA1	O	GV _{DD}	—
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	O	GV _{DD}	11
D2_MCS[0:3]	Chip Select	AB1, AG2, AC1, AH2	O	GV _{DD}	—
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	O	GV _{DD}	—
D2_MCK[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	O	GV _{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	O	GV _{DD}	—
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV _{DD}	25
Local Bus Controller Interface					
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV _{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV _{DD}	—
LA[27]	Burst Address	J21	O	BV _{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	O	BV _{DD}	5, 7, 9
LCS[0:4]	Chip Selects	B23, E16, D20, B25, A22	O	BV _{DD}	10
LCS[5]/DMA2_DREQ[1]	Chip Selects / DMA Request	D19	I/O	BV _{DD}	1, 10
LCS[6]/DMA2_DACK[1]	Chip Selects / DMA Ack	E19	O	BV _{DD}	1, 10
LCS[7]/DMA2_DDONE[1]	Chip Selects / DMA Done	C21	O	BV _{DD}	1, 10
LWE[0]/LBS[0]/LFW	Write Enable / Byte Select	D17	O	BV _{DD}	5, 9
LWE[1]/LBS[1]	Write Enable / Byte Select	F15	O	BV _{DD}	5, 9
LWE[2]/LBS[2]	Write Enable / Byte Select	B24	O	BV _{DD}	5, 9
LWE[3]/LBS[3]	Write Enable / Byte Select	D18	O	BV _{DD}	5, 9
LALE	Address Latch Enable	F19	O	BV _{DD}	5, 8, 9
LBCTL	Buffer Control	L18	O	BV _{DD}	5, 8, 9

19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

Table 77. MPC8572E Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1067 MHz		1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1067	800	1200	800	1333	800	1500	MHz	1, 2
CCB frequency	400	533	400	533	400	533	400	600	MHz	
DDR Data Rate	400	667	400	667	400	667	400	800	MHz	

Notes:

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2, “CCB/SYSCLK PLL Ratio,”](#) [Section 19.3, “e500 Core PLL Ratio,”](#) and [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
- The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. [Table 78](#) provides the clocking specifications for the memory bus.

Table 79. CCB Clock Ratio

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	8:1
100	10:1
101	12:1
110	Reserved
111	Reserved

19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

[Table 80](#) describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ at power up, as shown in [Table 80](#).

Table 80. e500 Core0 to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ Signals	e500 Core0:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

See Section 20.4, “1x/4x LP-Serial Signal Descriptions,” in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, 1023 33 × 33 FC-PBGA.

The package uses a 29.6 × 29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

Table 84. Package Thermal Characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer (1s)	R _{ΘJA}	15	°C/W	1, 2
Junction to ambient, natural convection	Four-layer (2s2p)	R _{ΘJA}	11	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer (1s)	R _{ΘJMA}	11	°C/W	1, 3
Junction to ambient (ar 200 ft./min.)	Four-layer (2s2p)	R _{ΘJMA}	8	°C/W	1, 3
Junction to board	—	R _{ΘJB}	4	°C/W	4
Junction to case	—	R _{ΘJC}	0.5	°C/W	5

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

Figure 66. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

21.10.1 SerDes 1 Interface Entirely Unused

If the high-speed SerDes 1 interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD1_TX[7:0]
- $\overline{\text{SD1_TX}}$ [7:0]
- Reserved pins C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1:

- SD1_RX[7:0]
- $\overline{\text{SD1_RX}}$ [7:0]
- SD1_REF_CLK
- $\overline{\text{SD1_REF_CLK}}$

Pins K32 and C29 must be tied to $\text{XV}_{\text{DD_SRDS1}}$. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300- Ω resistor.

The POR configuration pin `cfg_srds1_en` on TSEC2_TXD[5] can be used to power down SerDes 1 block for power saving. Note that both SVDD_SRDS1 and XVDD_SRDS1 must remain powered.

21.10.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes 1 interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:0]
- $\overline{\text{SD1_TX}}$ [7:0]
- Reserved pins: C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1 if not used:

- SD1_RX[7:0]
- $\overline{\text{SD1_RX}}$ [7:0]

Pins K32 and C29 must be tied to $\text{XV}_{\text{DD_SRDS1}}$. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300- Ω resistor.