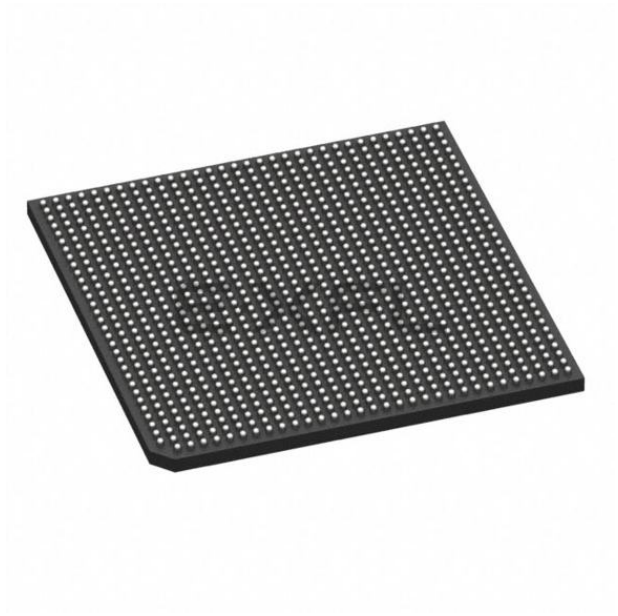

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8572epxatlc

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
  - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage		AV_{DD}	1.1 V ± 55 mV	V	1
Core power supply for SerDes transceivers		SV_{DD}	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.1 V ± 55 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	—
	DDR3 SDRAM Interface		1.5 V ± 75 mV		—
Three-speed Ethernet I/O voltage		LV_{DD} TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 3.3 V ± 165 mV 2.5 V ± 125 mV	V	4 4
DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus and GPIO I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR2 and DDR3 SDRAM Interface reference	$MV_{REF}n$	$GV_{DD}/2$ ± 1%	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus and GPIO signals	BV_{IN}	GND to BV_{DD}	V	—
	Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_J	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 21.2.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, that may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

Table 4. MPC8572E Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

Table 5. MPC8572EL Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

Table 14 provides the current draw characteristics for $MV_{REF}n$.

Table 14. Current Draw Characteristics for MV_{REF} *n*

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	$I_{MVREF}n$	—	1500	µA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 µA or 1250 uA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	>=667 MHz	V_{ILAC}	—	$MV_{REF}n$ – 0.20	V	—
	<= 533 MHz		—	$MV_{REF}n$ – 0.25		
AC input high voltage	>=667 MHz	V_{IHAC}	$MV_{REF}n$ + 0.20	—	V	—
—	<= 533 MHz		$MV_{REF}n$ + 0.25	—		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REF}n$ – 0.175	V	—
AC input high voltage	V_{IHAC}	$MV_{REF}n$ + 0.175	—	V	—

Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR3 mode.

Table 20. DDR3 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V_{IN}	—	—	mV	—
DC Differential Input Voltage	V_{ID}	—	—	mV	—
AC Differential Input Voltage	V_{IDAC}	—	—	mV	—
DC Differential Output Voltage	V_{OH}	—	—	mV	—
AC Differential Output Voltage	V_{OHAC}	—	—	mV	—
AC Differential Cross-point Voltage	V_{IXAC}	—	—	mV	—
Input Midpoint Voltage	V_{MP}	—	—	mV	—

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

Figure 9 shows the GMII transmit AC timing diagram.

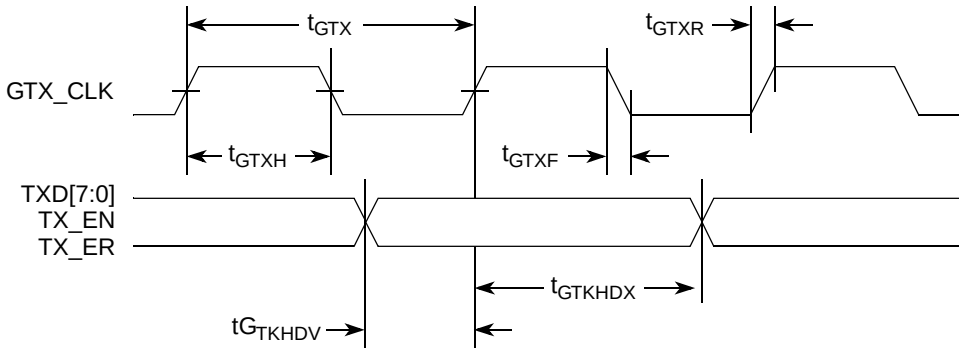


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}[2]	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

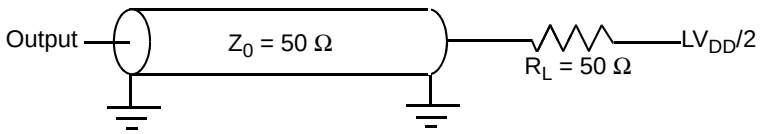


Figure 10. eTSEC AC Test Load

Table 35. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

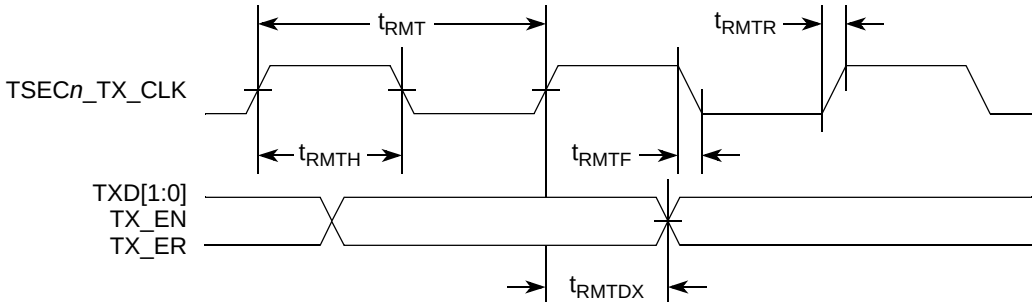


Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns

Figure 30 through Figure 35 show the local bus signals.

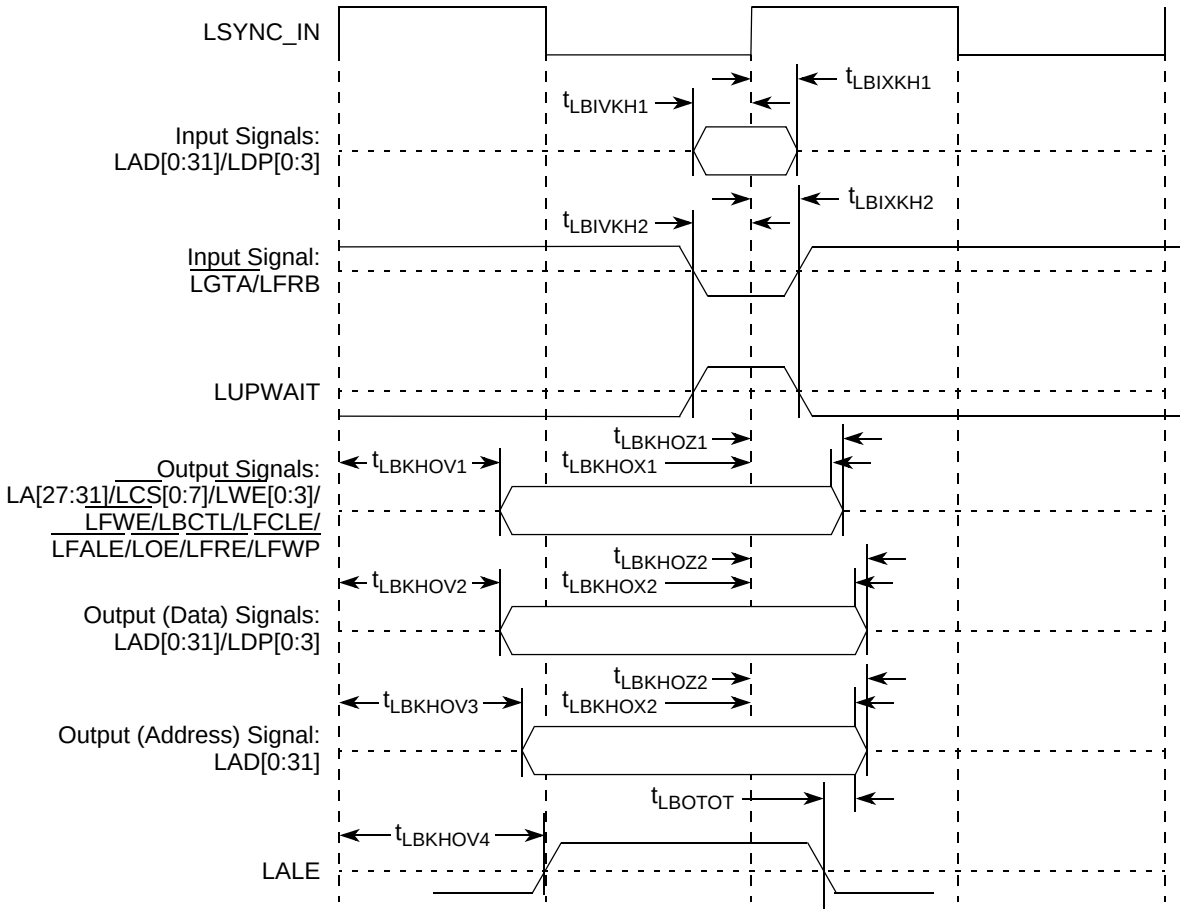


Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

Table 52 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC with PLL disabled.

Table 52. Local Bus General Timing Parameters—PLL Bypassed

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.0	ns	—
Input setup to local bus clock (except LGTA/LUPWAIT)	$t_{LBIVKH1}$	5.8	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.7	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	$t_{LBIXKH1}$	-1.3	—	ns	4, 5

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Table 55. I²C AC Electrical Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 2).

Parameter	Symbol[1]	Min	Max	Unit
Capacitive load for each bus line	Cb	—	400	pF

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8572E provides a delay time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8572E acts as the I2C bus master while transmitting, the MPC8572E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8572E would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8572E as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*.

Figure 40 provides the AC test load for the I²C.

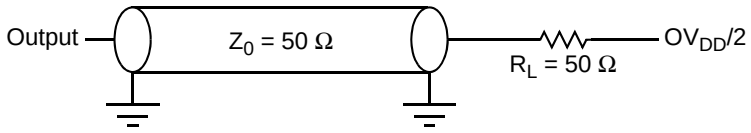


Figure 40. I²C AC Test Load

Figure 41 shows the AC timing diagram for the I²C bus.

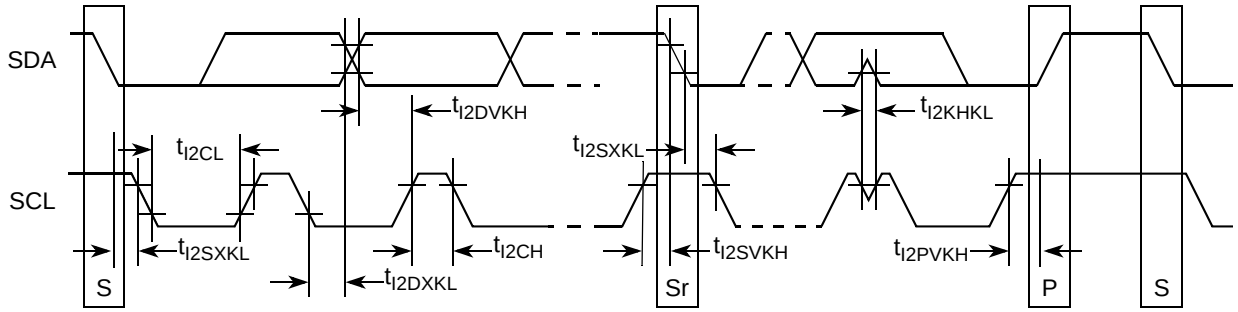


Figure 41. I²C Bus AC Timing Diagram

Table 58 provides the DC electrical characteristics for the GPIO interface operating at BV_{DD} = 1.8 V DC.

Table 58. GPIO DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	1.71	1.89	V
High-level input voltage	V_{IH}	0.65 x BV_{DD}	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.35 x BV_{DD}	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	TBD	TBD	μA
High-level output voltage (I_{OH} = –100 μA)	V_{OH}	BV_{DD} – 0.2	—	V
High-level output voltage (I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.45	—	V
Low-level output voltage (I_{OL} = 100 μA)	V_{OL}	—	0.2	V
Low-level output voltage (I_{OL} = 2 mA)	V_{OL}	—	0.45	V

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications[1]

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.

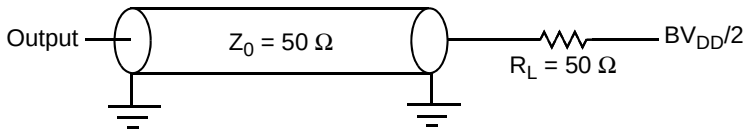


Figure 42. GPIO AC Test Load

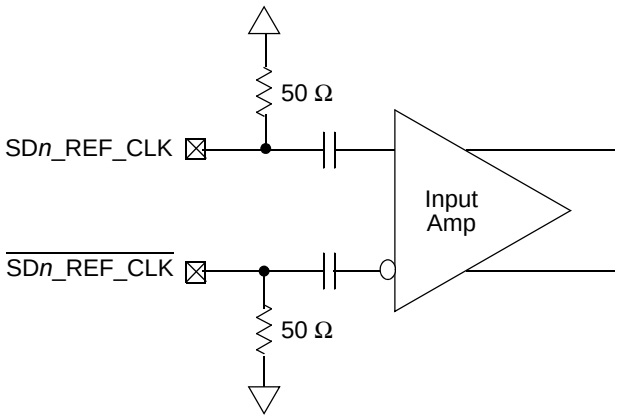


Figure 44. Receiver of SerDes Reference Clocks

15.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8572E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 15.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 45 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 46 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD}n\text{\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 47 shows the SerDes reference clock input requirement for single-ended signaling mode.

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

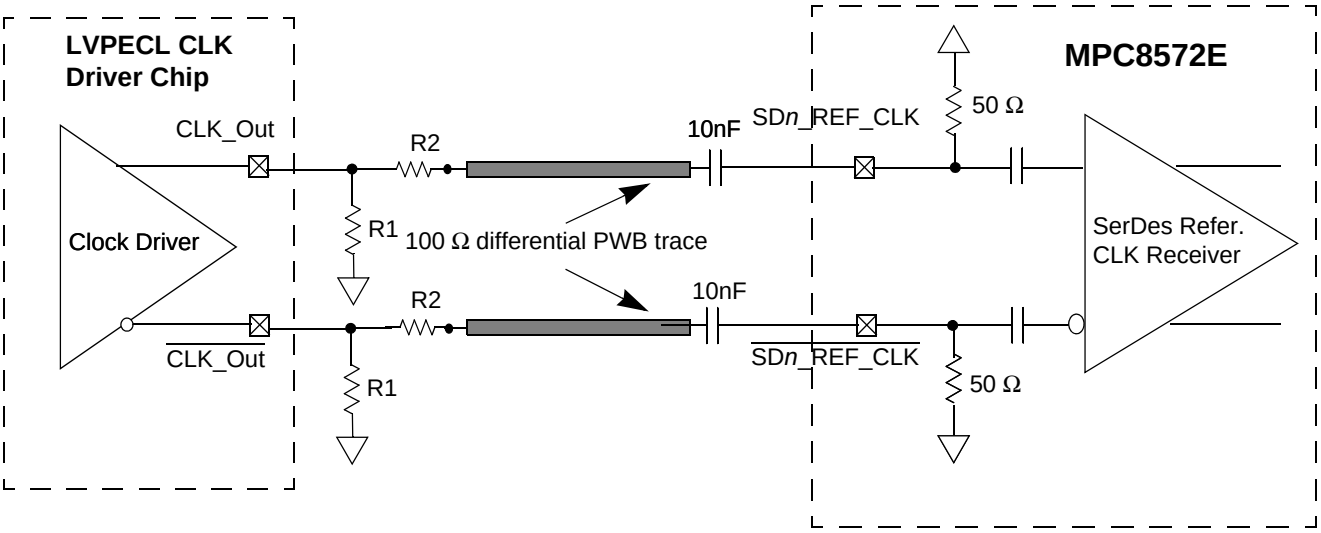


Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

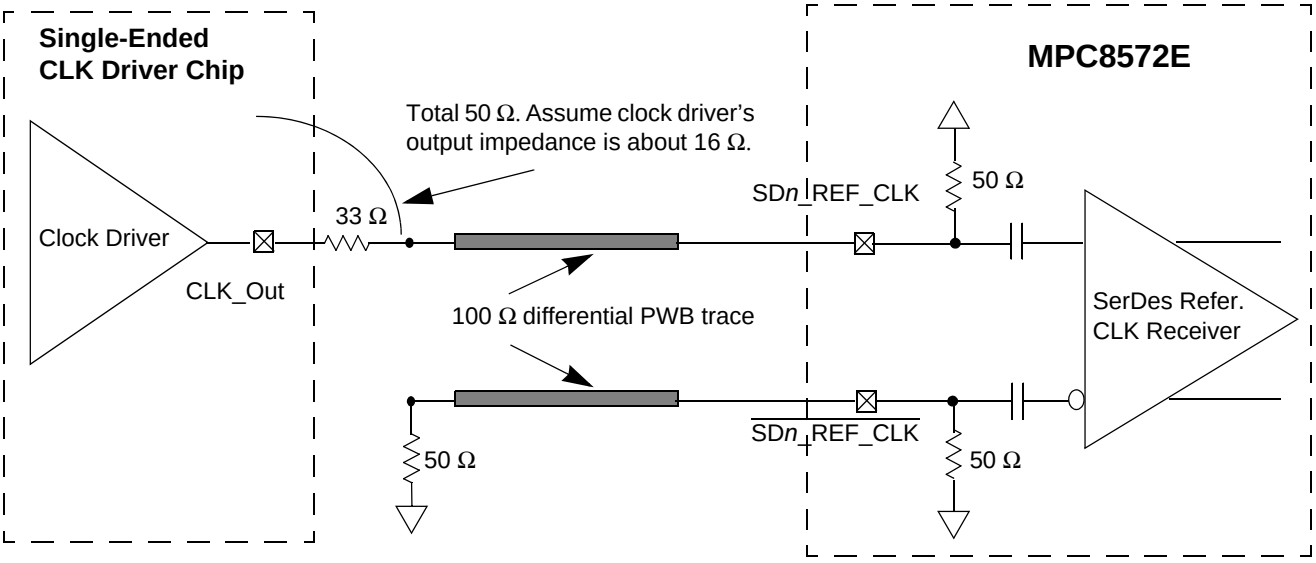


Figure 51. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

Table 62. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2.
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$\|V_{TX-CM-DC\ (during\ L0)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\| <= 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| <= 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\| <= 20$ mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection		—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.

Table 63. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nominal	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

18.2 Mechanical Dimensions of the MPC8572E FC-PBGA

Figure 61 shows the mechanical dimensions of the MPC8572E FC-PBGA package with full lid.

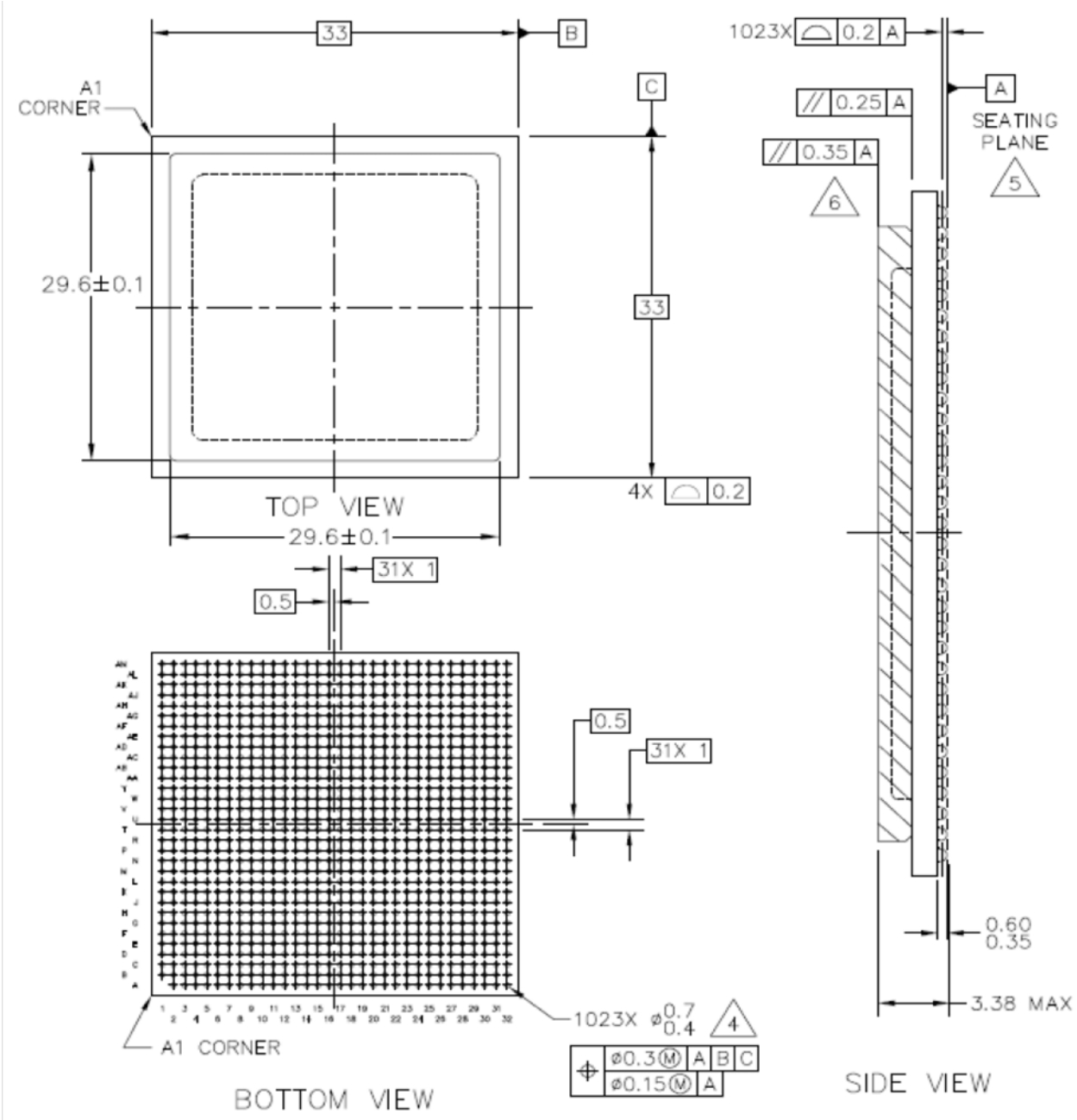


Figure 61. Mechanical Dimensions of the MPC8572E FC-PBGA with Full Lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0]	Receive Data Valid	AL24	I	LV_{DD}	1
TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1]	Receive Data Error	AM29	I	LV_{DD}	1
TSEC1_TX_CLK/FIFO1_TX_CLK	Transmit Clock In	AB20	I	LV_{DD}	1
TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0]	Transmit Enable	AJ24	O	LV_{DD}	1, 22
TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1]	Transmit Error	AK25	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 2					
TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8]	Receive Data	AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20	I	LV_{DD}	1
TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8]	Transmit Data	AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18	O	LV_{DD}	1, 5, 9, 24
TSEC2_COL/FIFO2_TX_FC	Collision Detect/Flow Control	AE19	I	LV_{DD}	1
TSEC2_CRS/FIFO2_RX_FC	Carrier Sense/Flow Control	AJ20	I/O	LV_{DD}	1, 16
TSEC2_GTX_CLK	Transmit Clock Out	AE18	O	LV_{DD}	—
TSEC2_RX_CLK/FIFO2_RX_CLK	Receive Clock	AL23	I	LV_{DD}	1
TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2]	Receive Data Valid	AJ22	I	LV_{DD}	1
TSEC2_RX_ER/FIFO2_RX_ER	Receive Data Error	AD19	I	LV_{DD}	1
TSEC2_TX_CLK/FIFO2_TX_CLK	Transmit Clock In	AC19	I	LV_{DD}	1
TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2]	Transmit Enable	AB19	O	LV_{DD}	1, 22
TSEC2_TX_ER/FIFO2_TX_ERR	Transmit Error	AB17	O	LV_{DD}	1, 5, 9
Three-Speed Ethernet Controller 3					
TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0]	Transmit Data	AG18, AG17, AH17, AH19	O	TV_{DD}	1, 5, 9
TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0]	Receive Data	AG16, AK19, AD16, AJ19	I	TV_{DD}	1

Figure 62 shows the PLL power supply filter circuits.

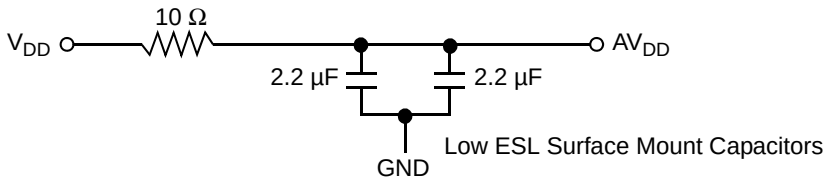
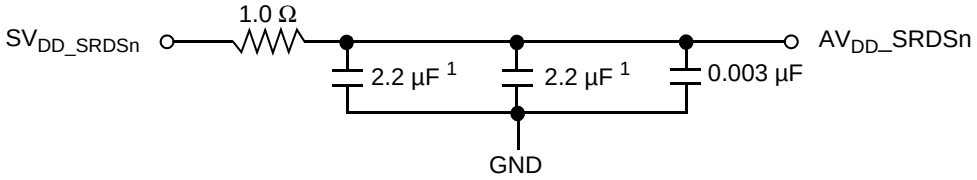


Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD}_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

AV_{DD}_SRDSn should be a filtered version of SV_{DD}_SRDS*n*.

NOTE

Signals on the SerDesn interface are fed from the XV_{DD}_SRDS*n* power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

Table 87. Part Numbering Nomenclature—Rev 2.1

MPC	*nnnn*	*e*	*t*	*l*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = –40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 150- MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included
		Blank = Not included					D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 88. Part Numbering Nomenclature—Rev 1.1.1

MPC	*nnnn*	*e*	*t*	*pp*	*ffm*	*r*

Product Code[1]	Part Identifier	Security Engine	Temperature	Package Sphere Type[2]	Processor Frequency/ DDR Data Rate[3]	Silicon Revision
MPC PPC	8572	E = Included	Blank=0 to 105°C C= –40 to 105°C	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz process or; 667 MT/s DDR datarate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included
		Blank = Not included				B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included

Notes:

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.