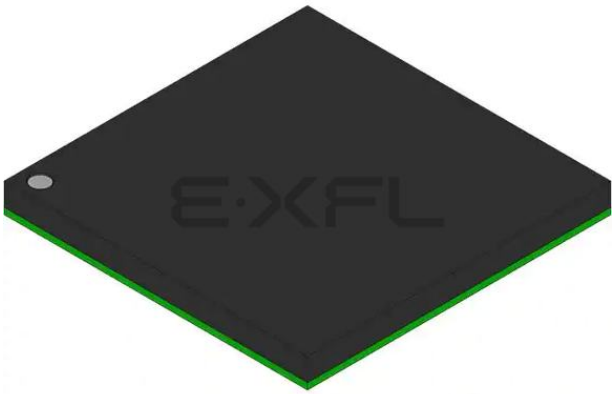

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Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 64x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpxn2120vmg116

3 Pin assignments

3.1 208-ball MAPBGA pin assignments

Figure 4 shows the 208-ball MAPBGA pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	PD0	PG1	PC12	PC9	PC7	PC2	PB13	PB10	PB8	RESET	V_{DDSYN}	XTAL	EXTAL	V_{SSSYN}	V_{SS}	A
B	PD2	PD1	PG0	PC11	PC10	PC8	PC3	PB14	PB11	V_{RC}	V_{RCCTL}	PB9	PB2	PB0	V_{DDA}	V_{RH}	B
C	PD3	PD4	PD14	PC14	PC13	PC5	PC6	PC1	PB15	PB12	PB6	PB4	PB3	PB1	V_{SSA}	V_{RL}	C
D	PD5	PD6	PD15	V_{DD}	PC15	V_{DDE1}	V_{SS}	PC4	PC0	V_{DD}	PB7	PB5	PA10	PA12	PA0	PA14	D
E	PD7	PD8	PE0	PE1									PA11	PA9	PA1	PA15	E
F	PD9	PD10	PE3	PE2									PA13	PA8	PA3	PA2	F
G	PD11	PD12	PE4	V_{SS}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DD}	PA7	PA5	PA4	G
H	PD13	PF0	PE5	V_{DD}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{RCSEL}	PG2	PG6	PA6	H
J	PF1	PF2	TDI	PE8				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DDE3}	PG3	PG7	PG11	J
K	PK1	PK2	JCOMP	V_{DDEMLB}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DD}	PG4	PG8	PG12	K
L	PK0	PE7	TMS	V_{DDE2}									V_{DD33}	PG5	PG9	PG13	L
M	PF4	PE6	TDO	PE9									TEST	PF13	PG10	PG14	M
N	PF6	PF3	PE10	PE11	V_{DD}	PE15	PE14	PH9	PH11	V_{DDE4}	PH15	PJ10	V_{SS}	PF12	PH3	PG15	N
P	PF8	PF5	TCK	PE12	PE13	PK10	PH8	PH10	PH12	PH13	PH14	PJ11	PF15	PF14	PH4	PH1	P
R	PF10	PF7	PF11	PK4	PK6	PK8	PJ0	PJ2	PJ4	PJ6	PJ9	PJ12	PJ14	PH5	PH6	PH2	R
T	V_{SS}	PF9	PK3	PK5	PK7	PK9	PJ1	PJ3	PJ5	PJ7	PJ8	PJ13	PJ15	PH0	PH7	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. PXN20 208-ball MAPBGA (full diagram)

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PB10	PB[10] AN[26] PCS_B[4]	26	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A9
PB11	PB[11] AN[27] PCS_B[5]	27	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B9
PB12	PB[12] AN[28] PCS_C[1]	28	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C10
PB13	PB[13] AN[29] PCS_C[2]	29	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A8
PB14	PB[14] AN[30] PCS_D[3]	30	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B8
PB15	PB[15] AN[31] PCS_D[4]	31	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C9
Port C (16)										
PC0	PC[0] AN[32]	32	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D9
PC1	PC[1] AN[33]	33	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C8
PC2	PC[2] AN[34] EVTI	34	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event In —	I/O I I —	V_{DDE1}	SHA	—	—	A7
PC3	PC[3] AN[35] EVTO	35	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event Out —	I/O I O —	V_{DDE1}	SHA	—	—	B7

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PC15	PC[15] AN[47] MA[2]	47	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I O —	V_{DDE1}	SHA	—	—	D5
Port D (16)										
PD0	PD[0] CNTX_A	48	00 01 10 11	Port D GPIO FlexCAN_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	A2
PD1	PD[1] CNRX_A	49	00 01 10 11	Port D GPIO FlexCAN_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	B2
PD2	PD[2] CNTX_B	50	00 01 10 11	Port D GPIO FlexCAN_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	B1
PD3	PD[3] CNRX_B	51	00 01 10 11	Port D GPIO FlexCAN_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	C1
PD4	PD[4] CNTX_C	52	00 01 10 11	Port D GPIO FlexCAN_C Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C2
PD5	PD[5] CNRX_C	53	00 01 10 11	Port D GPIO FlexCAN_C Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D1
PD6	PD[6] CNTX_D TXD_K SCL_B	54	00 01 10 11	Port D GPIO FlexCAN_D Transmit SCI_K Transmit I^2C_B Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	D2
PD7	PD[7] CNRX_D RXD_K SDA_B	55	00 01 10 11	Port D GPIO FlexCAN_D Receive SCI_K Receive I^2C_B Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	E1
PD8	PD[8] CNTX_E TXD_L SCL_C	56	00 01 10 11	Port D GPIO FlexCAN_E Transmit SCI_L Transmit I^2C_C Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	E2

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PE3	PE[3] RXD_D eMIOS[28]	67	00 01 10 11	Port E GPIO eSCI_D Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	F3
PE4	PE[4] TXD_E eMIOS[27]	68	00 01 10 11	Port E GPIO eSCI_E Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	G3
PE5	PE[5] RXD_E eMIOS[26]	69	00 01 10 11	Port E GPIO eSCI_E Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	H3
PE6	PE[6] TXD_F eMIOS[25]	70	00 01 10 11	Port E GPIO eSCI_F Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	M2
PE7	PE[7] RXD_F eMIOS[24]	71	00 01 10 11	Port E GPIO eSCI_F Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	L2
PE8	PE[8] TXD_G PCS_A[1]	72	00 01 10 11	Port E GPIO eSCI_G Transmit DSPI_A Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	J4
PE9	PE[9] RXD_G PCS_A[4]	73	00 01 10 11	Port E GPIO eSCI_G Receive DSPI_A Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	M4
PE10	PE[10] TXD_H PCS_B[3]	74	00 01 10 11	Port E GPIO eSCI_H Transmit DSPI_B Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	N3
PE11	PE[11] RXD_H PCS_B[2]	75	00 01 10 11	Port E GPIO eSCI_H Receive DSPI_B Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	N4
PE12	PE[12] TXD_J PCS_C[5]	76	00 01 10 11	Port E GPIO eSCI_J Transmit DSPI_C Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	P4
PE13	PE[13] RXD_J PCS_C[3]	77	00 01 10 11	Port E GPIO eSCI_J Receive DSPI_C Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	P5

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PF8	PF[8] SCK_C	88	00 01 10 11	Port F GPIO DSPI_C Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	P1
PF9	PF[9] SOUT_C	89	00 01 10 11	Port F GPIO DSPI_C Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	T2
PF10	PF[10] SIN_C	90	00 01 10 11	Port F GPIO DSPI_C Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	R1
PF11	PF[11] PCS_C[0] PCS_D[5] PCS_A[4]	91	00 01 10 11	Port F GPIO DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R3
PF12	PF[12] SCK_D	92	00 01 10 11	Port F GPIO DSPI_D Serial Clock — —	I/O I/O — —	V_{DDE3}	MH	—	—	N14
PF13	PF[13] SOUT_D	93	00 01 10 11	Port F GPIO DSPI_D Serial Data Out — —	I/O O — —	V_{DDE3}	MH	—	—	M14
PF14	PF[14] SIN_D	94	00 01 10 11	Port F GPIO DSPI_D Serial Data In — —	I/O I — —	V_{DDE3}	SH	—	—	P14
PF15	PF[15] PCS_D[0] PCS_A[5] PCS_B[4]	95	00 01 10 11	Port F GPIO DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select	I/O I/O O O	V_{DDE3}	SH	—	—	P13
Port G (16)										
PG0	PG[0] PCS_A[4] PCS_B[3] AN[48]	96	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	B3
PG1	PG[1] PCS_A[5] PCS_B[4] AN[49]	97	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	A3

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16
Port H (16)										
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PJ1	PJ[1] eMIOS[14] PCS_A[5]	129	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T7
PJ2	PJ[2] eMIOS[13] PCS_B[1]	130	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R8
PJ3	PJ[3] eMIOS[12] PCS_B[2]	131	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T8
PJ4	PJ[4] eMIOS[11] PCS_C[3]	132	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R9
PJ5	PJ[5] eMIOS[10] PCS_C[4]	133	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T9
PJ6	PJ[6] eMIOS[09] PCS_D[5]	134	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R10
PJ7	PJ[7] eMIOS[08] PCS_D[1]	135	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T10
PJ8	PJ[8] eMIOS[07]	136	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T11
PJ9	PJ[9] eMIOS[06]	137	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R11
PJ10	PJ[10] eMIOS[05]	138	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N12
PJ11	PJ[11] eMIOS[04]	139	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P12

3.2.1 Power and ground supply summary

Table 4. PXN20 power/ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations
			208
V_{DD}	Internal Logic Power	1.2 V	D4, D10, H4, G13, K13, N5
V_{DDE1}	External I/O Power	3.3–5.0 V	D6
V_{DDE2}			L4
V_{DDE3}			J13
V_{DDE4}			N10
V_{DDA}	Analog Power	3.3–5.0 V	B15
V_{DD33}	3.3 V I/O Power	3.3 V	L13
V_{DDEMLB}	Media Local Bus Power	2.5 or 3.3 V	K4
V_{RCSEL}	Voltage Regulator Select	V_{SSA} / V_{DDA}	H13
V_{RC}	Voltage Regulator Control Voltage	3.3–5.0 V	B10
V_{RCCTL}	Voltage Regulator Control Output	—[2]	B11
V_{DDSYN}	Clock Synthesizer Power	3.3 V	A12
V_{RH}	Analog High Voltage Reference	3.3–5.0 V	B16
V_{RL}	Analog Low Voltage Reference	0 V	C16
V_{SS}	Ground	0 V	A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16
V_{SSA}	Analog Ground	0 V	C15
V_{SSSYN}	Clock Synthesizer Ground	0 V	A15

1 Nominal voltages.

2 Base current to external NPN power transistor. Voltage may vary.

4 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the PXN20.

4.1 Maximum ratings

Table 5. Absolute maximum ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage[2]	V_{DD}	–0.3	1.32[3]	V
2	3.3 V Clock Synthesizer Voltage[2, 4]	V_{DDSYN}	–0.3	3.6	V
3	3.3 V I/O Buffer Voltage [2, 4]	V_{DD33}	–0.3	3.6	V
4	3.3–5.0 V Voltage Regulator Control Voltage [2, 5, 6]	V_{RC}	–0.3	5.5	V
5	3.3–5.0 V Analog Supply Voltage (reference to V_{SSA}) [2, 5]	V_{DDA}	–0.3	5.5	V
6	3.3–5.0 V External I/O Supply Voltage [2, 5, 7]	V_{DDE1}[8] V_{DDE2}[8] V_{DDE3}[8] V_{DDE4}[8]	–0.3 –0.3 –0.3 –0.3	5.5 5.5 5.5 5.5	V
7	2.5–3.3 V External I/O Supply Voltage (MLB) [2, 4]	V_{DDEMLB}[8]	–0.3	3.6	V
9	DC Input Voltage[9] V_{DDE1}, V_{DDE2}, V_{DDE3}, V_{DDE4} V_{DDEMLB}, V_{DDENEX}	V_{IN}	 –1.0[10] –1.0[9]	 V_{DDEx} + 0.3 V[11] V_{DDEx} + 0.3 V[10]	V
10	Analog Reference High Voltage	V_{RH}	–0.3	Minimum of 5.5 or V_{DDA} + 0.3	V
11	Analog Reference Low Voltage	V_{RL}	–0.3	5.5	V
12	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
13	V_{SS} to V_{SSSYN} Differential Voltage	$V_{SS} – V_{SSSYN}$	–100	100	mV
14	Maximum DC Digital Input Current[12] (per pin, applies to all digital F, MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
15	Maximum DC Analog Input Current[13] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
16	Storage Temperature Range	T_{STG}	–55.0	150.0	°C
17	Maximum Solder Temperature[14]	T_{SDR}	—	235.0	°C
18	Moisture Sensitivity Level[15]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 VRC cannot be 100mV higher than VDDA. VDDSYN and VDD33 cannot be 100 mV higher than VRC.

7 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDEx}.

4.3 ESD characteristics

Table 7. ESD ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		750 (corner pins)	V
		250 (all other pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4 VRC electrical specifications

Table 8. VRC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Units
1	Current which can be sourced by V_{RCCTL}	I_V_{RCCTL}	6.25 µA	20 mA	—
2	Minimum Required Gain from external circuit: I_{DD} / I_V_{RCCTL} (@V_{DD} = 1.32 V)[1] –40°C 25°C 150°C	BETA	 50 50 50	 500	

1 Assumes “typical usage” currents which will vary with application.

4.5 DC electrical specifications

Table 9. DC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Maximum Operating Temperature Range — Die Junction Temperature	T_J	–40.0	150.0	^oC
2	3.3 V Clock Synthesizer Voltage[1]	V_{DDSYN}	3.0	3.6	V
3	3.3 V I/O Buffer Voltage[1]	V_{DD33}	3.0	3.6	V
4	3.3–5.0 V Voltage Regulator Reference Voltage[1] V_{RCSEL} = V_{SSA} V_{RCSEL} = V_{DDA}	V_{VRC}	 3.0 4.5	 3.6 5.5	V
5	3.3–5.0 V Analog Supply Voltage	V_{DDA}	maximum of 3.0 V or V_{VRC} – 0.1	5.5	V

2 $V_{DDE1} – V_{DDE4}$ are separate power segments and may be powered independently with no differential voltage constraints between the power segments. $V_{DDE1} – V_{DDE3}$ pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the V_{DDE} level, resulting in inaccurate ADC results if the V_{DDE} voltage level is less than V_{DDA}.

3 When $V_{RCSEL} = V_{DDA}$ (high), the internally generated V_{DD33} voltage may be used to power V_{DDEMLB} as long as the PK[0:2] pads remain in the disabled default state with their output buffers, input buffers, and pull devices disabled.

4 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

5 The IHA pads are related to V_{DDA}.

6 Characterization Based Capability:
IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with V_{DDE} = 3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 1.62 V.

7 Characterization Based Capability:
IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with V_{DDEH} = 4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with V_{DDEH} = 3.0 V

8 All V_{OL}/V_{OH} values 100% tested with ±2 mA load.

9 Absolute value of current, measured at V_{IL} and V_{IH}.

10 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH. Leakage specification guaranteed only when power supplies are within specified operating conditions.

11 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

4.6 Operating current specifications

Table 10. Operating currents

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$	—	—	—	—
1	V_{DDE} Current $V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V V_{DDEMLB} @ 2.375 V – 3.6 V Static[2] Dynamic[3]	I_{DDE}	 0 Note 3	 30 25	 µA mA
2	V_{DDA} Current V_{DDA} @ 3.0 V – 5.5 V Run mode Sleep mode – Optional 32 kHz osc enabled	I_{DDA}	 1 20 +5	 30 50 +15	 mA µA µA
3	V_{RH} Current V_{RH} @ 3.0 V – 5.5 V Run mode Sleep mode	I_{RH}	 300 1	 700 30	 µA µA
4	V_{DD33} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode	I_{DD33}	 10 10	 20 20	 mA µA

Table 10. Operating currents (continued)

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
5	V_{DDSYN} Current V_{DD33} @ 3.0 V – 3.6 V	I_{DDSYN}			
	Run mode		5	10	mA
	Sleep mode		1	20	µA
	– Optional[4] 4–40 MHz osc enabled w/ no clock		+150	+350	µA
	– Optional[4] 4–40 MHz osc enabled w/ clock		+300	+400	µA
6	V_{RC} Current (excluding I_{DD}, I_{DD33}, I_{DDSYN})[5] V_{RC} @ 3.135 V – 5.5 V	I_{RC}			
	Run mode		1	10	mA
	Sleep mode		0	10	µA
	– Optional[4] 16MIRC enabled		+40	+60	µA
7	V_{DD} Current V_{DD} @ 1.08 V – 1.32 V	I_{DD}			
	Run mode (Maximum @ 116 MHz)[6]		200	340	mA
	Sleep mode		100	900	µA
	– Optional[4] 128KIRC enabled		+5	+10	µA
	– Optional[4] 16MIRC enabled		+200	+220	µA
	– Optional[4] 32 kHz osc enabled		+5	+20	µA
	– Optional[4] 4–40 MHz osc enabled w/ no clock		+5	+20	µA
	– Optional[4] 4–40 MHz osc enabled w/ clock		+150	+200	µA
	– Optional[4] 32 KB RAM		+10	+150	µA
	– Optional[4] 64 KB RAM		+20	+300	µA
	– Optional[4] 128 KB RAM		+40	+600	µA

1 Typ – Nominal voltage levels and functional activity. Max – Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application-specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 11 for more information.

4 Optional currents are values that should be added to their respective current specifications to obtain the actual value for that specification when the optional function is active. The plus sign (+) in the Typ and Max columns indicates these optional currents. For example, V_{DDSYN} in Sleep mode draws 1 .µA (typ). With the optional 4–40 MHz osc enabled w/ no clock, add 150 .µA for a total of 151 .µA (typ).

5 V_{RC} Current excluding the current supply to V_{DD33}, V_{DDSYN} and V_{DD} from V_{RC}.

6 Maximum supply current transition: 50mA per 20µS observation window.

[2] The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.

[3] "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

[4] This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

[5] Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

[6] Modulation depth selected must not result in f_{PLL} value greater than the f_{PLL} maximum specified value.

[7] Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.

[8] Depth tolerance is the programmed modulation depth ±0.25% of f_{SYS}.

[9] See the Block Guide for VCO frequency synthesis equations.

[10] Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

4.11 ADC electrical characteristics

Table 20. ADC conversion specifications (operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Analog High Reference Voltage	V_{RH}	V_{DDA} – 0.5	V_{DDA}	V
2	Analog Low Reference Voltage	V_{RL}	0	0.5	V
3	Analog Input Voltage	AV_{IN}	V_{RL}	V_{RH}	V
4	Sampling Frequency	F_S	—	1.53	MHz
5	Maximum ADC Clock Frequency	F_{MAX}	—	60	MHz
6	Sampling Time V_{DDA} = 3.0 V – 3.6 V V_{DDA} > 3.6 V – 5.5 V	t_S	 250 125	—	ns
7	Differential Non Linearity	DNL	–1.0	1.0	LSB
8	Integral Non Linearity	INL	–1.5	1.5	LSB
9	Offset Error	OFS	–1.0	1.0	LSB
10	Gain Error	GNE	–2.0	2.0	LSB
11	Total Unadjusted Error [1]	TUE	–2.0	2.0	LSB

[1] TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding V_{DDE} segment.

4.12 Flash memory electrical characteristics

Table 21. Flash program and erase specifications[1]

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	—	500	µs
2	Page (128 bits and 256 bits) Program Time[4]	$t_{pprogram}$	—	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	2600	7500	ms

Table 24. De-rated pad AC specifications (3.3 V, 3.3 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6], (ns)	Load Drive (pF)
3	Fast[8]	00	2.5	1.2	10
		01		1.2	20
		10		1.2	30
		11		1.2	50
4	Input	N/A	3/3	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 3.0 – 3.6 V, V_{DDEH} = 3.0 – 3.6 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 Delay and rise/fall are measured to 20% or 80% of the respective signal.

6 This parameter is guaranteed by characterization before qualification rather than 100% tested.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

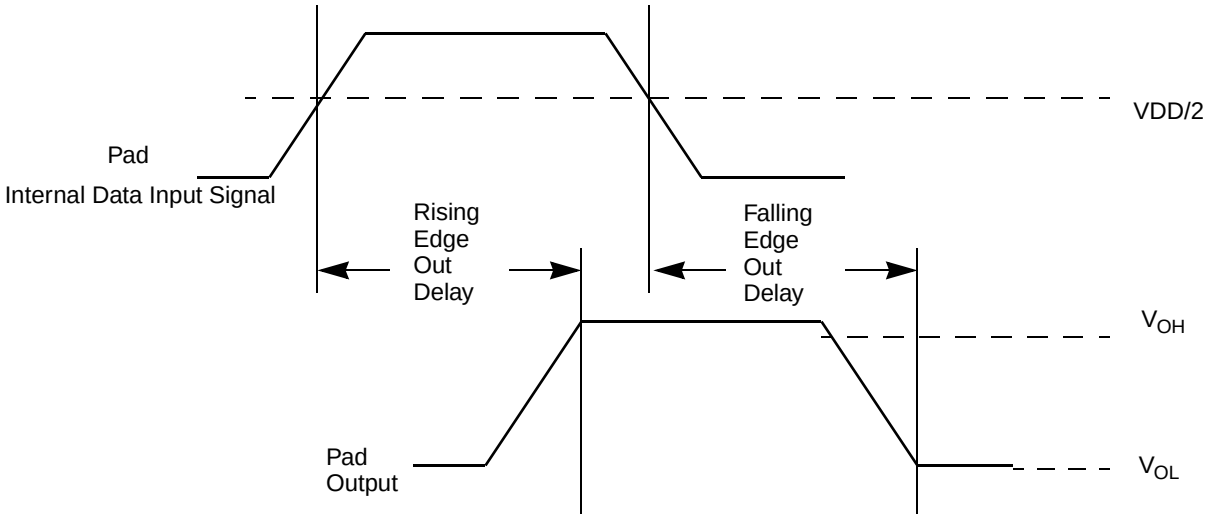


Figure 6. Pad output delay

4.14.3 JTAG (IEEE 1149.1) interface

Table 27. JTAG interface timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at $V_{DDE}/2$)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	25	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

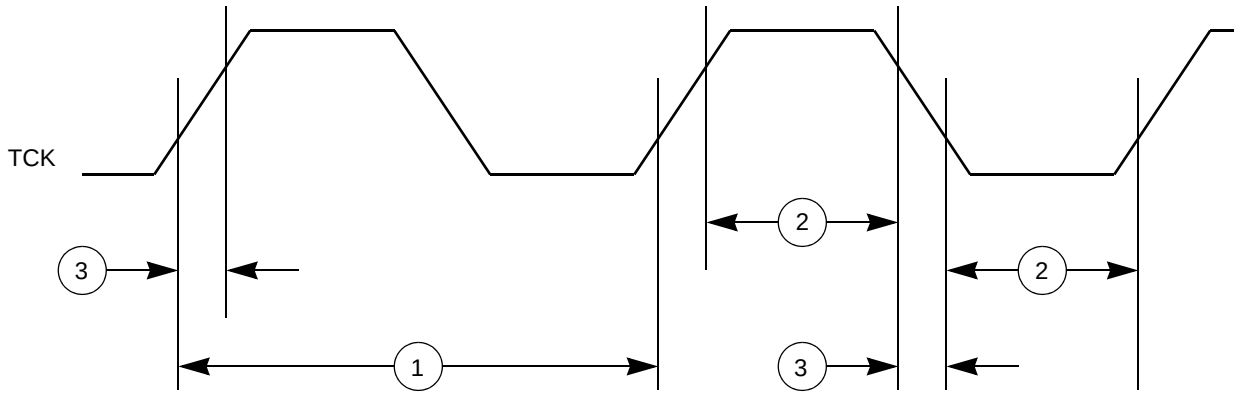


Figure 9. JTAG test clock input timing

4.14.4 Enhanced Modular I/O Subsystem (eMIOS)

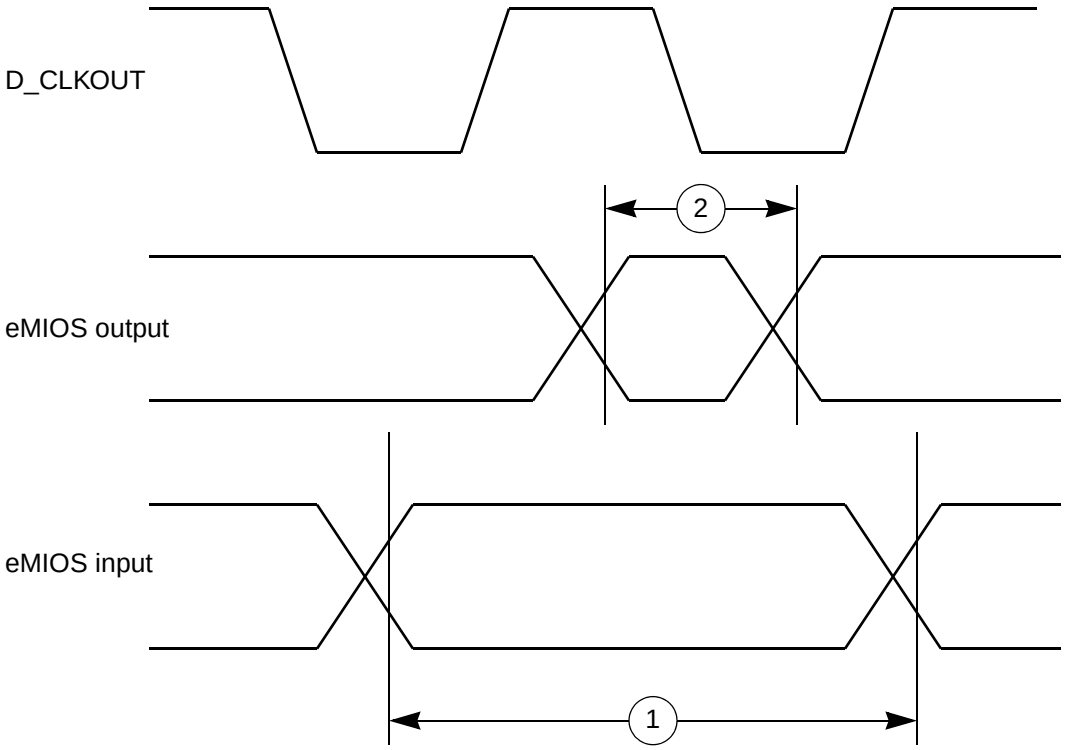
Table 28. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1[2]	—	t_{CYC}

1 eMIOS timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and CL = 30 pF with SRC = 0b11.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 13. eMIOS timing



1 The Controller can shut off MLBCLK to place MLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

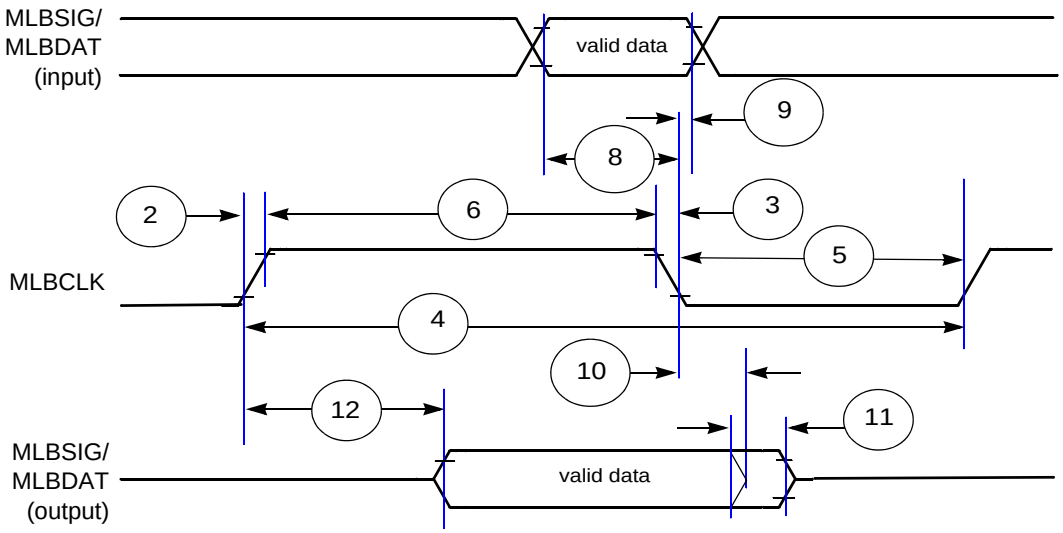


Figure 23. Media Local Bus (MLB) timing

4.14.7 Fast Ethernet Controller (FEC) interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.14.7.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 33. MII receive signal timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

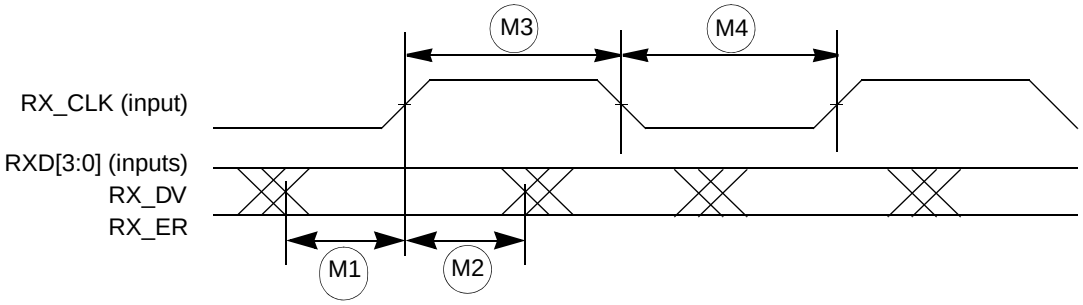


Figure 24. MII receive signal timing diagram

4.14.7.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 34. MII transmit signal timing[1]

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1 Output pads configured with SRC = 0b11.

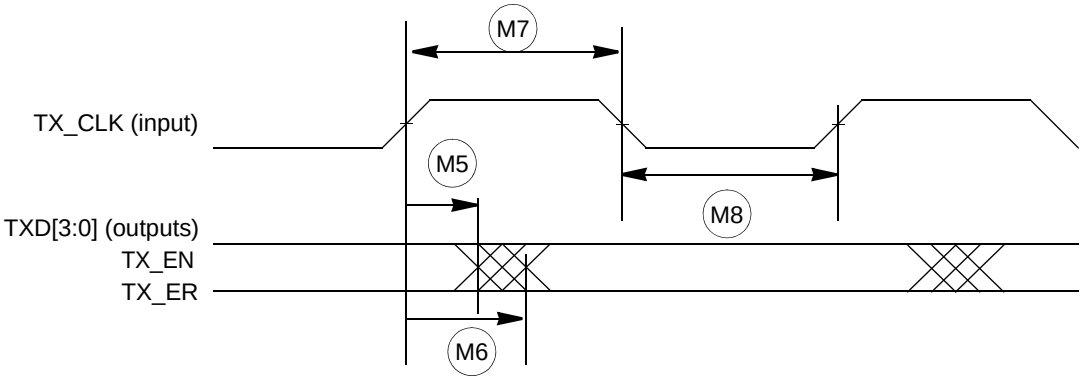


Figure 25. MII transmit signal timing diagram

4.14.7.3 MII async inputs signal timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1 Output pads configured with SRC = 0b11.

5 Package characteristics

5.1 Package mechanical data

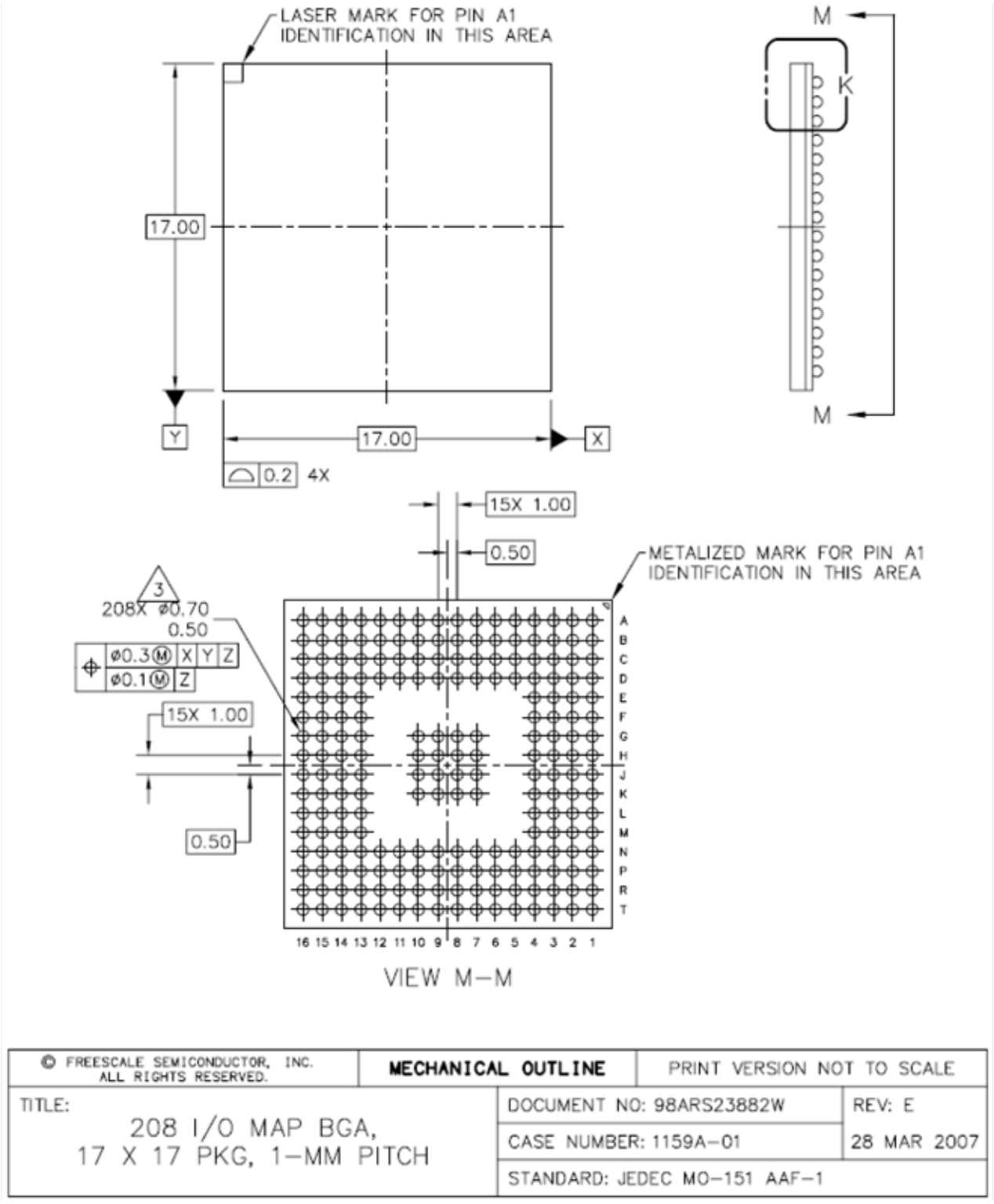
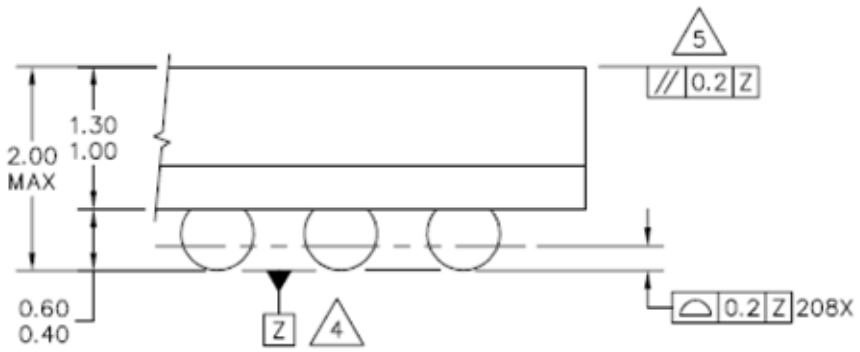


Figure 28. 208 MAPBGA package mechanical drawing



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
   MAP BGA: 5253
   MAP BGA PGE DIE: 5371

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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: E
	CASE NUMBER: 1159A–01	28 MAR 2007
	STANDARD: JEDEC MO–151 AAF–1	

Figure 29. 208 MAPBGA package detail