Infineon Technologies - MB95F108AJWPMC-GE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f108ajwpmc-ge1

■ HANDLING DEVICES

- Preventing Latch-up

  Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

  Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

  When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

  Also, take care to prevent the analog power supply voltage (AV_{CC}, AVR) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

- Stable Supply Voltage

  Supply voltage should be stabilized.

  A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

  For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz/60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

- Serial communication

  There is a possibility to receive wrong data due to noise or other causes on the serial communication.

  Therefore, design a printed circuit board so as to avoid noise.

  Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ PIN CONNECTION

- Treatment of Unused Input Pin

  Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

- Treatment of Power Supply Pins on A/D Converter

  Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

  Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 μF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

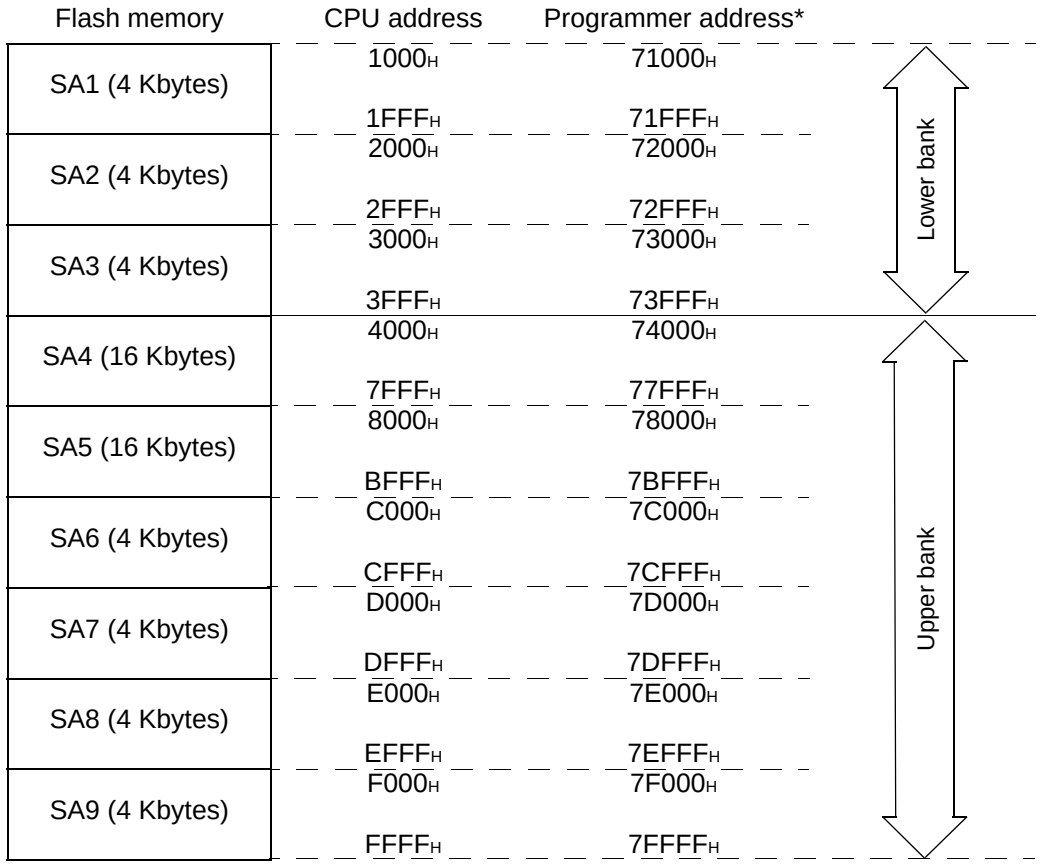
Package	Applicable adapter model	Parallel programmers
FPT-64P-M24	TEF110-108F35AP	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-64P-M23	TEF110-108F36AP	

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

• MB95F108AMS/F108ANS/F108AJS/F108AMW/F108ANW/F108AJW (60 Kbytes)



*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

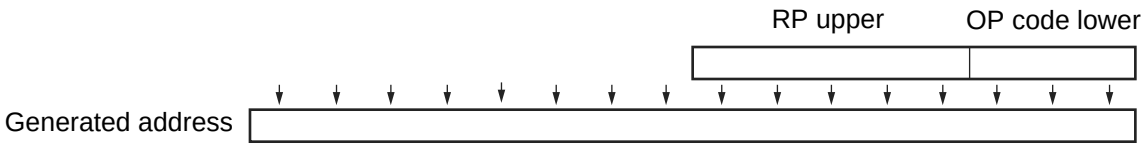
• Programming Method

1) Set the type code of the parallel programmer to “17222”.
2) Load program data to programmer addresses 71000_H to $7FFFF_H$.
3) Programmed by parallel programmer

	Flash	RAM	Address #1	Address #2
MB95F104AMS/F104ANS/F104AJS	16 Kbytes	512 bytes	0280H	C000H
MB95F104AMW/F104ANW/F104AJW				
MB95F106AMS/F106ANS/F106AJS	32 Kbytes	1 Kbyte	0480H	8000H
MB95F106AMW/F106ANW/F106AJW				
MB95F108AMS/F108ANS/F108AJS	60 Kbytes	2 Kbytes	0880H	1000H
MB95F108AMW/F108ANW/F108AJW				

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX_B (no effect to mapping)	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is set to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low = no interruption

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

Address	Register abbreviation	Register name	R/W	Initial value
002B$_H$	DDRG	Port G direction register	R/W	00000000$_B$
002C$_H$	—	(Disabled)	—	—
002D$_H$	PUL1	Port 1 pull-up register	R/W	00000000$_B$
002E$_H$	PUL2	Port 2 pull-up register	R/W	00000000$_B$
002F$_H$	PUL3	Port 3 pull-up register	R/W	00000000$_B$
0030$_H$	PUL4	Port 4 pull-up register	R/W	00000000$_B$
0031$_H$	PUL5	Port 5 pull-up register	R/W	00000000$_B$
0032$_H$	PUL7	Port 7 pull-up register	R/W	00000000$_B$
0033$_H$	—	(Disabled)	—	—
0034$_H$	PULE	Port E pull-up register	R/W	00000000$_B$
0035$_H$	PULG	Port G pull-up register	R/W	00000000$_B$
0036$_H$	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000$_B$
0037$_H$	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000$_B$
0038$_H$	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000$_B$
0039$_H$	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000$_B$
003A$_H$	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000$_B$
003B$_H$	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000$_B$
003C$_H$	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000$_B$
003D$_H$	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000$_B$
003E$_H$	TMCSRH0	16-bit reload timer control status register (Upper byte) ch.0	R/W	00000000$_B$
003F$_H$	TMCSRL0	16-bit reload timer control status register (Lower byte) ch.0	R/W	00000000$_B$
0040$_H$, 0041$_H$	—	(Disabled)	—	—
0042$_H$	PCNTH0	16-bit PPG status control register (Upper byte) ch.0	R/W	00000000$_B$
0043$_H$	PCNTL0	16-bit PPG status control register (Lower byte) ch.0	R/W	00000000$_B$
0044$_H$	PCNTH1	16-bit PPG status control register (Upper byte) ch.1	R/W	00000000$_B$
0045$_H$	PCNTL1	16-bit PPG status control register (Lower byte) ch.1	R/W	00000000$_B$
0046$_H$, 0047$_H$	—	(Disabled)	—	—
0048$_H$	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000$_B$
0049$_H$	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$	EIC01	External interrupt circuit control register ch.8/ch.9	R/W	00000000$_B$
004D$_H$	EIC11	External interrupt circuit control register ch.10/ch.11	R/W	00000000$_B$

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(Vcc = AVcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.15	1.10	mA	
	I_{CCH}		V_{CC} = 5.5 V Sub stop mode T_A = + 25 °C	—	3.5	20	µA	Main stop mode for single clock product
	I_{LVD}	V_{CC}	Current consumption for low voltage detection circuit only	—	38	50	µA	
	I_{CSV}		At oscillating 100 kHz current consumption of internal CR oscillator	—	20	36	µA	
	I_A	AVcc	V_{CC} = 5.5 V F_{CH} = 16 MHz At operating of A/D conversion	—	2.4	4.7	mA	
	I_{AH}		V_{CC} = 5.5 V F_{CH} = 16 MHz At stopping A/D conversion T_A = + 25 °C	—	1	5	µA	

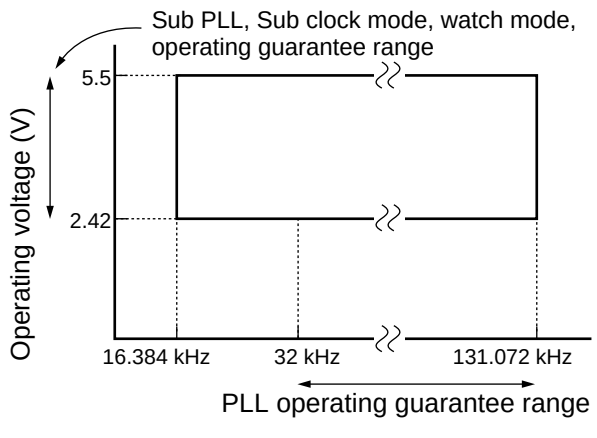
*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR).

*2 : Single clock products only

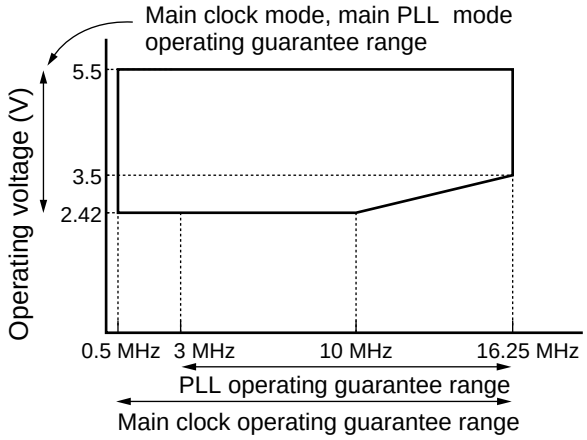
*3 : Product without clock supervisor only

*4 :
- The power-supply current is determined by the external clock. When the low voltage detection option is selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) to the specified value. Also, when both low voltage detection option and clock supervisor are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) and current consumption of internal CR oscillator (I_{CSV}) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

- Operating voltage – Operating frequency (T_A = – 40 °C to + 85 °C)
  - MB95F104AMS/F104ANS/F104AJS/F106AMS/F106ANS/F106AJS/F108AMS/F108ANS/F108AJS/F104AMW/ MB95F104ANW/F104AJW/F106AMW/F106ANW/F106AJW/F108AMW/F108ANW/F108AJW

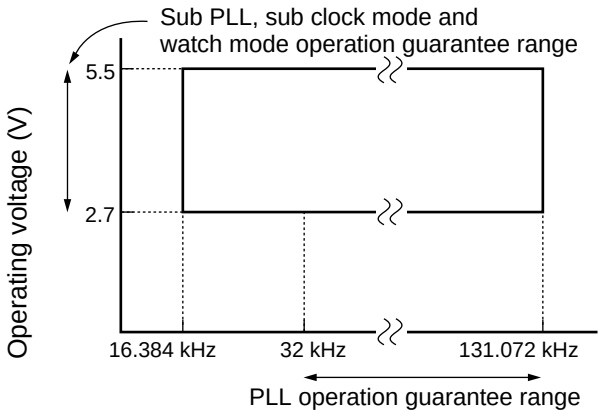


Source clock frequency (F_{SPL})

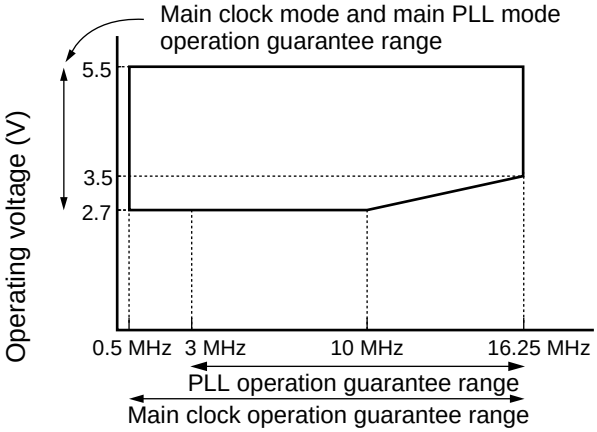


Source clock frequency (F_{SP})

- Operating voltage – Operating frequency (T_A = + 5 °C to + 35 °C)
  - MB95FV100D-103



Source clock frequency (F_{SPL})



Source clock frequency (F_{SP})

(3) External Reset

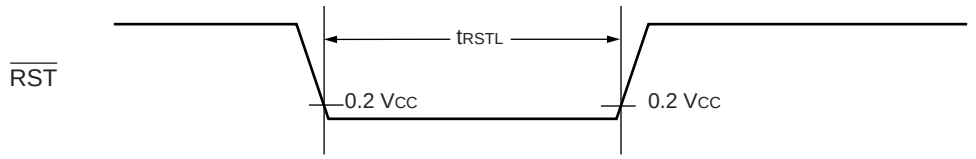
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode
		100	—	µs	At timebase timer mode

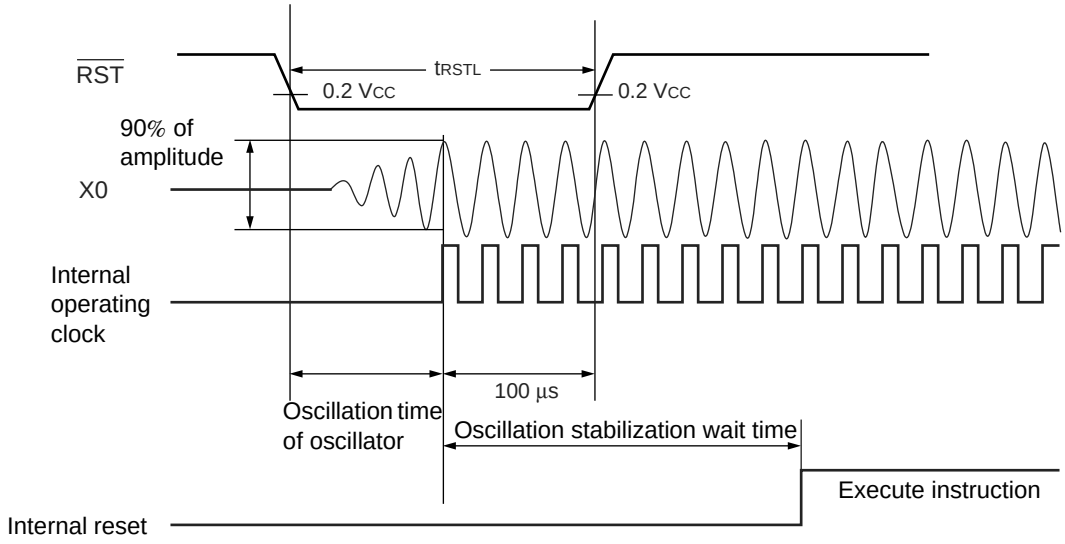
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



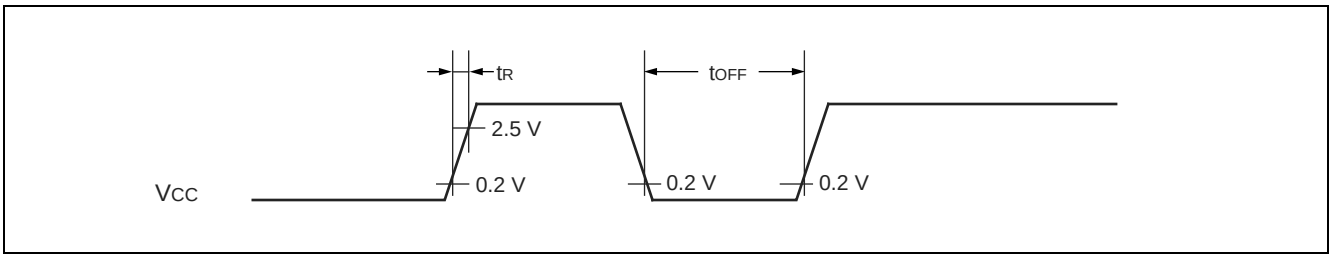
• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



(4) Power-on Reset

(AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below

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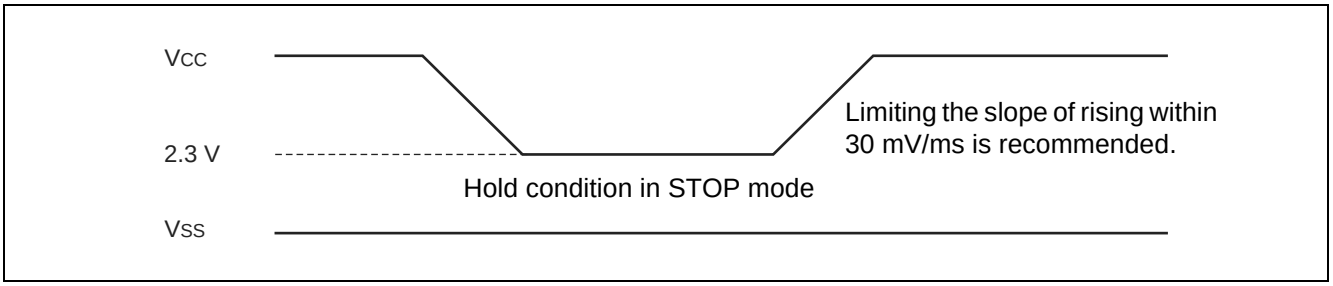
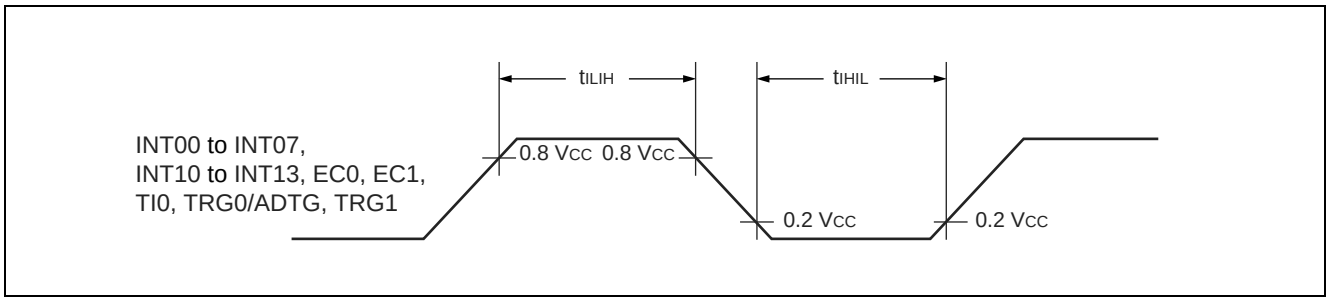


(5) Peripheral Input Timing

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, INT10 to INT13, EC0, EC1, TI0, TRG0/ADTG, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



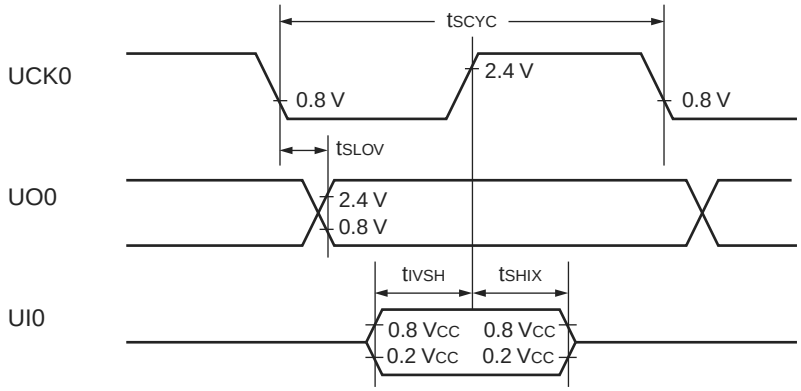
(6) UART/SIO, Serial I/O Timing

(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

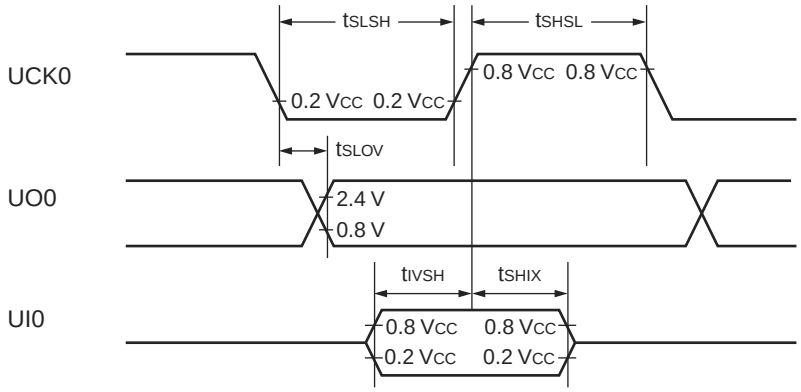
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+ 190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

• Internal shift clock mode



• External shift clock mode



Sampling at the rising edge of sampling clock *1 and enabled serial clock delay *2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

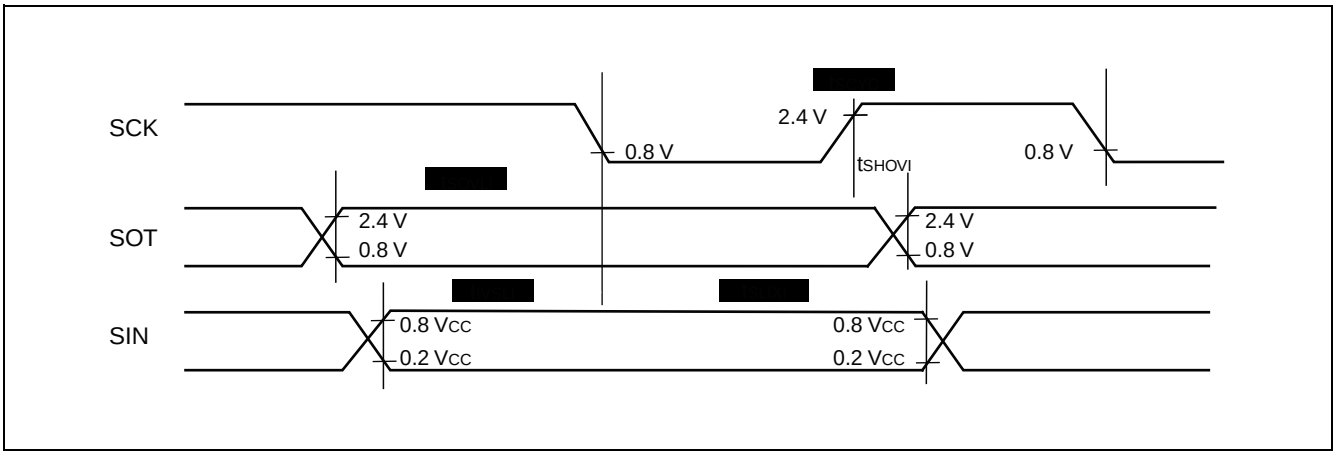
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



Sampling at the falling edge of sampling clock *1 and enabled serial clock delay *2

(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

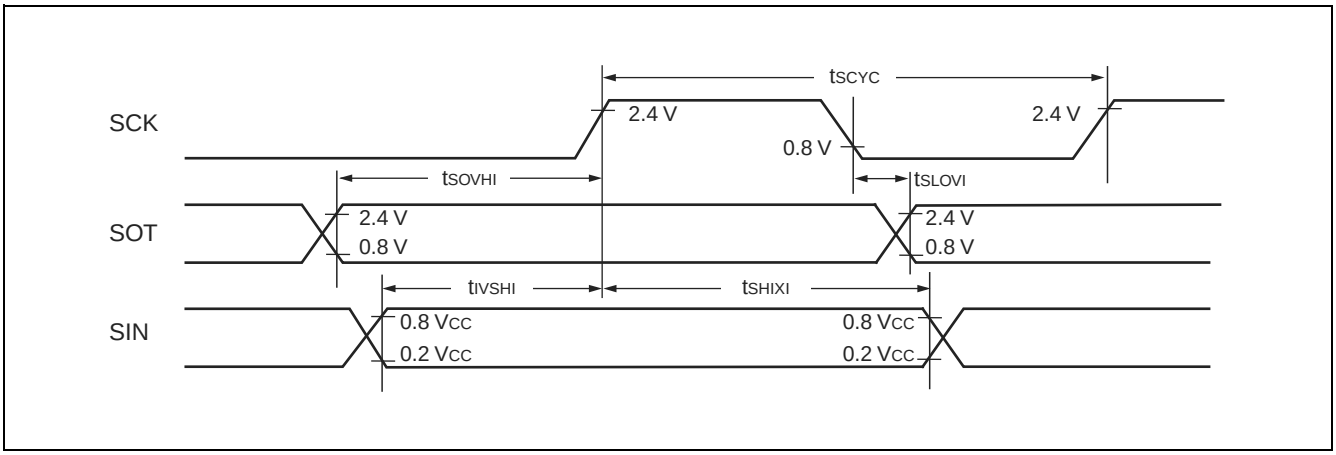
(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		− 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



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(Vcc = 5.0 V ± 10%, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Data hold time	$t_{HD;DAT}$	SCL0 SDA0	R = 1.7 kΩ, C = 50 pF*1	0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{MCLK} − 20	—	ns	At reception
SDA↓→SCL↑ (at wake-up function)	t_{WAKEUP}	SCL0 SDA0		Oscillation stabilization wait time + 2 t_{MCLK} − 20	—	ns	

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 :
- Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR0) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR0) .
- Actual timing of I²C is determined by m and n values set by the machine clock (t_{MCLK}) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n limits the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n limits the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

5. A/D Converter

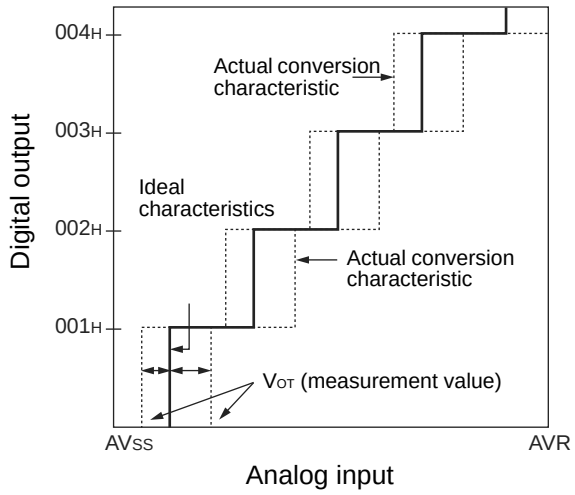
(1) A/D Converter Electr ical Characteristics

(AVcc = Vcc = 4.0 V to 5.5 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

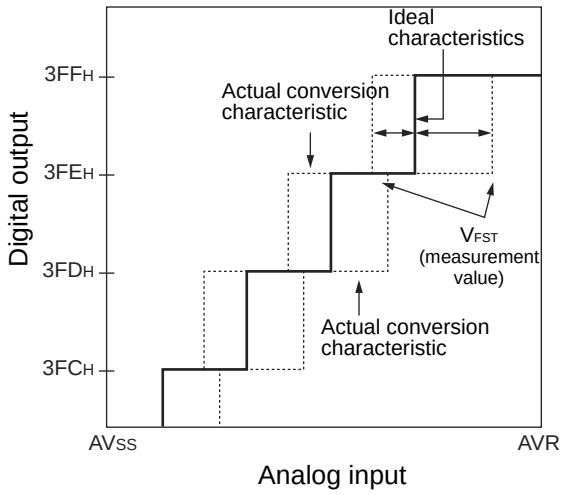
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3.0	—	+ 3.0	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AVss − 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ AVcc < 4.5 V, At external impedance < 2.4 kΩ
Analog input current	I_{AIN}	− 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AVss	—	AVR	V	
Reference voltage	—	AVss + 4.0	—	AVcc	V	AVR pin
Reference voltage supply current	I_R	—	600	900	µA	AVR pin, During A/D operation
	I_{RH}	—	—	5	µA	AVR pin, At stop mode

(Continued)

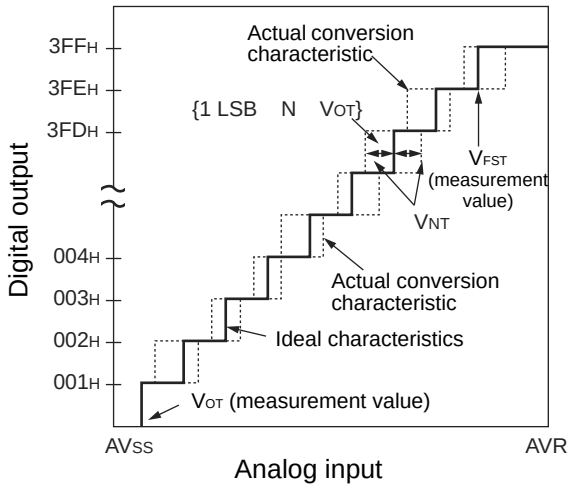
Zero transition error



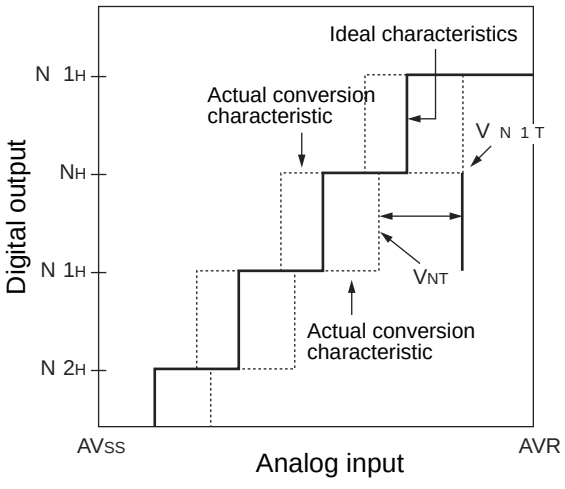
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

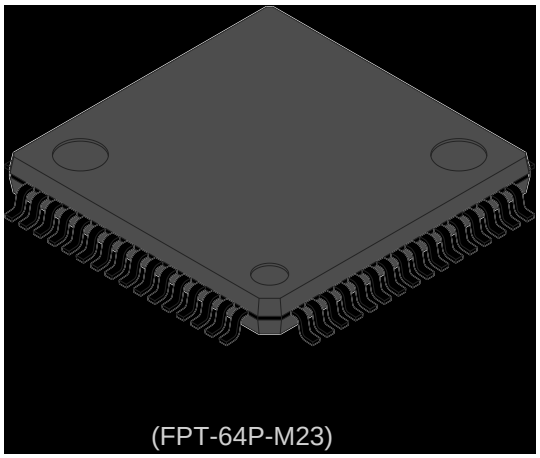
N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N – 1) to N.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AVR – 1.5 LSB [V]

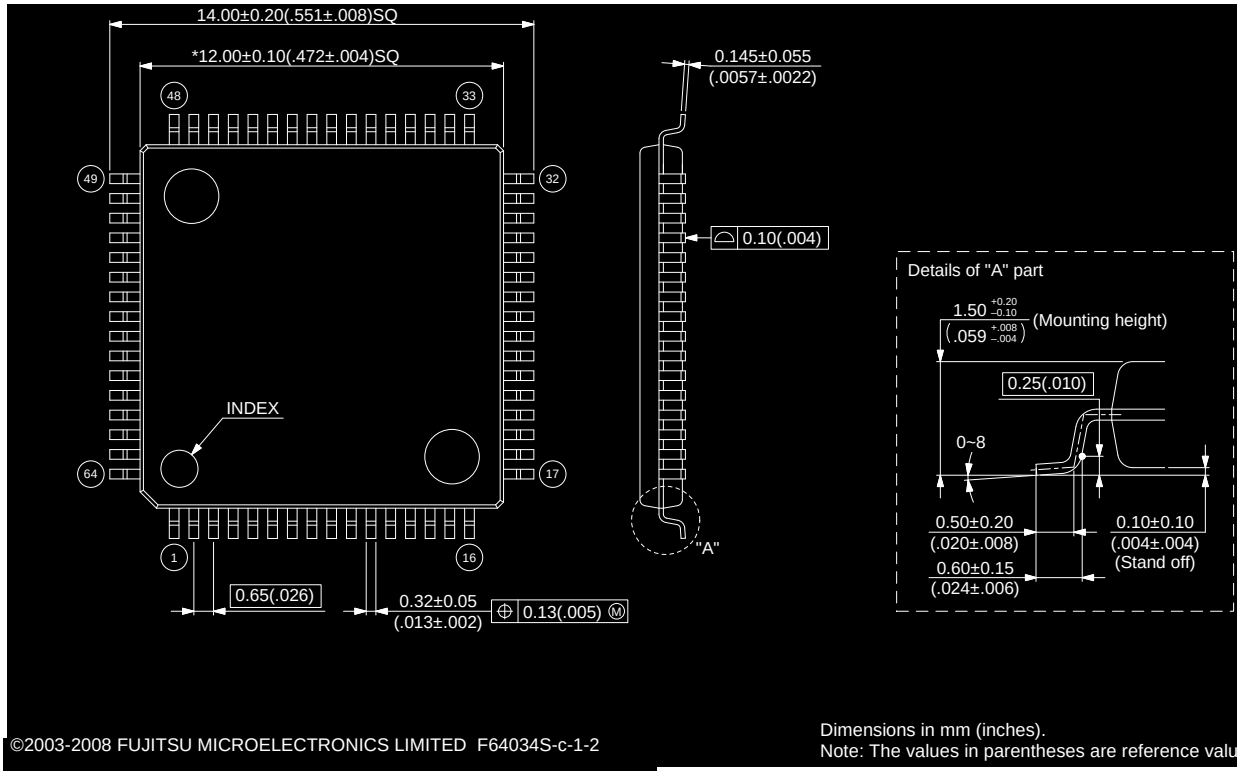
■ MASK OPTION

No.	Part number	MB95108AM	MB95F104AMS MB95F104ANS MB95F104AJS MB95F106AMS MB95F106ANS MB95F106AJS MB95F108AMS MB95F108ANS MB95F108AJS	MB95F104AMW MB95F104ANW MB95F104AJW MB95F106AMW MB95F106ANW MB95F106AJW MB95F108AMW MB95F108ANW MB95F108AJW	MB95FV100D-103
	Specifying procedure	Specify when ordering MASK	Setting disabled	Setting disabled	Setting disabled
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specify when ordering MASK	Specified by part number	Specified by part number	Changing by the switch on MCU board
3	Clock supervisor* • With clock supervisor • Without clock supervisor	Specify when ordering MASK	Specified by part number	Specified by part number	Changing by the switch on MCU board
4	Reset output* • With reset output • Without reset output	Specify when ordering MASK	Specified by part number	Specified by part number	MCU board switch set as following ; • With supervisor : Without reset output • Without supervisor : With reset output
5	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$

* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

(Continued)





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MEMO