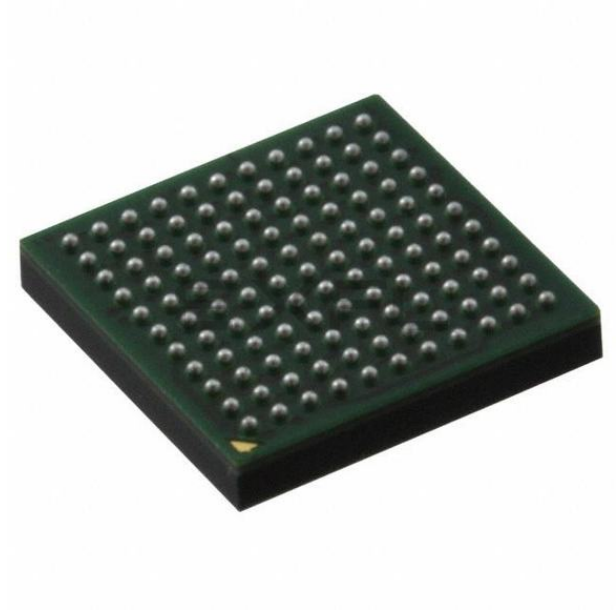

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x16b; D/A 2x6b, 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-XFBGA
Supplier Device Package	121-XFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk80fn256vdc15

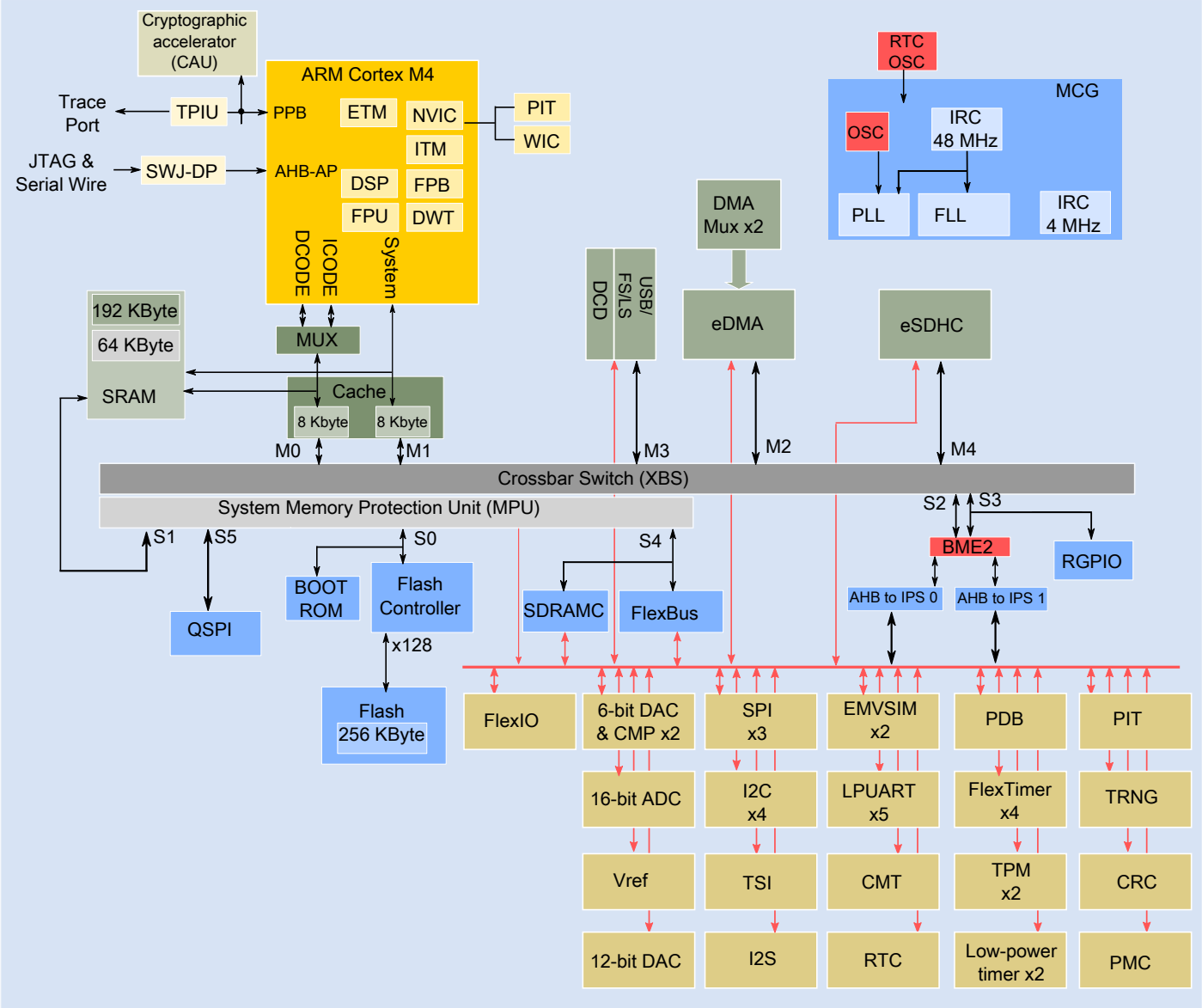

Figure 1. K80 Block Diagram

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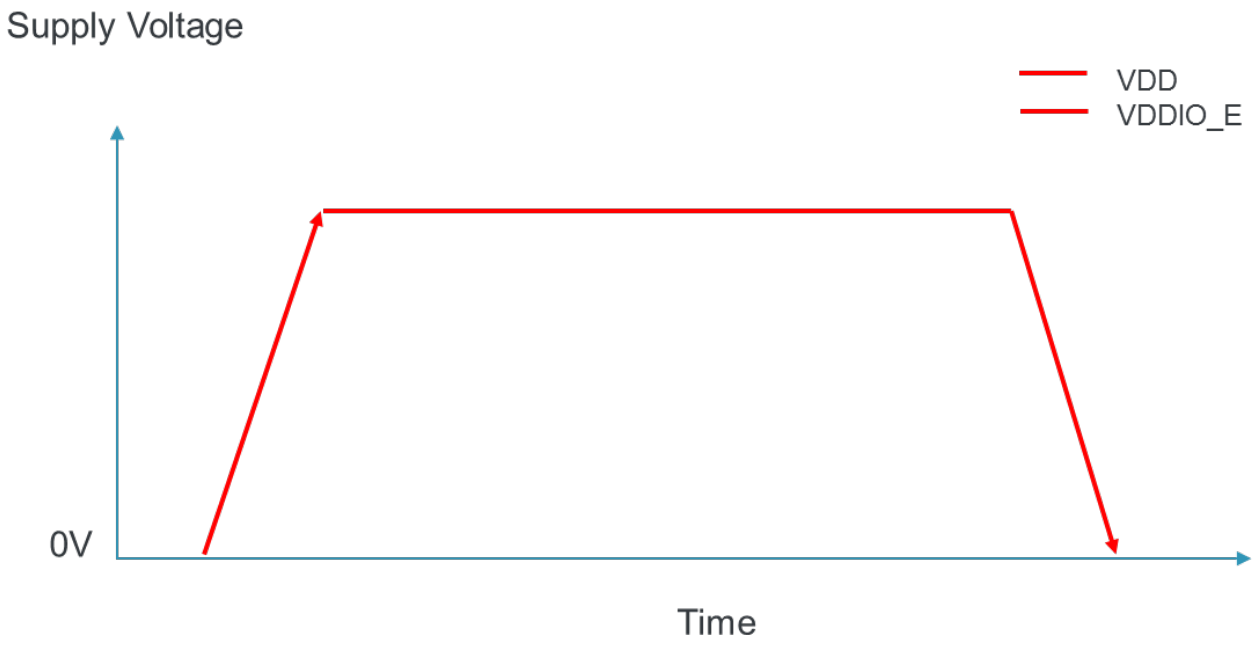


Figure 2. VDD = VDDIO_E

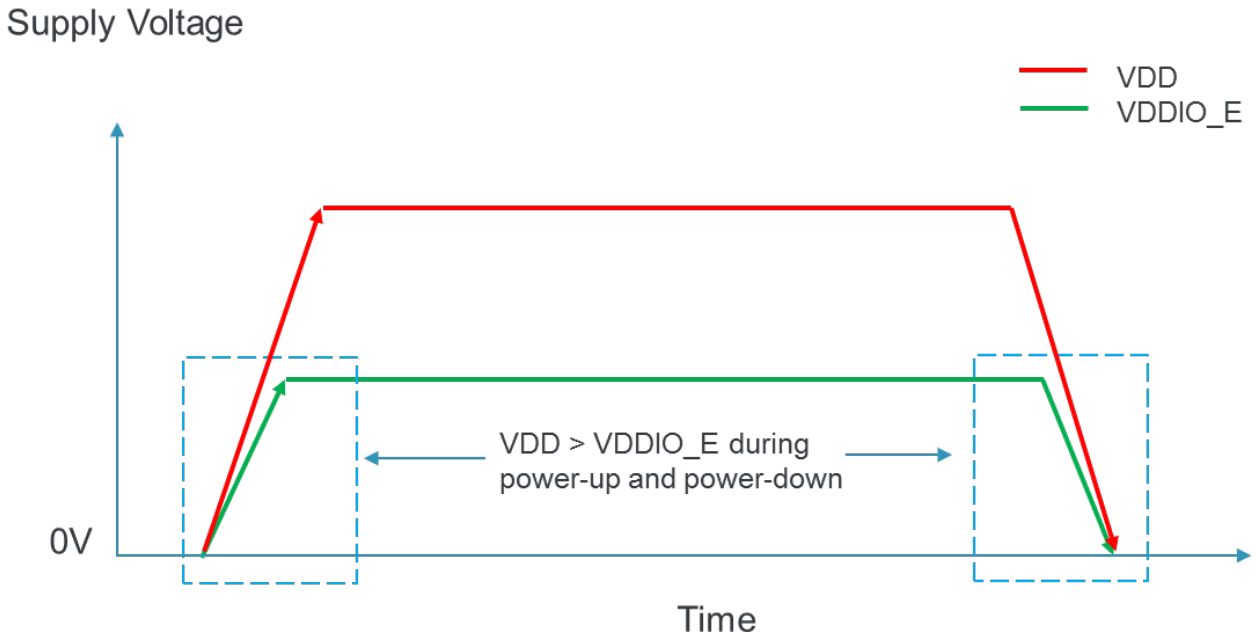


Figure 3. VDD > VDDIO_E

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 7. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					2
	• @ 25°C	—	28	31.55	mA	
	• @ 105°C	—	39.6	50.10		
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					3, 4
	• @ 25°C	—	54	57.55	mA	
	• @ 105°C	—	70	80.50		
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V					5
	• @ 25°C	—	25.1	28.65	mA	
	• @ 105°C	—	37.8	48.30		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					6
	• @ 25°C	—	38	40.70	mA	
	• @ 105°C	—	51.7	65.04		
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					7, 8
	• @ 25°C	—	48	50.70	mA	
	• @ 105°C	—	63.7	77.04		
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0V					
	• @ 25°C	—	34.5	37.2	mA	
	• @ 105°C	—	50.3	63.64		
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled					9
	• @ 25°C	—	14.2	19.87	mA	
	• @ 105°C	—	26.2	35.66		
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks enabled					9
		—	24.4	30.07	mA	

Table continues on the next page...

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V	— —	7 5	ns ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.
5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1,

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + \theta_{JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	100 LQFP	121 XFBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	52	71	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	39	36.8	°C/W	1

Table continues on the next page...

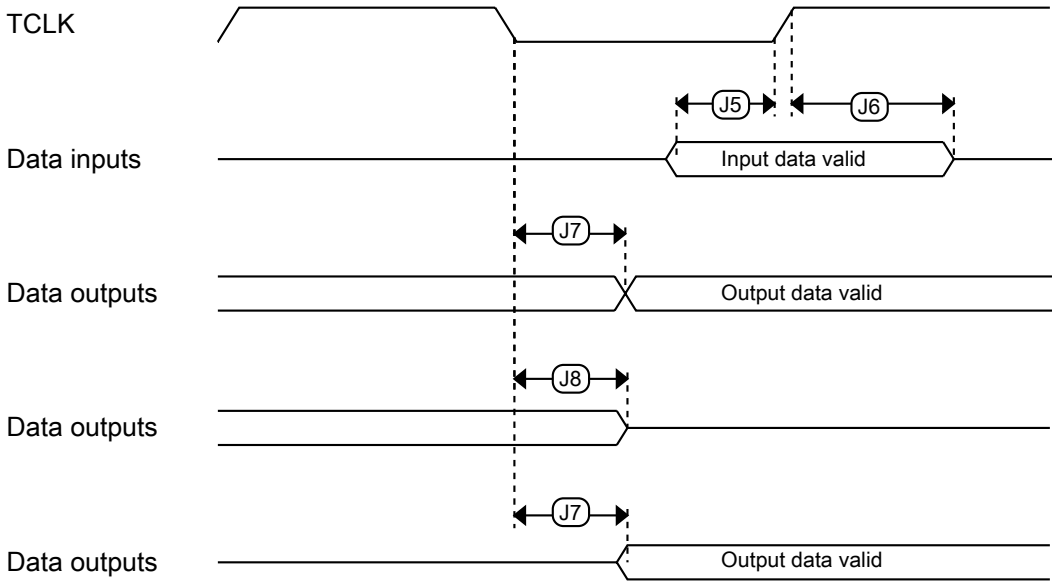


Figure 11. Boundary scan (JTAG) timing

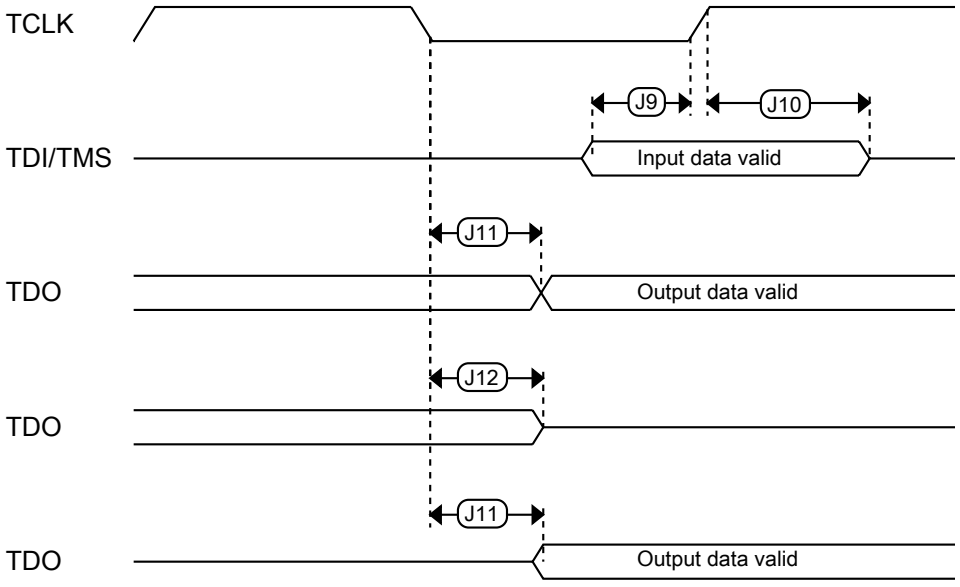


Figure 12. Test Access Port timing

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15pf (1.8V) and 35pf (3V) on output pins. Input slew: 1ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 22. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

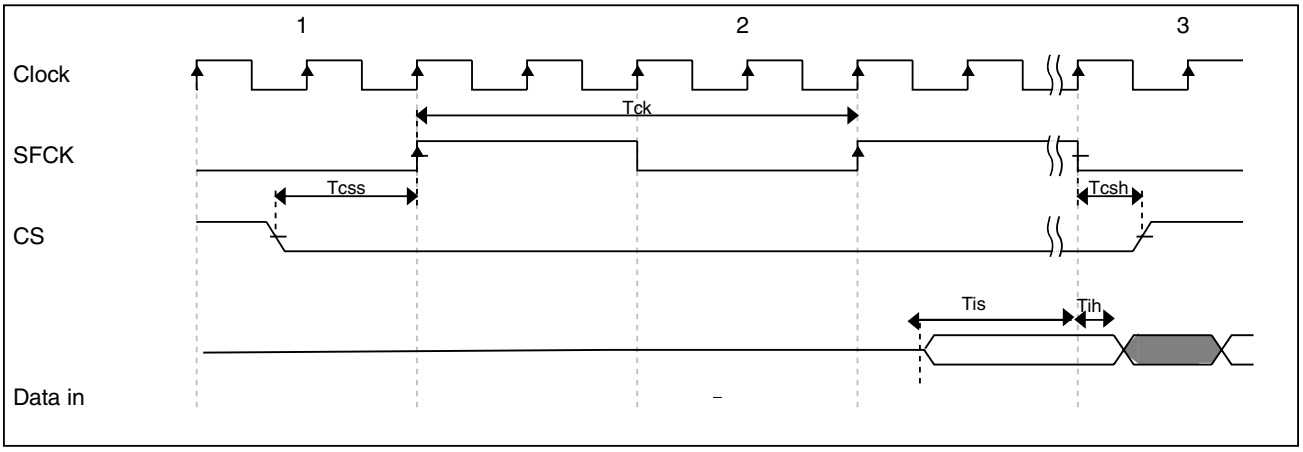


Figure 14. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15pf (1.8V) and 35pf (3V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 23. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4	-	ns
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

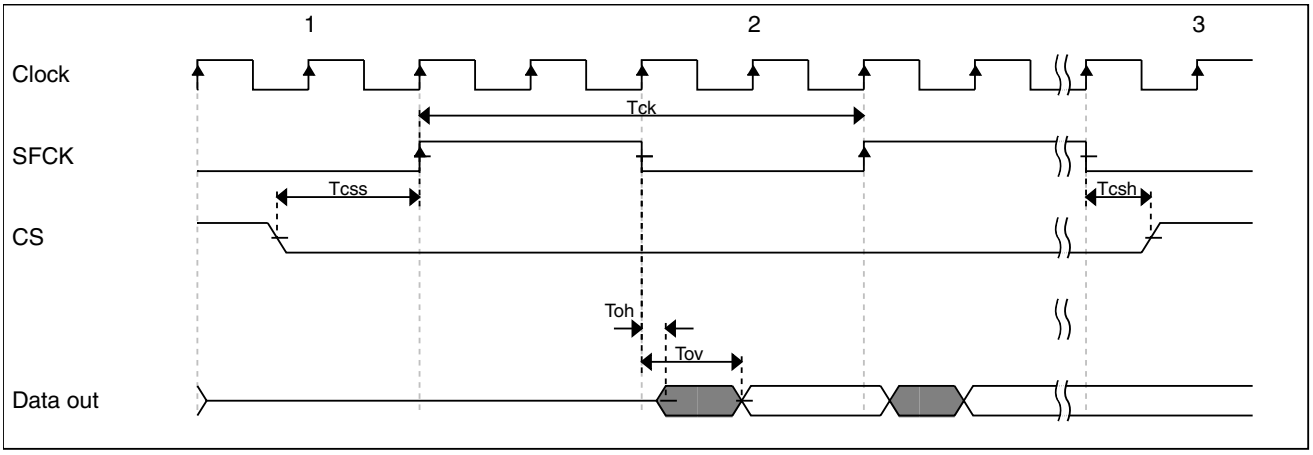


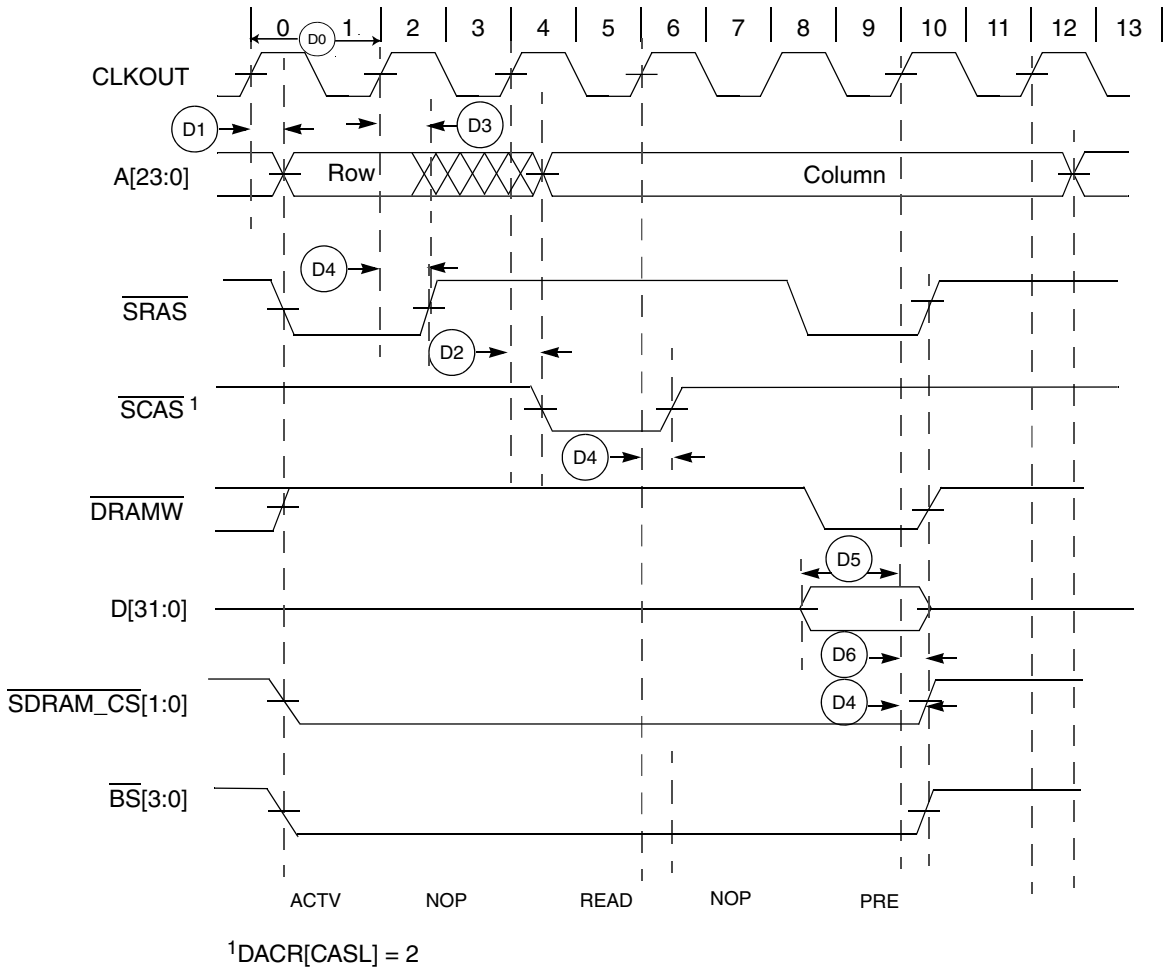
Figure 15. QuadSPI output timing (SDR mode) diagram

Table 24. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	2.8	ns
T_{oh}	Output Data Hold	-1.4	-	ns
T_{ck}	SCK clock period	-	100	MHz
T_{css}	Chip select output setup time	2	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.



[1]DACR[CASL] = 2

Figure 22. SDRAM read timing diagram

Table 35. SDRAM Timing (Full voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.2	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	12.0	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	12.0	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz

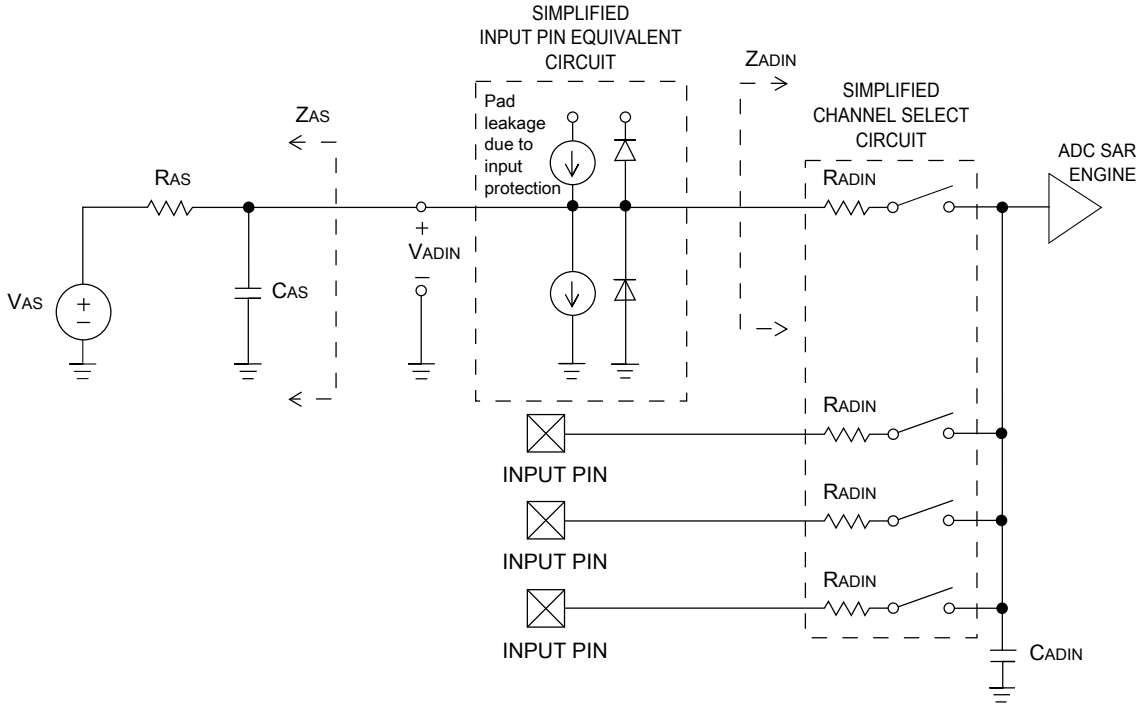


Figure 24. ADC input impedance equivalency diagram

3.5.1.2 ADC electrical characteristics

Table 38. ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

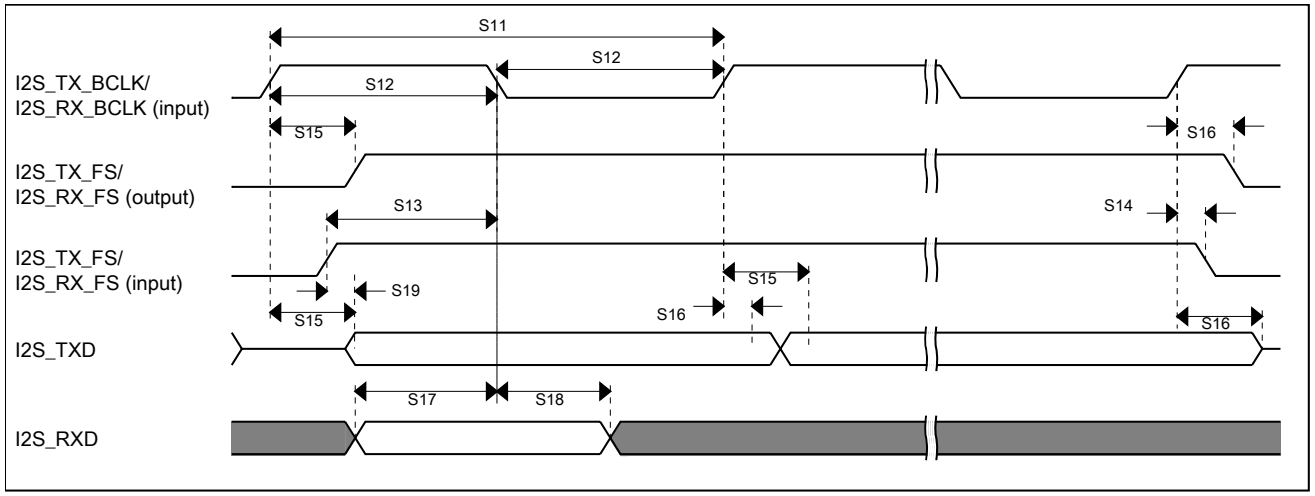


Figure 42. I2S/SAI timing — slave modes

3.7.10.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 62. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
121-pin XFBGA	98ASA00595D
144-pin LQFP	98ASS23177W[1]

1. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

5 Pinout

5.1 K80 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 144-pin LQFP and 121-WLCSP packages for this product are not yet available, however they are included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
x	—	H6	K9	NC	NC	NC								
—	—	—	G8	ADC0_SE16	ADC0_SE16	ADC0_SE16								
—	—	A11	—	NC	NC	NC								
—	—	J6	—	NC	NC	NC								
—	—	J4	—	NC	NC	NC								
1	1	B1	C10	PTE0	DISABLED		PTE0	SPI1_PCS1	LPUART1_TX	SDHC0_D1	QSPI0A_DATA3	I2C1_SDA	RTC_CLKOUT	
2	2	C2	D9	PTE1/LLWU_P0	DISABLED		PTE1/LLWU_P0	SPI1_SCK	LPUART1_RX	SDHC0_D0	QSPI0A_SCLK	I2C1_SCL	SPI1_SIN	
3	3	C1	D10	PTE2/LLWU_P1	DISABLED		PTE2/LLWU_P1	SPI1_SOUT	LPUART1_CTS_b	SDHC0_DCLK	QSPI0A_DATA0		SPI1_SCK	
4	4	D2	B11	PTE3	DISABLED		PTE3	SPI1_PCS2	LPUART1_RTS_b	SDHC0_CMD	QSPI0A_DATA2		SPI1_SOUT	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
32	—	K3	K11	ADC0_DM3	ADC0_DM3	ADC0_DM3								
33	22	F5	H8	VDDA	VDDA	VDDA								
34	23	G5	H9	VREFH	VREFH	VREFH								
35	24	G6	J9	VREFL	VREFL	VREFL								
36	25	F6	J8	VSSA	VSSA	VSSA								
37	26	L2	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
38	27	L1	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
39	28	L3	L11	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22								
40	29	K4	L10	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
42	30	K5	H7	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
43	31	L4	L9	XTAL32	XTAL32	XTAL32								
44	32	L5	L8	EXTAL32	EXTAL32	EXTAL32								
45	33	K6	K8	VBAT	VBAT	VBAT								
46	34	—	G7	VDD	VDD	VDD								
47	35	—	F6	VSS	VSS	VSS								
48	—	H5	L7	PTA20	DISABLED		PTA20	I2C0_SCL	LPUART4_TX	FTM_CLKIN1	FXIO0_D8	EWM_OUT_b	TPM_CLKIN1	
49	—	J5	K7	PTA21/ LLWU_P21	DISABLED		PTA21/ LLWU_P21	I2C0_SDA	LPUART4_RX		FXIO0_D9	EWM_IN		
50	36	L7	J7	PTA0	JTAG_TCLK/ SWD_CLK	TSI0_CH1	PTA0	LPUART0_CTS_b	FTM0_CH5		FXIO0_D10	EMVSIM0_CLK	JTAG_TCLK/ SWD_CLK	
51	37	H8	J6	PTA1	JTAG_TDI	TSI0_CH2	PTA1	LPUART0_RX	FTM0_CH6	I2C3_SDA	FXIO0_D11	EMVSIM0_IO	JTAG_TDI	
52	38	J7	K6	PTA2	JTAG_TDO/ TRACE_SWO	TSI0_CH3	PTA2	LPUART0_TX	FTM0_CH7	I2C3_SCL	FXIO0_D12	EMVSIM0_PD	JTAG_TDO/ TRACE_SWO	
53	39	H9	L6	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	LPUART0_RTS_b	FTM0_CH0		FXIO0_D13	EMVSIM0_RST	JTAG_TMS/ SWD_DIO	
54	40	J8	H6	PTA4/ LLWU_P3	NMI_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1		FXIO0_D14	EMVSIM0_VCCEN	NMI_b	

5.2 Recommended connection for unused analog and digital pins

Table 65 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 65. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DAC0_OUT, DAC1_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Analog	PTx/TSIOx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOUT33	Tie to input and ground through 10kΩ	Tie to input and ground through 10kΩ
USB	VREGIN	Tie to output and ground through 10kΩ	Tie to output and ground through 10kΩ
USB	USB0_VSS	Always connect to VSS	Always connect to VSS
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential

Table continues on the next page...

Table 65. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K80 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8/ LLWU_P24	NC	A
B	PTE0	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB4	B
C	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB5	C
D	PTE4/ LLWU_P2	PTE3	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTE6/ LLWU_P16	PTE5	PTD11/ LLWU_P25	PTD10	VDDIO_E	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	PTE9/ LLWU_P17	PTE8	PTE7	PTD12	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	PTE11	PTE10/ LLWU_P18	PTD13	PTD14	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	USB0_DM	USB0_DP	VSS	PTD15	PTA20	NC	PTA11/ LLWU_P23	PTA1	PTA3	PTA17	PTA29	H
J	VOUT33	VREGIN	ADC0_DP3	NC	PTA21/ LLWU_P21	NC	PTA2	PTA4/ LLWU_P3	PTA10/ LLWU_P22	PTA16	RESET_b	J
K	ADC0_DM0	ADC0_DP0	ADC0_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	RTC_ WAKEUP_B	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC0_DM1	ADC0_DP1	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	XTAL32	EXTAL32	VSS	PTA0	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 46. K80 121 XFBGA Pinout Diagram

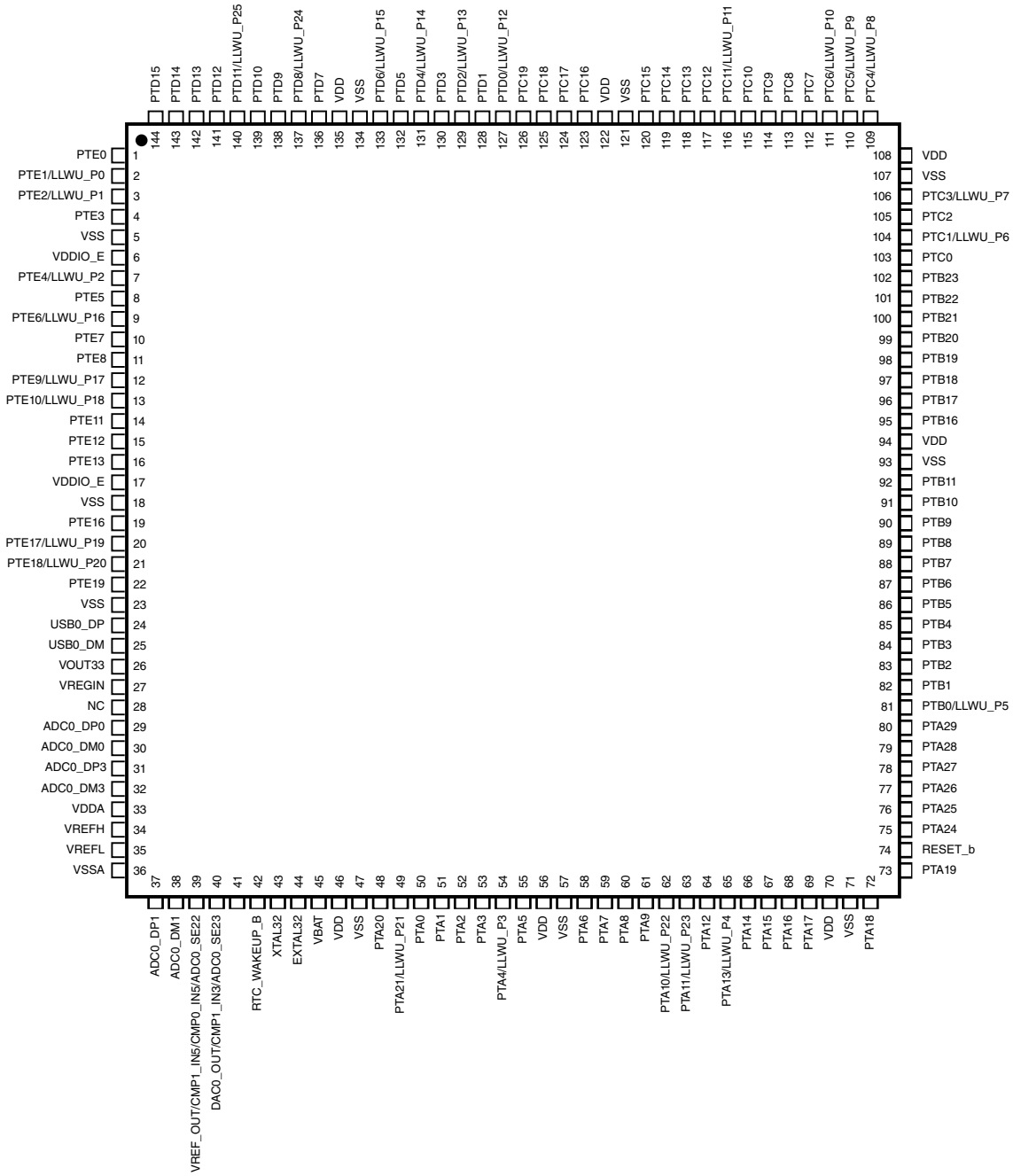


Figure 47. K80 144 LQFP Pinout Diagram

NOTE

The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: MK80.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K80
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB

Table continues on the next page...

Term	Definition
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

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