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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x16b; D/A 2x6b, 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk80fn256vll15

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [1]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{IO}	Input voltage (except PORTE, VBAT domain pins, and USB0)[2]	–0.3	V_{DD} + 0.3	V
V_{IO_E}	PORTE input voltage[3]	–0.3	V_{DDIO_E} + 0.3	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
VREGIN	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V

1. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}. However, it is required that the V_{DD} domain be powered up before V_{DDIO_E}. V_{DDIO_E} must never be higher than V_{DD} during power ramp up, or power down. V_{DD} and V_{DDIO_E} may ramp together if tied to the same power supply.
2. Includes ADC, CMP, and RESET_b inputs.
3. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when $V_{DD} \geq V_{DDIO\_E}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{DD} < V_{DDIO\_E}$.

1.4.1 Recommended POR Sequencing

Cases

- VDD = VDDIO_E
- VDD > VDDIO_E
- VDD < VDDIO_E

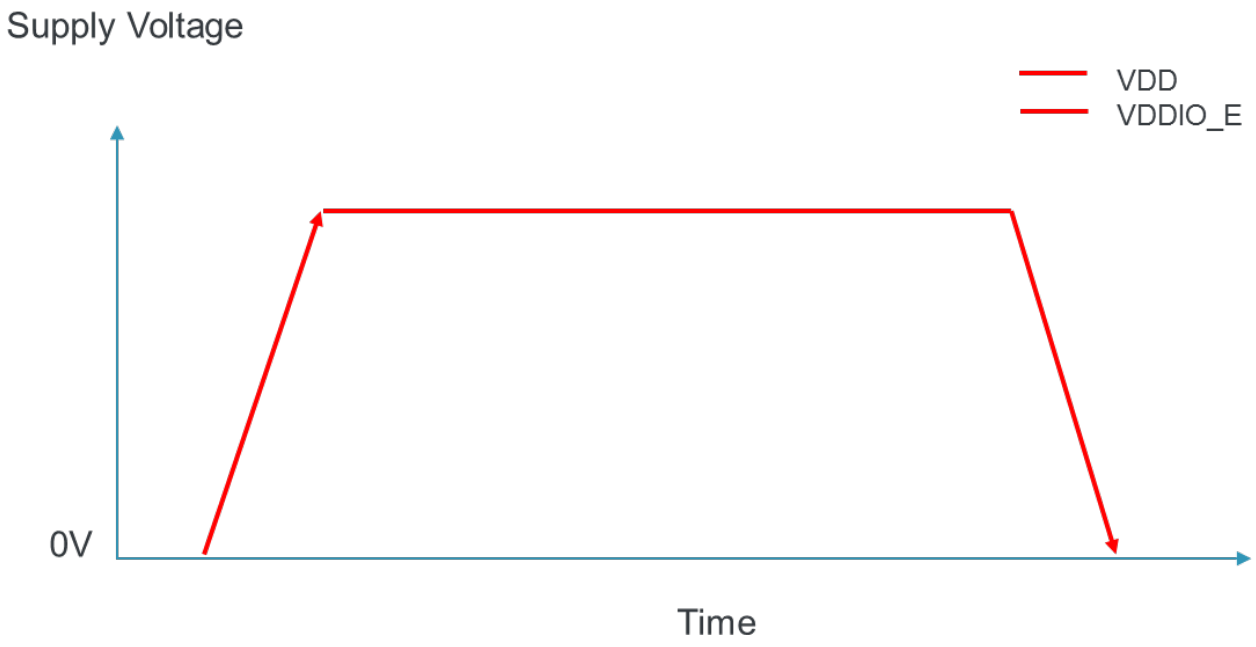

Figure 2. VDD = VDDIO_E

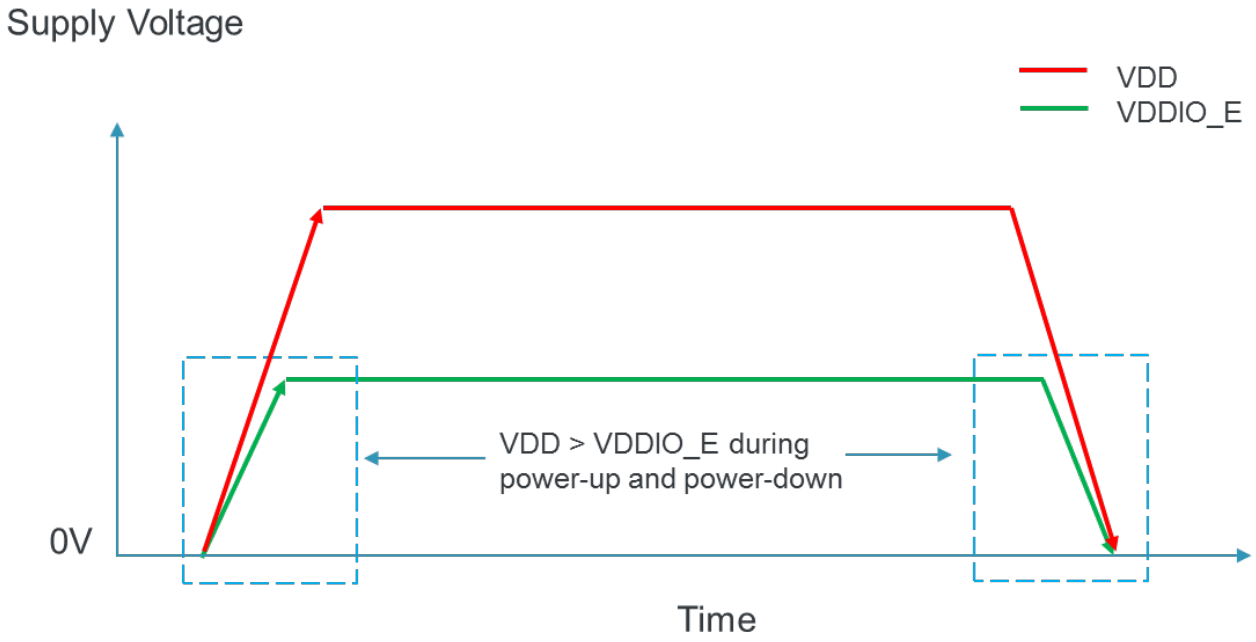

Figure 3. VDD > VDDIO_E

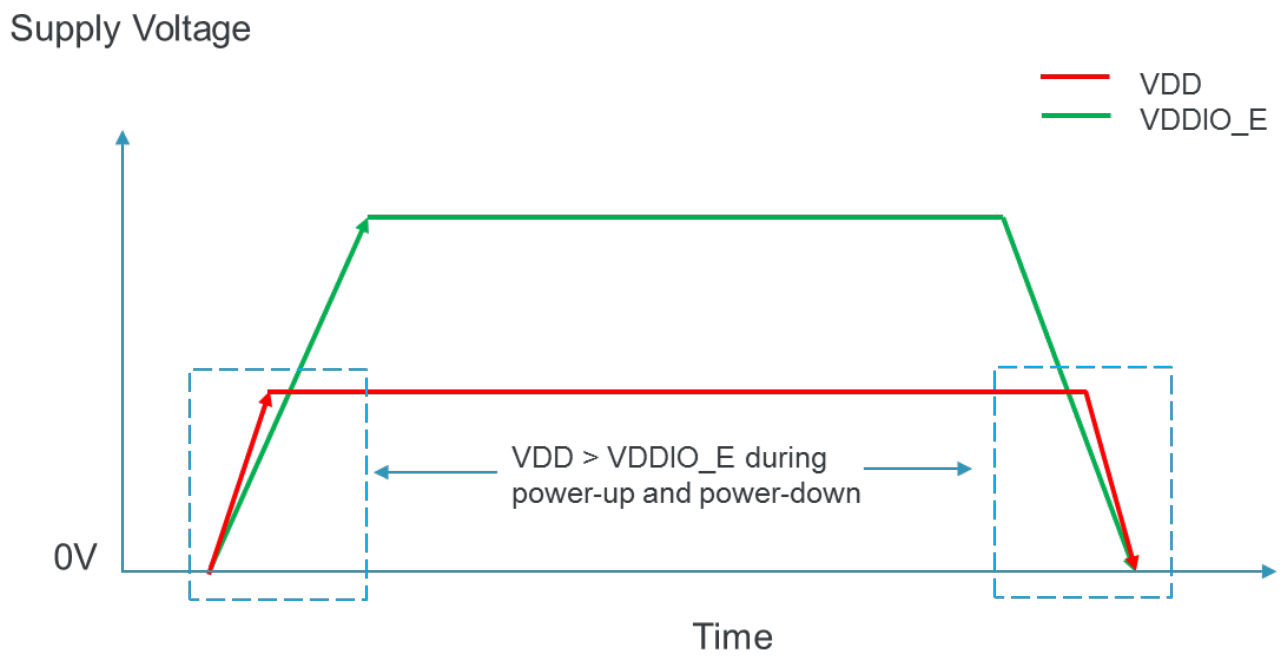

Figure 4. VDD < VDDIO_E

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

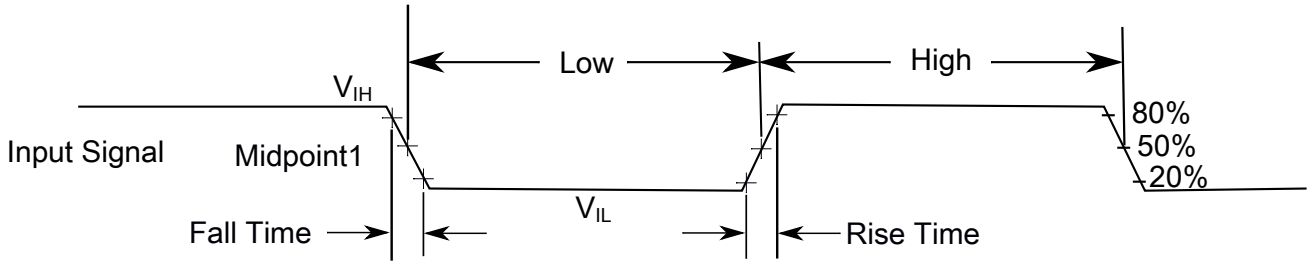

Figure 5. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, timers, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 34 16 10 8	 ns ns ns ns	4, 5
	Port rise and fall time (low drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 34 16 7 5	 ns ns ns ns	6, 7
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DDIO\_E} \le 2.7V$ • $2.7 \le V_{DDIO\_E} \le 3.6V$ • Slew disabled • $1.71 \le V_{DDIO\_E} \le 2.7V$ • $2.7 \le V_{DDIO\_E} \le 3.6V$	 — — — —	 34 16 7 5	 ns ns ns ns	5, 8
	Port rise and fall time (low drive strength) • Slew enabled	 — —	 34 16	 ns ns	7, 8

Table 16. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
	ext clk freq: between (2/5)fint and (3/5)f_{int} maybe reset (phase dependency) ext clk freq: below (2/5)f_{int} always reset						
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11 ext clk freq: above (16/5)f_{int} never reset ext clk freq: between (15/5)f_{int} and (16/5)f_{int} maybe reset (phase dependency) ext clk freq: below (15/5)f_{int} always reset		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco_ut}	DCO output frequency range — untrimmed	Low range (DRS=00, DMX32=0) 640 × f_{ints_ut}	16.0	23.04	26.66	MHz	2
		Mid range (DRS=01, DMX32=0) 1280 × f_{ints_ut}	32.0	46.08	53.32		
		Mid-high range (DRS=10, DMX32=0) 1920 × f_{ints_ut}	48.0	69.12	79.99		
		High range (DRS=11, DMX32=0) 2560 × f_{ints_ut}	64.0	92.16	106.65		
		Low range (DRS=00, DMX32=1) 732 × f_{ints_ut}	18.3	26.35	30.50		
		Mid range (DRS=01, DMX32=1) 1464 × f_{ints_ut}	36.6	52.70	60.99		
		Mid-high range (DRS=10, DMX32=1) 2197 × f_{ints_ut}	54.93	79.09	91.53		
		High range (DRS=11, DMX32=1) 2929 × f_{ints_ut}	73.23	105.44	122.02		
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01)	40	41.94	50	MHz	

Table continues on the next page...

Table 26. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	4.5	ns
T_{oh}	Output Data Hold	1.5	-	ns
T_{ck}	SCK clock period	-	75 (with learning)	MHz
		-	45 (without learning)	
T_{css}	Chip select output setup time	2	-	Clk(sck)
T_{csh}	Chip select output hold time	-1	-	Clk(sck)

Hyperflash mode

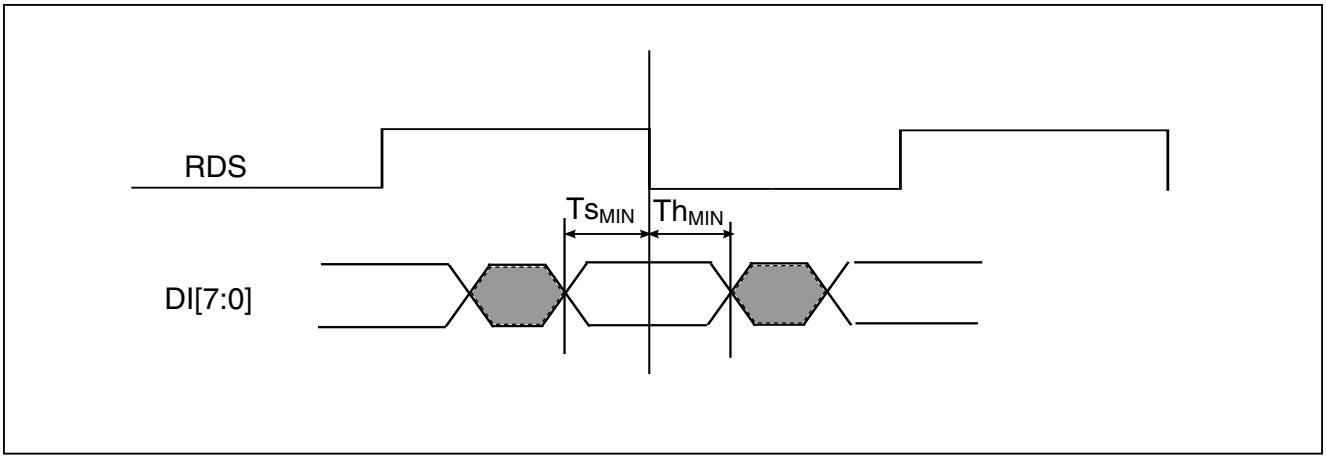

Figure 18. QuadSPI input timing (Hyperflash mode) diagram

Table 27. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Ts_{MIN}	Setup time for incoming data	2	-	ns
Th_{MIN}	Hold time requirement for incoming data	2	-	ns

Table 32. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ °C.

3.3.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 33. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	11.8	ns	
FB3	Address, data, and control output hold	1.0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	6	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.0	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE}}$/BWE*n*, $\overline{\text{FB\_CS}}$*n*, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 34. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	12.6	ns	

Table continues on the next page...

3. D7 and D8 are for write cycles only.

Table 36. SDRAM Timing (Limited voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.1	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	7.3	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	11.1	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz
3. D7 and D8 are for write cycles only.

Following figure shows an SDRAM write cycle.

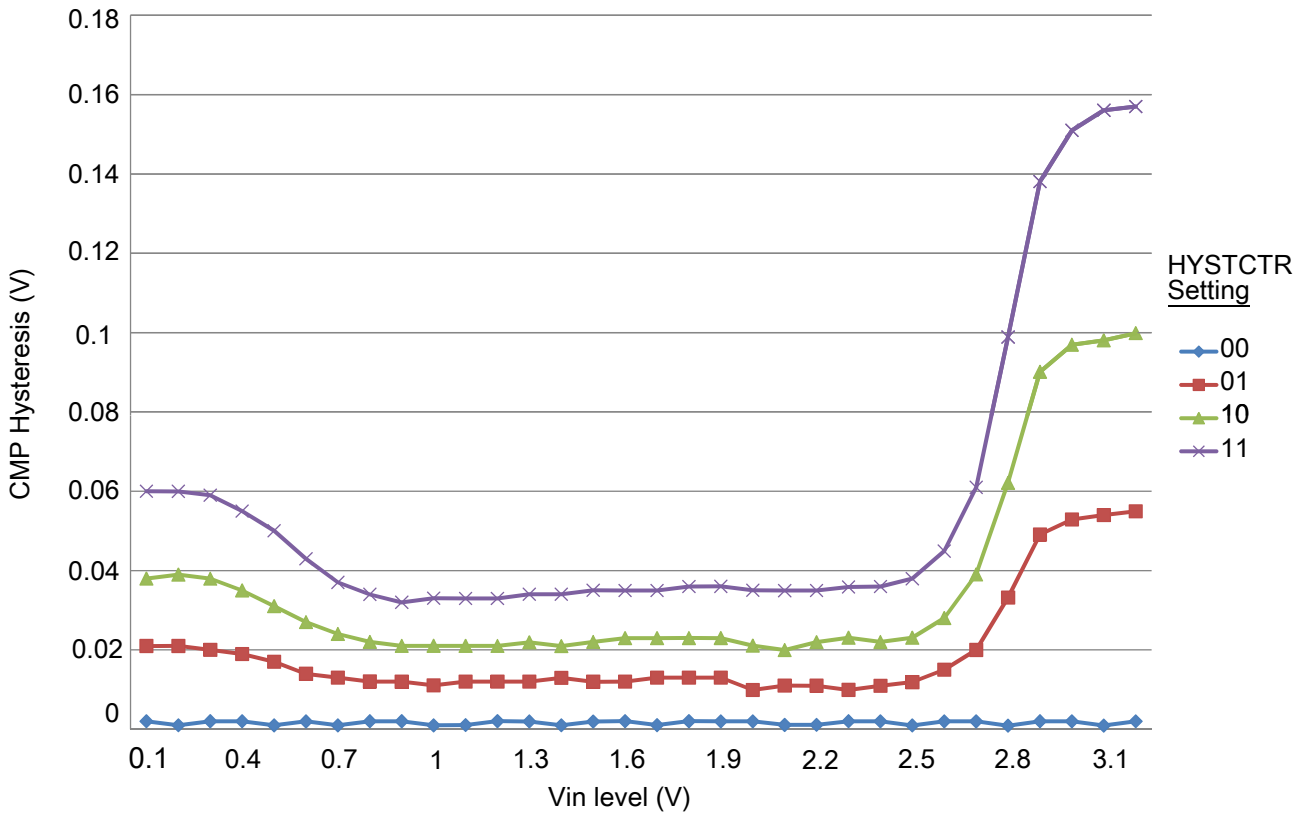

Figure 27. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.5.3 12-bit DAC electrical characteristics

3.5.3.1 12-bit DAC operating requirements

Table 40. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

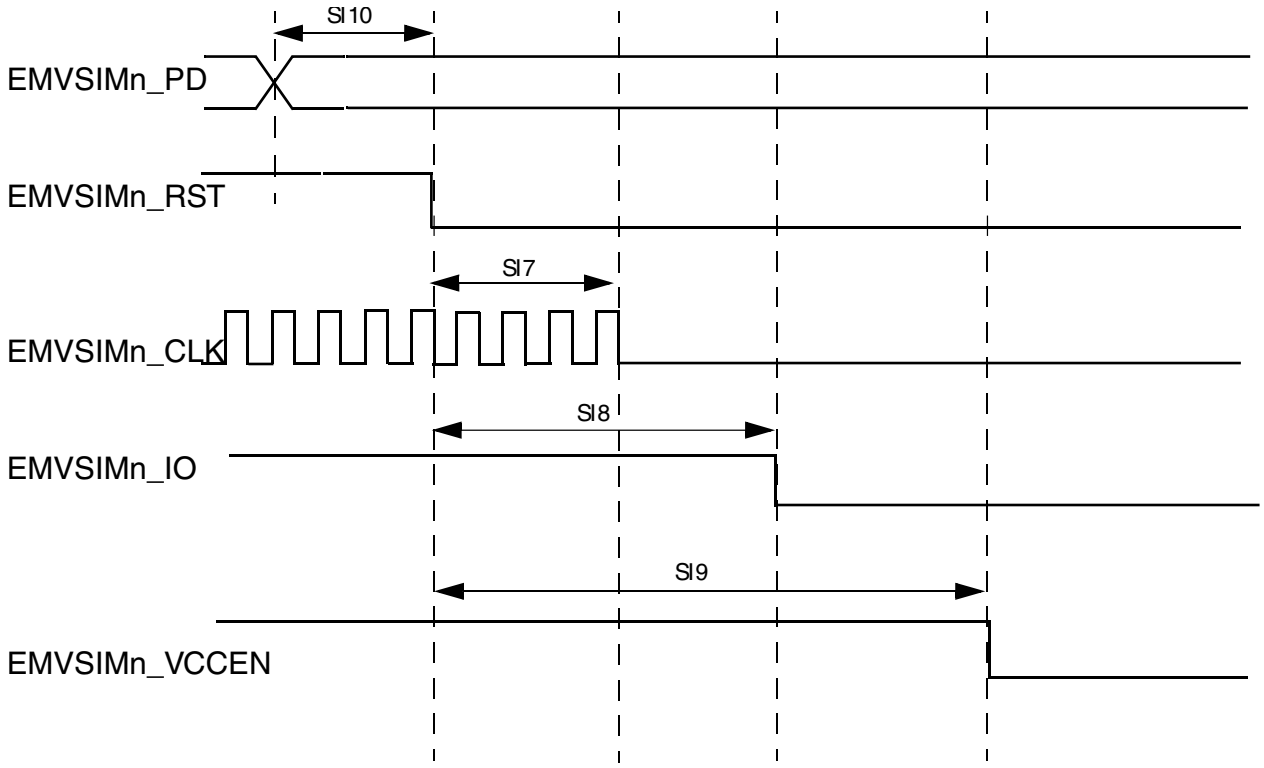

Figure 33. Smart Card Interface Power Down AC Timing

Table 49. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk[1]	1.1 × 1/Frtcclk	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/ Frtcclk	2.2 × 1/Frtcclk	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/ Frtcclk	3.3 × 1/Frtcclk	µs
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/ Frtcclk	1.1 × 1/Frtcclk	µs

1. Frtcclk is ERCLK32K, and this clock must be enabled during the power down sequence.

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

3.7.2 USB VREG electrical specifications

Table 50. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.7.3 USB DCD electrical specifications

Table 51. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}, V_{DM_SRC}	USB_DP and USB_DM source voltages (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}, I_{DP_SINK}	USB_DM and USB_DP sink currents	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.7.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 54. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	16	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

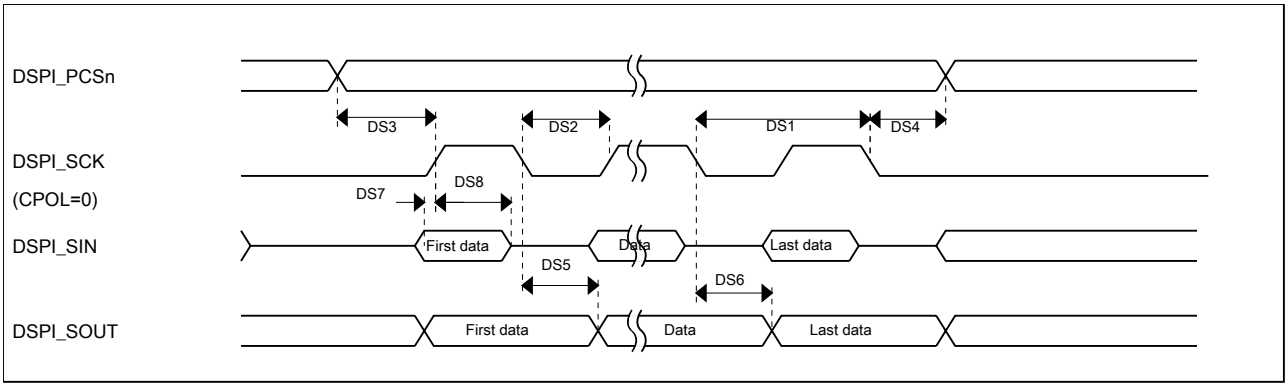

Figure 36. DSPI classic SPI timing — master mode

Table 55. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

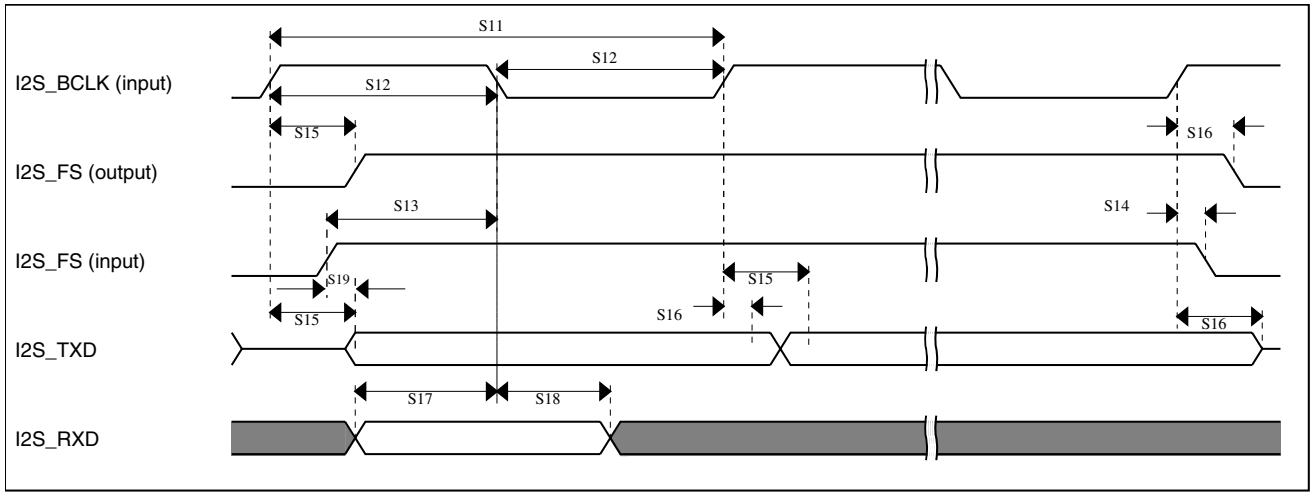

Figure 40. I²S timing — slave modes

3.7.10.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 60. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

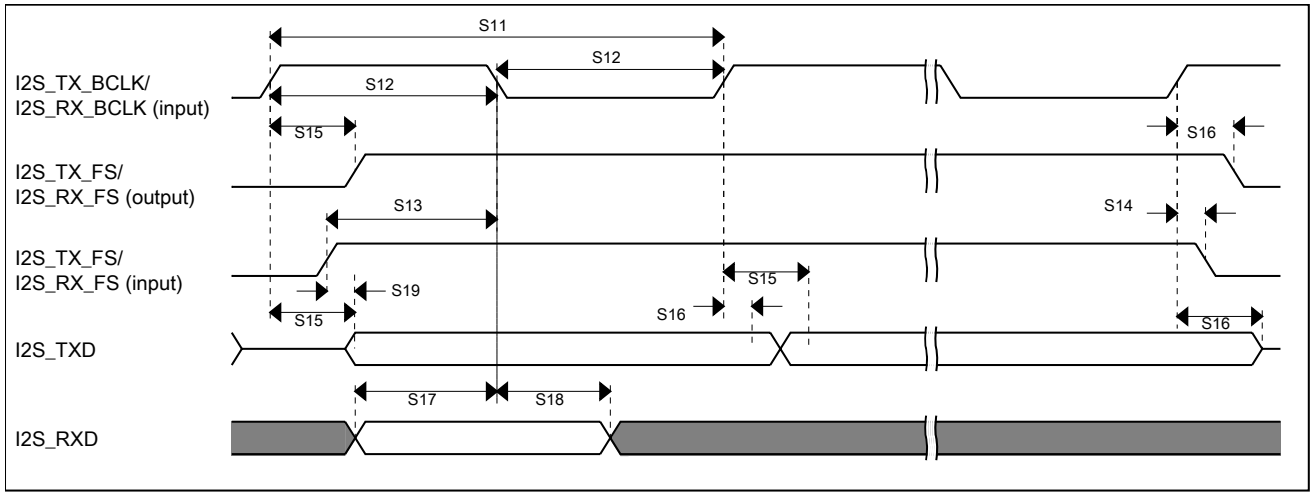

Figure 44. I2S/SAI timing — slave modes

3.8 Human-machine interfaces (HMI)

3.8.1 TSI electrical specifications

Table 64. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
55	41	K7	H5	PTA5	DISABLED		PTA5	USB0_CLKIN	FTM0_CH2		FXIO0_D15	I2S0_TX_BCLK	JTAG_TRST_b	
56	—	L10	G6	VDD	VDD	VDD								
57	—	K10	F5	VSS	VSS	VSS								
58	—	—	—	PTA6	DISABLED		PTA6	I2C2_SCL	FTM0_CH3	EMVSIM1_CLK	CLKOUT		TRACE_CLKOUT	
59	—	—	—	PTA7	ADC0_SE10	ADC0_SE10	PTA7	I2C2_SDA	FTM0_CH4	EMVSIM1_IO			TRACE_D3	
60	—	—	—	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0	EMVSIM1_PD		FTM1_QD_PHA/TPM1_CH0	TRACE_D2	
61	—	—	—	PTA9	DISABLED		PTA9		FTM1_CH1	EMVSIM1_RST		FTM1_QD_PHB/TPM1_CH1	TRACE_D1	
62	—	J9	L5	PTA10/LLWU_P22	DISABLED		PTA10/LLWU_P22	I2C2_SDA	FTM2_CH0	EMVSIM1_VCCEN	FXIO0_D16	FTM2_QD_PHA/TPM2_CH0	TRACE_D0	
63	—	H7	L4	PTA11/LLWU_P23	DISABLED		PTA11/LLWU_P23	I2C2_SCL	FTM2_CH1		FXIO0_D17	FTM2_QD_PHB/TPM2_CH1		
64	42	K8	K5	PTA12	DISABLED		PTA12		FTM1_CH0	TRACE_CLKOUT	FXIO0_D18	I2S0_TXD0	FTM1_QD_PHA/TPM1_CH0	
65	43	L8	J5	PTA13/LLWU_P4	DISABLED		PTA13/LLWU_P4		FTM1_CH1	TRACE_D3	FXIO0_D19	I2S0_TX_FS	FTM1_QD_PHB/TPM1_CH1	
66	44	K9	L3	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_TX	TRACE_D2	FXIO0_D20	I2S0_RX_BCLK	I2S0_TXD1	
67	45	L9	K4	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_RX	TRACE_D1	FXIO0_D21	I2S0_RXD0		
68	46	J10	J4	PTA16	DISABLED		PTA16	SPI0_SOUT	LPUART0_CTS_b	TRACE_D0	FXIO0_D22	I2S0_RX_FS	I2S0_RXD1	
69	47	H10	K3	PTA17	DISABLED		PTA17	SPI0_SIN	LPUART0_RTS_b		FXIO0_D23	I2S0_MCLK		
70	48	E6	L2	VDD	VDD	VDD								
71	49	G7	K2	VSS	VSS	VSS								
72	50	L11	L1	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0			TPM_CLKIN0	
73	51	K11	K1	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1/LPTMR1_ALT1	TPM_CLKIN1	
74	52	J11	J1	RESET_b	RESET_b	RESET_b								
75	—	—	—	PTA24	DISABLED		PTA24	EMVSIM0_CLK				FB_A29		

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
76	—	—	—	PTA25	DISABLED		PTA25	EMVSIM0_IO				FB_A28		
77	—	—	—	PTA26	DISABLED		PTA26	EMVSIM0_PD				FB_A27		
78	—	—	—	PTA27	DISABLED		PTA27	EMVSIM0_RST				FB_A26		
79	—	—	—	PTA28	DISABLED		PTA28	EMVSIM0_VCCEN				FB_A25		
80	—	H11	J2	PTA29	DISABLED		PTA29					FB_A24		
81	53	G11	J3	PTB0/LLWU_P5	ADC0_SE8/TSI0_CH0	ADC0_SE8/TSI0_CH0	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0		SDRAM_CAS_b	FTM1_QD_PHA/TPM1_CH0	FXIO0_D0	
82	54	G10	H2	PTB1	ADC0_SE9/TSI0_CH6	ADC0_SE9/TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1		SDRAM_RAS_b	FTM1_QD_PHB/TPM1_CH1	FXIO0_D1	
83	55	G9	H1	PTB2	ADC0_SE12/TSI0_CH7	ADC0_SE12/TSI0_CH7	PTB2	I2C0_SCL	LPUART0_RTS_b		SDRAM_WE	FTM0_FLT3	FXIO0_D2	
84	56	G8	H3	PTB3	ADC0_SE13/TSI0_CH8	ADC0_SE13/TSI0_CH8	PTB3	I2C0_SDA	LPUART0_CTS_b		SDRAM_CS0_b	FTM0_FLT0	FXIO0_D3	
85	—	B11	H4	PTB4	DISABLED		PTB4	EMVSIM1_IO			SDRAM_CS1_b	FTM1_FLT0		
86	—	C11	G1	PTB5	DISABLED		PTB5	EMVSIM1_CLK				FTM2_FLT0		
87	—	F11	G2	PTB6	DISABLED		PTB6	EMVSIM1_VCCEN			FB_AD23/SDRAM_D23			
88	—	E11	G3	PTB7	DISABLED		PTB7	EMVSIM1_PD			FB_AD22/SDRAM_D22			
89	—	D11	G4	PTB8	DISABLED		PTB8	EMVSIM1_RST	LPUART3_RTS_b		FB_AD21/SDRAM_D21			
90	57	E10	G5	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART3_CTS_b		FB_AD20/SDRAM_D20			
91	58	D10	F1	PTB10	DISABLED		PTB10	SPI1_PCS0	LPUART3_RX	I2C2_SCL	FB_AD19/SDRAM_D19	FTM0_FLT1	FXIO0_D4	
92	59	C10	F2	PTB11	DISABLED		PTB11	SPI1_SCK	LPUART3_TX	I2C2_SDA	FB_AD18/SDRAM_D18	FTM0_FLT2	FXIO0_D5	
93	60	L6	F5	VSS	VSS	VSS								
94	61	E7	G6	VDD	VDD	VDD								

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
											SDRAM_DQM1			
126	—	A4	B6	PTC19	DISABLED		PTC19		LPUART3_CTS_b		FB_CS3_b/FB_BE7_0_BLS31_24_b/SDRAM_DQM0	FB_TA_b		
127	91	D4	C6	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0	LPUART2_RTS_b	FTM3_CH0	FB_ALE/FB_CS1_b/FB_TS_b		FXIO0_D22	
128	92	D3	D6	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	LPUART2_CTS_b	FTM3_CH1	FB_CS0_b		FXIO0_D23	
129	93	C3	D7	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT	LPUART2_RX	FTM3_CH2	FB_AD4/SDRAM_A12		I2C0_SCL	
130	94	B3	A7	PTD3	DISABLED		PTD3	SPI0_SIN	LPUART2_TX	FTM3_CH3	FB_AD3/SDRAM_A11		I2C0_SDA	
131	95	A3	B7	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	LPUART0_RTS_b	FTM0_CH4	FB_AD2/SDRAM_A10	EWM_IN	SPI1_PCS0	
132	96	A2	C7	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	LPUART0_CTS_b	FTM0_CH5	FB_AD1/SDRAM_A9	EWM_OUT_b	SPI1_SCK	
133	97	B2	A8	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	LPUART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
134	98	—	F6	VSS	VSS	VSS								
135	99	—	E7	VDD	VDD	VDD								
136	100	A1	B8	PTD7	DISABLED		PTD7	CMT_IRO	LPUART0_TX	FTM0_CH7	SDRAM_CKE	FTM0_FLT1	SPI1_SIN	
137	—	A10	A9	PTD8/LLWU_P24	DISABLED		PTD8/LLWU_P24	I2C0_SCL				FB_A16	FXIO0_D24	
138	—	A9	C8	PTD9	DISABLED		PTD9	I2C0_SDA				FB_A17	FXIO0_D25	
139	—	E4	B9	PTD10	DISABLED		PTD10					FB_A18	FXIO0_D26	
140	—	E3	A10	PTD11/LLWU_P25	DISABLED		PTD11/LLWU_P25	SPI2_PCS0				FB_A19	FXIO0_D27	
141	—	F4	D8	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0			FB_A20	FXIO0_D28	
142	—	G3	C9	PTD13	DISABLED		PTD13	SPI2_SOUT				FB_A21	FXIO0_D29	
143	—	G4	B10	PTD14	DISABLED		PTD14	SPI2_SIN				FB_A22	FXIO0_D30	
144	—	H4	A11	PTD15	DISABLED		PTD15	SPI2_PCS1				FB_A23	FXIO0_D31	

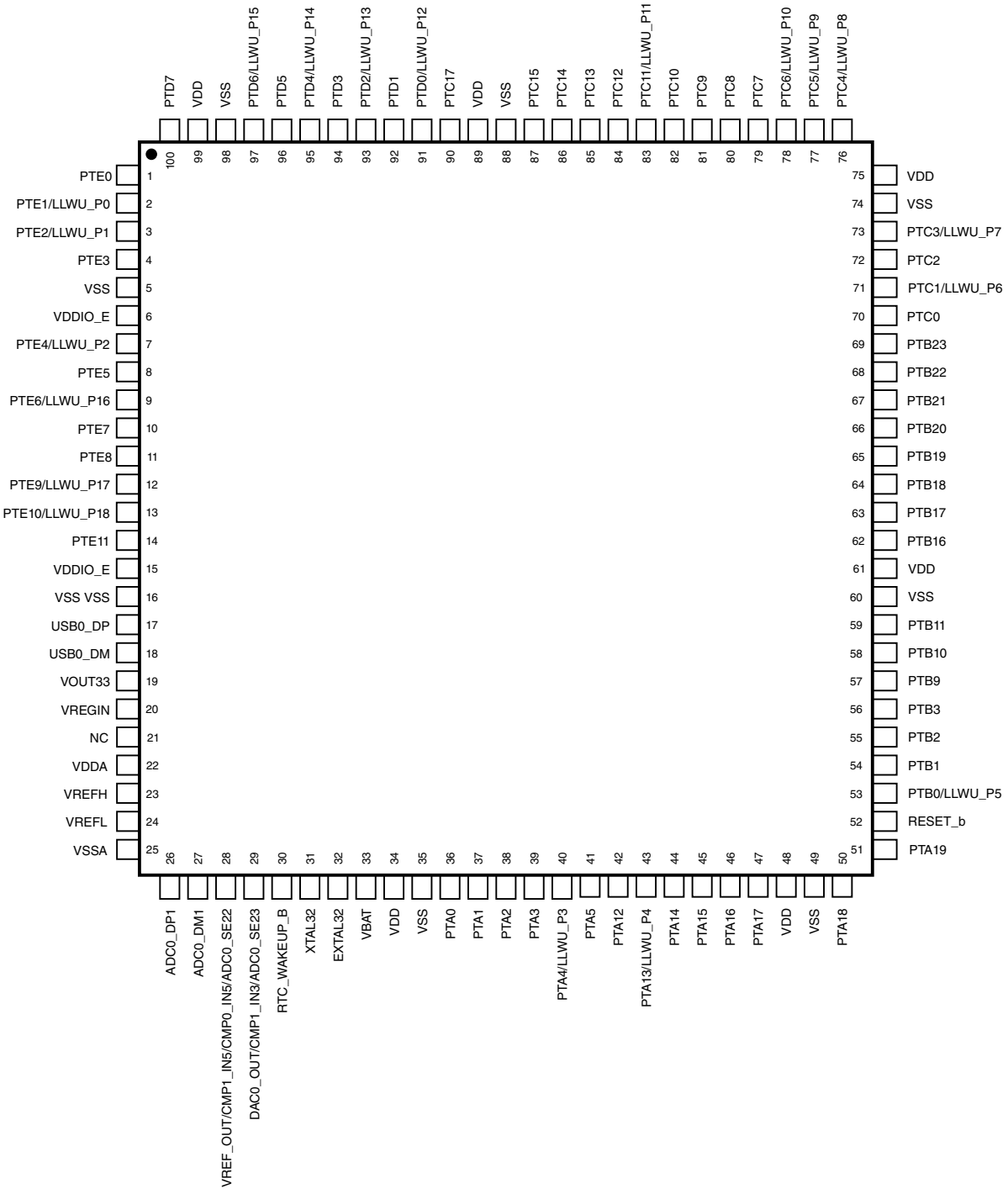

Figure 45. K80 100 LQFP Pinout Diagram

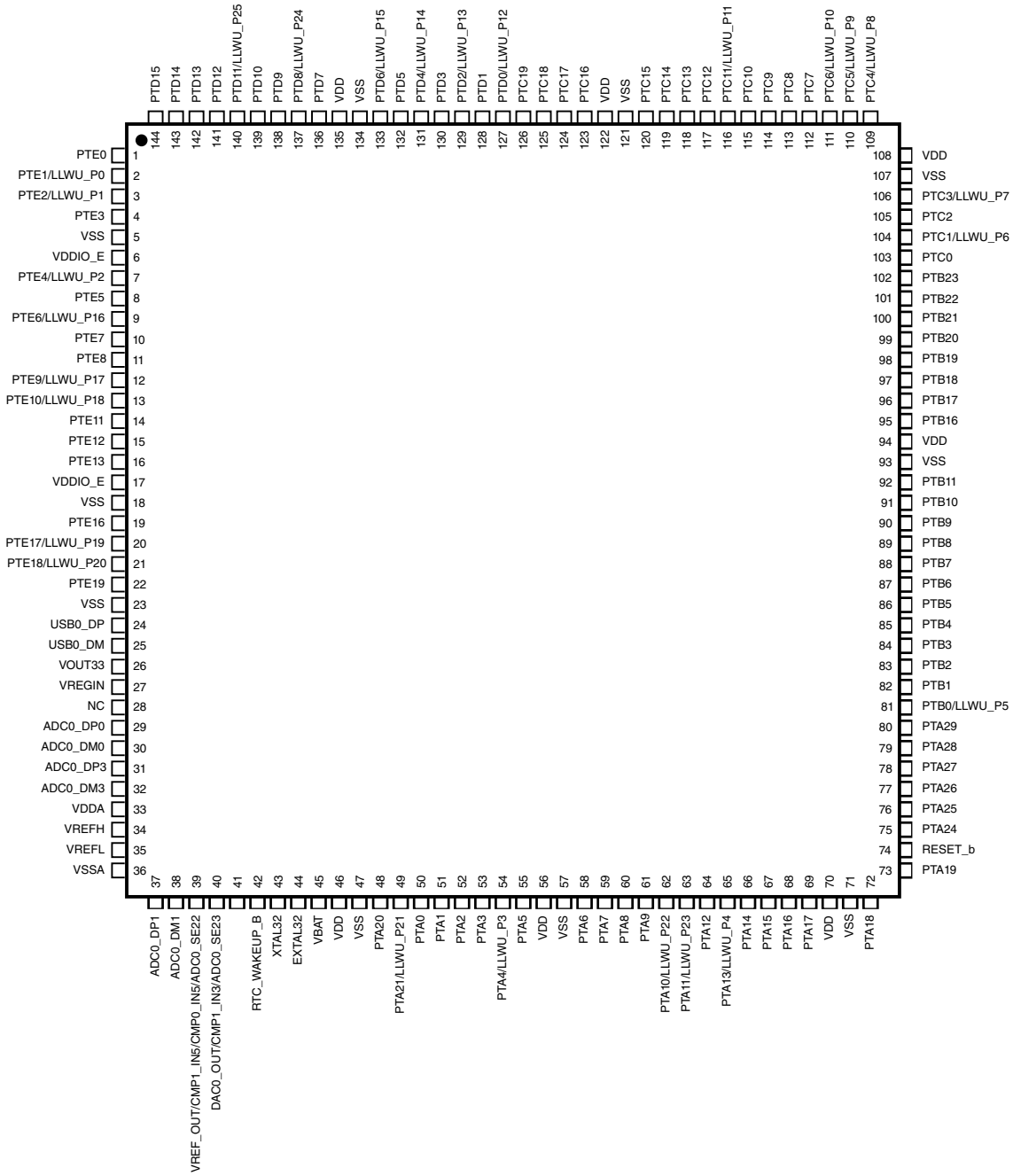

Figure 47. K80 144 LQFP Pinout Diagram

NOTE

The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

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