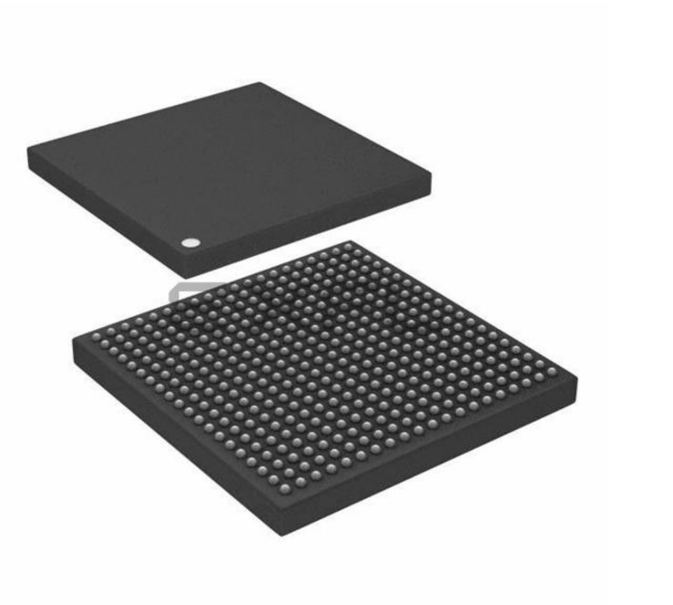

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | SC1400 Core |
| Interface | Host Interface, I²C, UART |
| Clock Rate | 200MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 208kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-LFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7113vm800 |

# Table of Contents



## List of Figures

**Table 1. MSC7113 Signals by Ball Designator (continued)**

| Number | Signal Names | | | | | |
|---|---|---|---|---|---|---|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| B15 (1L44X) | NC | | | | | |
| B15 (1M88B) | BM2 | GPID7 | | GPOD7 | reserved | |
| B16 | NC | | | | | |
| B17 | NC | | | | | |
| B18 | NC | | | | | |
| B19 | NC | | | | | |
| B20 | NC | | | | | |
| C1 | D24 | | | | | |
| C2 | D30 | | | | | |
| C3 | D25 | | | | | |
| C4 | $\overline{CS1}$ | | | | | |
| C5 | DQM3 | | | | | |
| C6 | DQM0 | | | | | |
| C7 | DQS1 | | | | | |
| C8 | $\overline{RAS}$ | | | | | |
| C9 | $\overline{CAS}$ | | | | | |
| C10 | GPIC5 | | | GPOC5 | HD13 | |
| C11 | GPIC1 | | | GPOC1 | HD9 | |
| C12 | reserved | | | | HD3 | |
| C13 | NC | | | | | |
| C14 | NC | | | | | |
| C15 | NC | | | | | |
| C16 | NC | | | | | |
| C17 | NC | | | | | |
| C18 | NC | | | | | |
| C19 | NC | | | | | |
| C20 | NC | | | | | |
| D1 | $V_{DDM}$ | | | | | |
| D2 | D28 | | | | | |
| D3 | D27 | | | | | |
| D4 | GND | | | | | |
| D5 | $V_{DDM}$ | | | | | |
| D6 | $V_{DDM}$ | | | | | |
| D7 | $V_{DDM}$ | | | | | |
| D8 | $V_{DDM}$ | | | | | |
| D9 | $V_{DDM}$ | | | | | |
| D10 | $V_{DDM}$ | | | | | |
| D11 | $V_{DDIO}$ | | | | | |

Table 1. MSC7113 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|---|---|---|---|---|---|---|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| R18 | TDO | | | | | |
| R19 | reserved | | | | EE0/DBREQ | |
| R20 | TEST0 | | | | | |
| T1 | $V_{DDM}$ | | | | | |
| T2 | D20 | | | | | |
| T3 | D22 | | | | | |
| T4 | $V_{DDM}$ | | | | | |
| T5 | $V_{DDM}$ | | | | | |
| T6 | $V_{DDC}$ | | | | | |
| T7 | $V_{DDM}$ | | | | | |
| T8 | $V_{DDM}$ | | | | | |
| T9 | $V_{DDC}$ | | | | | |
| T10 | $V_{DDM}$ | | | | | |
| T11 | $V_{DDM}$ | | | | | |
| T12 | $V_{DDIO}$ | | | | | |
| T13 | $V_{DDIO}$ | | | | | |
| T14 | $V_{DDIO}$ | | | | | |
| T15 | $V_{DDIO}$ | | | | | |
| T16 | $V_{DDC}$ | | | | | |
| T17 | $V_{DDC}$ | | | | | |
| T18 | reserved | | | | MDIO | |
| T19 | TMS | | | | | |
| T20 | $\overline{HRESET}$ | | | | | |
| U1 | GND | | | | | |
| U2 | D21 | | | | | |
| U3 | D23 | | | | | |
| U4 | $V_{DDM}$ | | | | | |
| U5 | $V_{DDC}$ | | | | | |
| U6 | $V_{DDC}$ | | | | | |
| U7 | $V_{DDC}$ | | | | | |
| U8 | $V_{DDC}$ | | | | | |
| U9 | $V_{DDC}$ | | | | | |
| U10 | $V_{DDC}$ | | | | | |
| U11 | $V_{DDC}$ | | | | | |
| U12 | $V_{DDC}$ | | | | | |
| U13 | $V_{DDC}$ | | | | | |
| U14 | $V_{DDC}$ | | | | | |
| U15 | $V_{DDC}$ | | | | | |

**Table 1. MSC7113 Signals by Ball Designator (continued)**

| Number | Signal Names | | | | | |
|---|---|---|---|---|---|---|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| U16 | $V_{DDC}$ | | | | | |
| U17 | $V_{DDC}$ | | | | | |
| U18 | reserved | | | | COL | |
| U19 | TCK | | | | | |
| U20 | $\overline{TRST}$ | | | | | |
| V1 | $V_{DDM}$ | | | | | |
| V2 | NC | | | | | |
| V3 | A13 | | | | | |
| V4 | A11 | | | | | |
| V5 | A10 | | | | | |
| V6 | A5 | | | | | |
| V7 | A2 | | | | | |
| V8 | BA0 | | | | | |
| V9 | NC | | | | | |
| V10 | reserved | | | | EVNT0 | |
| V11 | SWTE | GPIA16 | $\overline{IRQ12}$ | GPOA16 | EVNT4 | |
| V12 | GPIA8 | | $\overline{IRQ6}$ | GPOA8 | T0TCK | |
| V13 | GPIA4 | | $\overline{IRQ1}$ | GPOA4 | T1RFS | |
| V14 | GPIA0 | | $\overline{IRQ11}$ | GPOA0 | T1TD | |
| V15 | GPIA28 | | $\overline{IRQ17}$ | GPOA28 | TX_ER | reserved |
| V16 | GPID6 | | | GPOD6 | RXD2 | reserved |
| V17 | GPIA22 | | $\overline{IRQ22}$ | GPOA22 | RXD0 | |
| V18 | GPIA24 | | $\overline{IRQ24}$ | GPOA24 | TX_EN | |
| V19 | reserved | | | | CRS | |
| V20 | TDI | | | | | |
| W1 | GND | | | | | |
| W2 | $V_{DDM}$ | | | | | |
| W3 | A12 | | | | | |
| W4 | A8 | | | | | |
| W5 | A7 | | | | | |
| W6 | A6 | | | | | |
| W7 | A3 | | | | | |
| W8 | NC | | | | | |
| W9 | GPIA17 | | $\overline{IRQ13}$ | GPOA17 | EVNT1 | CLKO |
| W10 | BM0 | GPIC14 | | GPOC14 | EVNT2 | |
| W11 | GPIA10 | | $\overline{IRQ5}$ | GPOA10 | T0RFS | |
| W12 | GPIA7 | | $\overline{IRQ7}$ | GPOA7 | T0TFS | |
| W13 | GPIA3 | | $\overline{IRQ8}$ | GPOA3 | T1RD | |

## 2.2 Recommended Operating Conditions

**Table 3** lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | $V_{DDC}$ | 1.14 to 1.26 | V |
| Memory supply voltage | $V_{DDM}$ | 2.38 to 2.63 | V |
| PLL supply voltage | $V_{DDPLL}$ | 1.14 to 1.26 | V |
| I/O supply voltage | $V_{DDIO}$ | 3.14 to 3.47 | V |
| Reference voltage | $V_{REF}$ | 1.19 to 1.31 | V |
| Operating temperature range | $T_J$<br>$T_A$ | maximum: 105<br>minimum: –40 | °C<br>°C |

## 2.3 Thermal Characteristics

**Table 4** describes thermal characteristics of the MSC7113 for the MAP-BGA package.

**Table 4. Thermal Characteristics for MAP-BGA Package**

| Characteristic | Symbol | MAP-BGA 17 × 17 mm[5] | | Unit |
|---|---|---|---|---|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient[1, 2] | $R_{\theta JA}$ | 39 | 31 | °C/W |
| Junction-to-ambient, four-layer board[1, 3] | $R_{\theta JA}$ | 23 | 20 | °C/W |
| Junction-to-board[4] | $R_{\theta JB}$ | 12 | | °C/W |
| Junction-to-case[5] | $R_{\theta JC}$ | 7 | | °C/W |
| Junction-to-package-top[6] | $\Psi_{JT}$ | 2 | | °C/W |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

**Section 3.1**, *Thermal Design Considerations* explains these characteristics in detail.

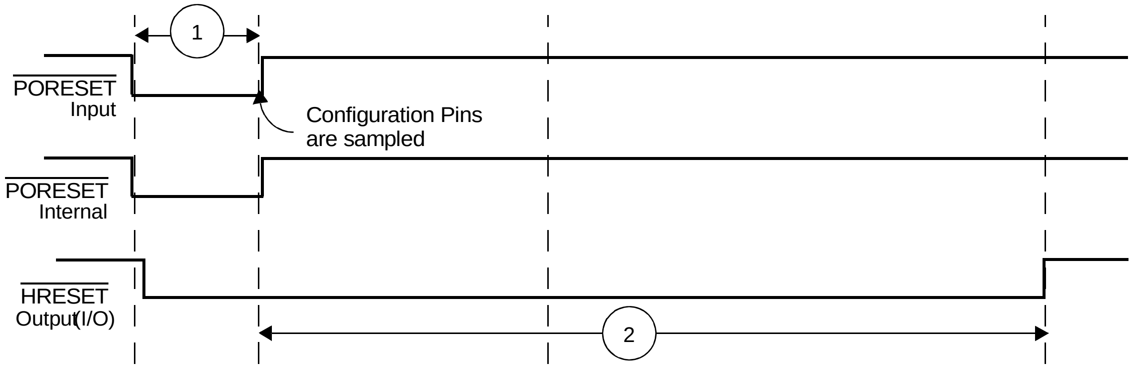



**Figure 4. Timing Diagram for a Reset Configuration Write**

## 2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

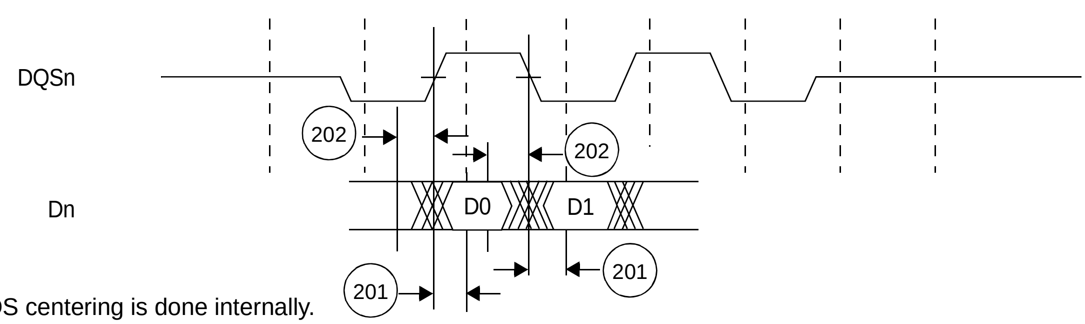
### 2.5.4.1 DDR DRAM Input AC Timing Specifications

**Table 17** provides the input AC timing specifications for the DDR DRAM interface.

**Table 17. DDR DRAM Input AC Timing**

| No. | Parameter | Symbol | Min | Max | | Unit |
|---|---|---|---|---|---|---|
| | | | | Mask Set 1L44X | Mask Set 1M88B | |
| — | AC input low voltage | $V_{IL}$ | — | $V_{REF}$ – 0.31 | $V_{REF}$ – 0.31 | V |
| — | AC input high voltage | $V_{IH}$ | $V_{REF}$ + 0.31 | $V_{DDM}$ + 0.3 | $V_{DDM}$ + 0.3 | V |
| 201 | Maximum Dn input setup skew relative to DQSn input | — | — | 1026 | 900 | ps |
| 202 | Maximum Dn input hold skew relative to DQSn input | — | — | 386 | 900 | ps |

**Notes:**
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if 0 ≤ n ≤ 7).
2. See **Table 18** for $t_{CK}$ value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.




**Note**: DQS centering is done internally.

**Figure 5. DDR DRAM Input Timing Diagram**

**Table 20. TDM Timing**

| No. | Characteristic | Expression | Min | Max | Units |
|---|---|---|---|---|---|
| 307 | TDMxTCK High to TDMxTD output valid | | — | 14.0 | ns |
| 308 | TDMxTD hold time | | 2.0 | — | ns |
| 309 | TDMxTCK High to TDMxTD output high impedance | | — | 10.0 | ns |
| 310 | TDMXTFS/TDMxRFS output valid | | — | 13.5 | ns |
| 311 | TDMxTFS/TDMxRFS output hold time | | 2.5 | — | ns |

**Notes:**
1. Output values are based on 30 pF capacitive load.
2. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. Refer to the *MSC711x Reference Manual* for details. TDMxTCK and TDMxRCK are shown using the rising edge.

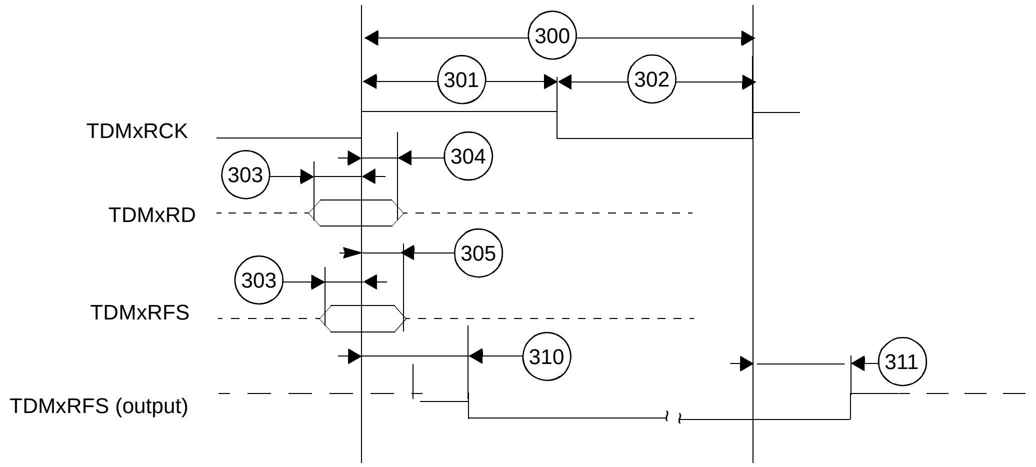



**Figure 8. TDM Receive Signals**

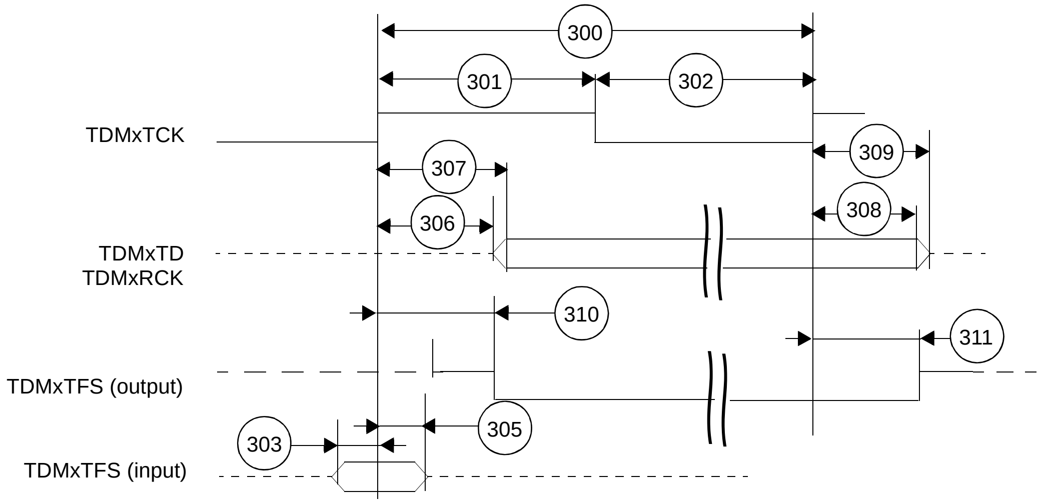



**Figure 9. TDM Transmit Signals**

## 2.5.6 Ethernet Timing

### 2.5.6.1 Receive Signal Timing

**Table 21. Receive Signal Timing**

| No. | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 800 | Receive clock period:<br>• MII: RXCLK (max frequency = 25 MHz)<br>• RMII: REFCLK (max frequency = 50 MHz) | <br>40<br>20 | <br>—<br>— | <br>ns<br>ns |
| 801 | Receive clock pulse width high—as a percent of clock period<br>• MII: RXCLK<br>• RMII: REFCLK | 35<br>14<br>7 | 65<br>—<br>— | %<br>ns<br>ns |
| 802 | Receive clock pulse width low—as a percent of clock period:<br>• MII: RXCLK<br>• RMII: REFCLK | 35<br>14<br>7 | 65<br>—<br>— | %<br>ns<br>ns |
| 803 | RXDn, RX_DV, CRS_DV, RX_ER to receive clock rising edge setup time | 4 | — | ns |
| 804 | Receive clock rising edge to RXDn, RX_DV, CRS_DV, RX_ER hold time | 2 | — | ns |

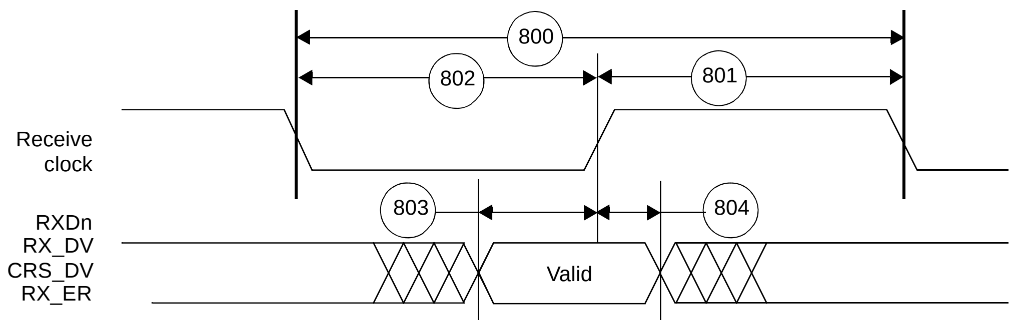



**Figure 10. Ethernet Receive Signal Timing**

## 2.5.7 HDI16 Signals

**Table 25. Host Interface (HDI16) Timing[1, 2]**

| No. | Characteristics[3] | Mask Set 1L44X | | Mask Set 1M88B | | Unit |
|---|---|---|---|---|---|---|
| | | Expression | Value | Expression | Value | |
| 40 | Host Interface Clock period | $T_{HCLK}$ | Note 1 | $T_{CORE}$ | Note 1 | ns |
| 44a | Read data strobe minimum assertion width[4]<br>HACK read minimum assertion width | $3.0 \times T_{HCLK}$ | Note 11 | $2.0 \times T_{CORE} + 9.0$ | Note 11 | ns |
| 44b | Read data strobe minimum deassertion width[4]<br>HACK read minimum deassertion width | $1.5 \times T_{HCLK}$ | Note 11 | $1.5 \times T_{CORE}$ | Note 11 | ns |
| 44c | Read data strobe minimum deassertion width[4] after “Last Data Register” reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7]<br>HACK minimum deassertion width after “Last Data Register” reads[5,6] | $2.5 \times T_{HCLK}$ | Note 11 | $2.5 \times T_{CORE}$ | Note 11 | ns |
| 45 | Write data strobe minimum assertion width[8]<br>HACK write minimum assertion width | $1.5 \times T_{HCLK}$ | Note 11 | $1.5 \times T_{CORE}$ | Note 11 | ns |
| 46 | Write data strobe minimum deassertion width[8]<br>HACK write minimum deassertion width after ICR, CVR and Data Register writes[5] | $2.5 \times T_{HCLK}$ | Note 11 | $2.5 \times T_{CORE}$ | Note 11 | ns |
| 47 | Host data input minimum setup time before write data strobe deassertion[8]<br>Host data input minimum setup time before HACK write deassertion | — | 3.0 | — | 2.5 | ns |
| 48 | Host data input minimum hold time after write data strobe deassertion[8]<br>Host data input minimum hold time after HACK write deassertion | — | 4.0 | — | 2.5 | ns |
| 49 | Read data strobe minimum assertion to output data active from high impedance[4]<br>HACK read minimum assertion to output data active from high impedance | — | 1.0 | — | 1.0 | ns |
| 50 | Read data strobe maximum assertion to output data valid[4]<br>HACK read maximum assertion to output data valid | $(2.0 \times T_{HCLK}) + 8.0$ | Note 11 | $(2.0 \times T_{CORE}) + 8.0$ | Note 11 | ns |
| 51 | Read data strobe maximum deassertion to output data high impedance[4]<br>HACK read maximum deassertion to output data high impedance | — | 8.0 | — | 9.0 | ns |
| 52 | Output data minimum hold time after read data strobe deassertion[4]<br>Output data minimum hold time after HACK read deassertion | — | 1.0 | — | 1.0 | ns |
| 53 | HCS[1–2] minimum assertion to read data strobe assertion[4] | — | 0.0 | — | 0.5 | ns |
| 54 | HCS[1–2] minimum assertion to write data strobe assertion[8] | — | 0.0 | — | 0.0 | ns |
| 55 | HCS[1–2] maximum assertion to output data valid | $(2.0 \times T_{HCLK}) + 8.0$ | Note 11 | $(2.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 56 | HCS[1–2] minimum hold time after data strobe deassertion[9] | — | 0.0 | — | 0.5 | ns |
| 57 | HA[0–3], HRW minimum setup time before data strobe assertion[9] | — | 5.0 | — | 5.0 | ns |
| 58 | HA[0–3], HRW minimum hold time after data strobe deassertion[9] | — | 5.0 | — | 5.0 | ns |
| 61 | Maximum delay from read data strobe deassertion to host request deassertion for “Last Data Register” read[4, 5, 10] | $(3.0 \times T_{HCLK}) + 8.0$ | Note 11 | $(3.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 62 | Maximum delay from write data strobe deassertion to host request deassertion for “Last Data Register” write[5,8,10] | $(3.0 \times T_{HCLK}) + 8.0$ | Note 11 | $(3.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 63 | Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion. | $(2.0 \times T_{HCLK}) + 1.0$ | Note 11 | $(2.0 \times T_{CORE}) + 1.0$ | Note 11 | ns |
| 64 | Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion | $(5.0 \times T_{HCLK}) + 8.0$ | Note 11 | $(5.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |

### 2.5.9 UART Timing

**Table 27. UART Timing**

| No. | Characteristics | Expression | Mask Set 1L44X | | Mask Set 1M88B | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| — | Internal bus clock (APBCLK) | $F_{CORE}/2$ | — | 100 | — | 133 | MHz |
| — | Internal bus clock period (1/APBCLK) | $T_{APBCLK}$ | 10.0 | — | 7.52 | — | ns |
| 400 | URXD and UTXD inputs high/low duration | $16 \times T_{APBCLK}$ | 160.0 | — | 120.3 | — | ns |
| 401 | URXD and UTXD inputs rise/fall time | | — | 5 | — | 5 | ns |
| 402 | UTXD output rise/fall time | | — | 5 | — | 5 | ns |

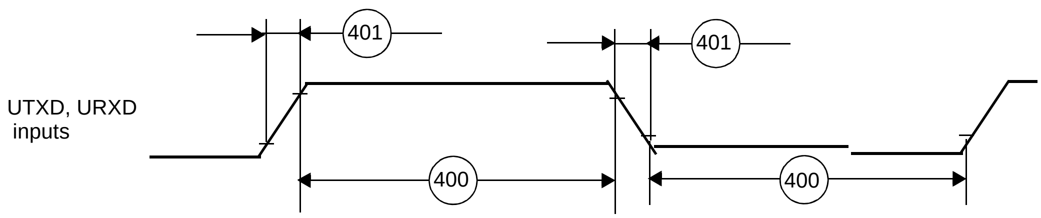



**Figure 21. UART Input Timing**

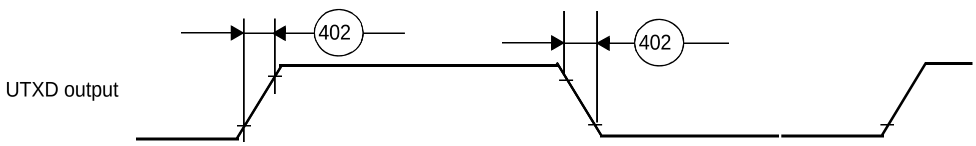



**Figure 22. UART Output Timing**

### 2.5.10 EE Timing

**Table 28. EE0 Timing**

| Number | Characteristics | Type | Min |
|---|---|---|---|
| 65 | EE0 input to the core | Asynchronous | 4 core clock periods |
| 66 | EE0 output from the core | Synchronous to core clock | 1 core clock period |

**Notes:**
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC1400 Core Reference Manual* for details.
3. Refer to **Table 14** for details on EE pin functionality.

**Figure 23** shows the signal behavior of the EE pin.

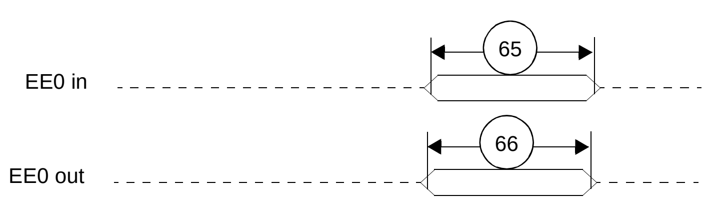



**Figure 23. EE Pin Timing**

## 2.5.11 Event Timing

**Table 29. EVNT Signal Timing**

| Number | Characteristics | Type | Min |
|---|---|---|---|
| 67 | EVNT as input | Asynchronous | 1.5 × APBCLK periods |
| 68 | EVNT as output | Synchronous to core clock | 1 APBCLK period |

**Notes:**
1. Refer to **Table 27** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to the *MSC711x Reference Manual* for details on EVNT pin functionality.

**Figure 24** shows the signal behavior of the EVNT pin.

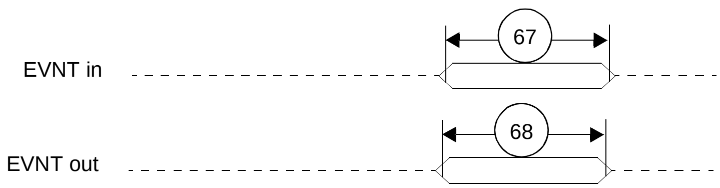



**Figure 24. EVNT Pin Timing**

## 2.5.12 GPIO Timing

**Table 30. GPIO Signal Timing[1,2,3]**

| Number | Characteristics | Type | Min |
|---|---|---|---|
| 601 | GPI[4.5] | Asynchronous | 1.5 × APBCLK periods |
| 602 | GPO[5] | Synchronous to core clock | 1 APBCLK period |
| 603 | Port A edge-sensitive interrupt | Asynchronous | 1.5 × APBCLK periods |
| 604 | Port A level-sensitive interrupt | Asynchronous | 3 × APBCLK periods[6] |

**Notes:**
1. Refer to **Table 27** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to *MSC711x Reference Manual* for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPA_DR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The input and output signals cannot toggle faster than 50 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

**Figure 25** shows the signal behavior of the GPI/GPO pin.

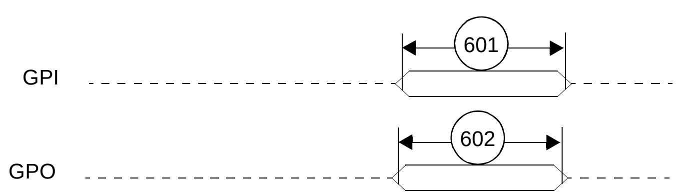



**Figure 25. GPI/GPO Pin Timing**

## 2.5.13 JTAG Signals

**Table 31. JTAG Timing**

| No. | Characteristics | All frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 700 | TCK frequency of operation (1/($T_C \times 3$); maximum 22 MHz) | 0.0 | 40.0 | MHz |
| 701 | TCK cycle time | 25.0 | — | ns |
| 702 | TCK clock pulse width measured at $V_{M\,=}$ 1.6 V | 11.0 | — | ns |
| 703 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 704 | Boundary scan input data set-up time | 5.0 | — | ns |
| 705 | Boundary scan input data hold time | 14.0 | — | ns |
| 706 | TCK low to output data valid | 0.0 | 20.0 | ns |
| 707 | TCK low to output high impedance | 0.0 | 20.0 | ns |
| 708 | TMS, TDI data set-up time | 5.0 | — | ns |
| 709 | TMS, TDI data hold time | 25.0 | — | ns |
| 710 | TCK low to TDO data valid | 0.0 | 24.0 | ns |
| 711 | TCK low to TDO high impedance | 0.0 | 10.0 | ns |
| 712 | $\overline{\text{TRST}}$ assert time | 100.0 | — | ns |
| **Note:** | All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface. | | | |

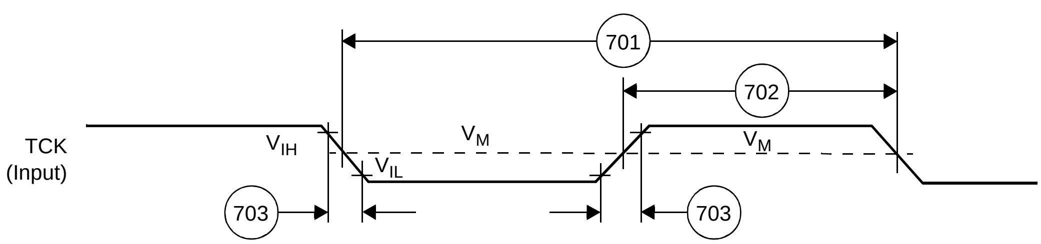



**Figure 26. Test Clock Input Timing Diagram**

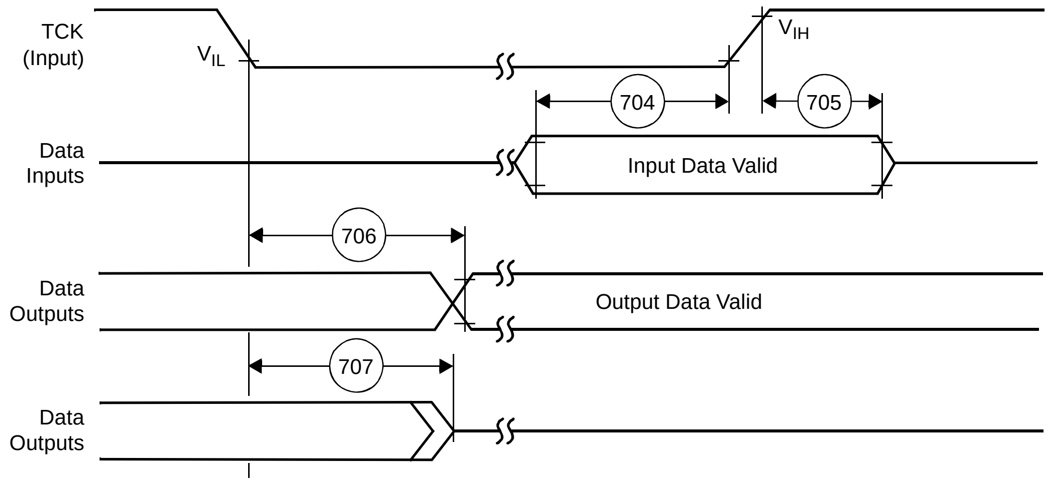



**Figure 27. Boundary Scan (JTAG) Timing Diagram**

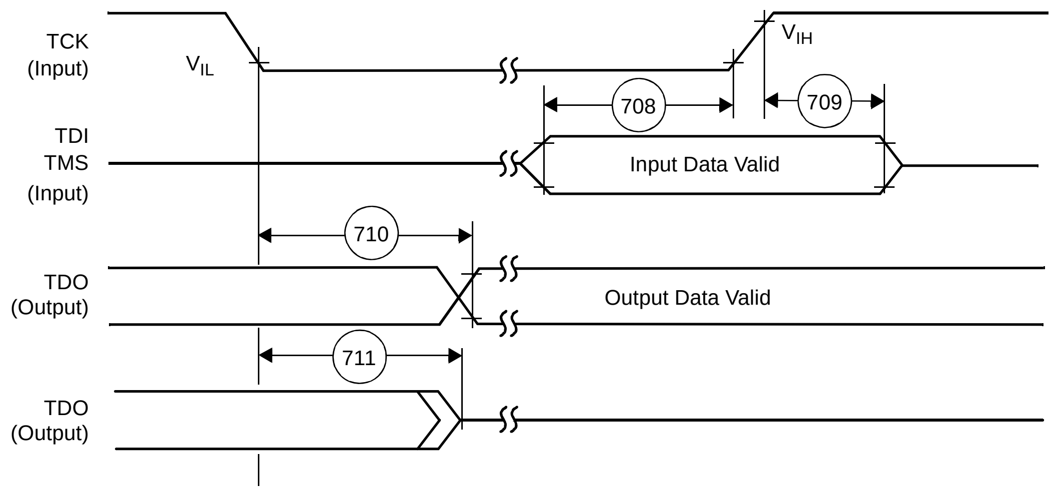



**Figure 28. Test Access Port Timing Diagram**

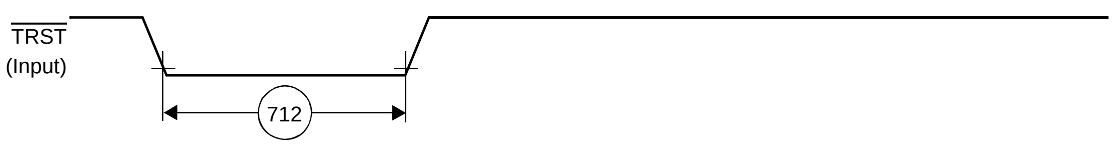



**Figure 29. $\overline{\text{TRST}}$ Timing Diagram**

# 3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7113 device into a system design.

## 3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, $T_J$, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

$T_A$ = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7113 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 $W/cm^2$ with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If $T_J$ appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine $T_J$:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 2}$$

where

$T_T$ = thermocouple (or infrared) temperature on top of the package (°C)

$\Psi_{JT}$ = thermal characterization parameter (°C/W)

$P_D$ = power dissipation in the package (W)

### 3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the $V_{DDIO}$ (3.3 V) supply first.
2. Turn on the $V_{DDC}$ (1.2 V) supply second.
3. Turn on the $V_{DDM}$ (2.5 V) supply third.
4. Turn on the $V_{REF}$ (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the $V_{REF}$ (1.25 V) supply first.
2. Turn off the $V_{DDM}$ (2.5 V) supply second.
3. Turn off the $V_{DDC}$ (1.2 V) supply third.
4. Turn of the $V_{DDIO}$ (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of $V_{DDIO}$ and $V_{DDC}$ is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for $V_{DDC}$ and $V_{DDM}$ is less than 10 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 1.

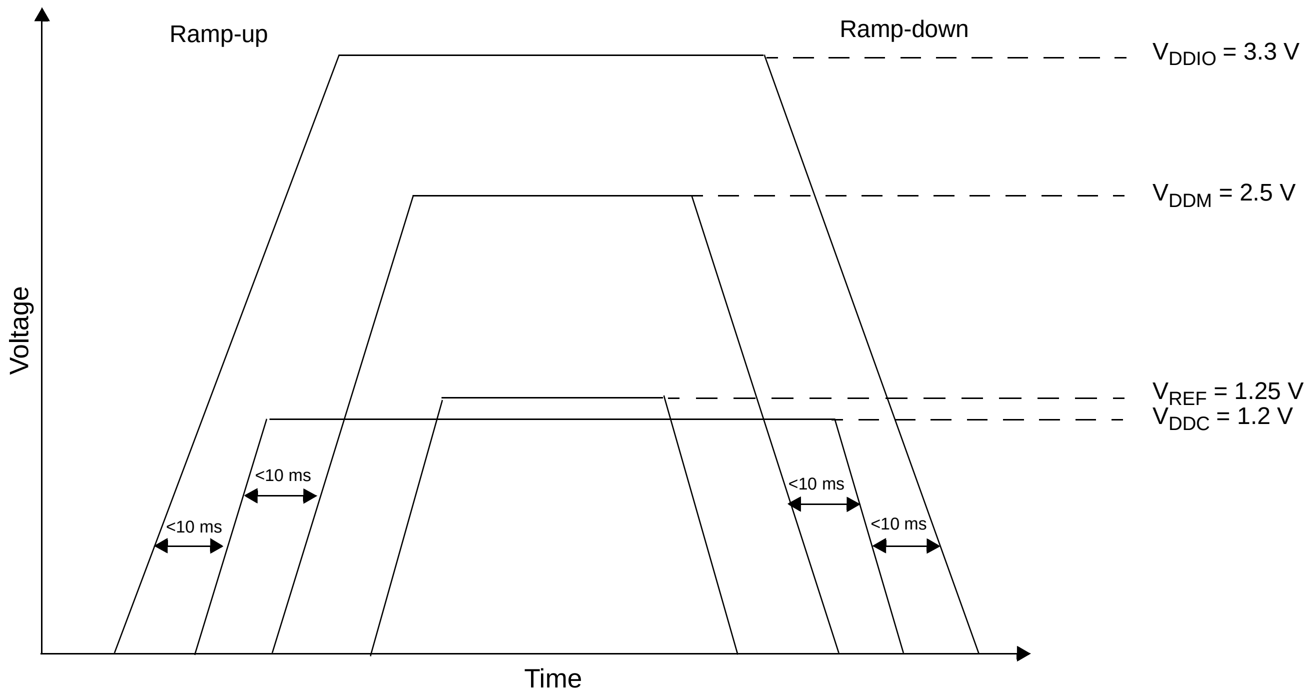



**Figure 30. Voltage Sequencing Case 1**

### 3.2.2.2 Case 2

The power-up sequence is as follows:

1. Turn on the $V_{DDIO}$ (3.3 V) supply first.
2. Turn on the $V_{DDC}$ (1.2 V) and $V_{DDM}$ (2.5 V) supplies simultaneously (second).
3. Turn on the $V_{REF}$ (1.25 V) supply last (third).

**Note:** Make sure that the time interval between the ramp-up of $V_{DDIO}$ and $V_{DDC}$/$V_{DDM}$ is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the $V_{REF}$ (1.25 V) supply first.
2. Turn off the $V_{DDM}$ (2.5 V) supply second.
3. Turn off the $V_{DDC}$ (1.2 V) supply third.
4. Turn of the $V_{DDIO}$ (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for $V_{DDIO}$ and $V_{DDC}$ is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for $V_{DDC}$ and $V_{DDM}$ is less than 10 ms for power-up and power-down.
- Refer to **Figure 31** for relative timing for Case 2.

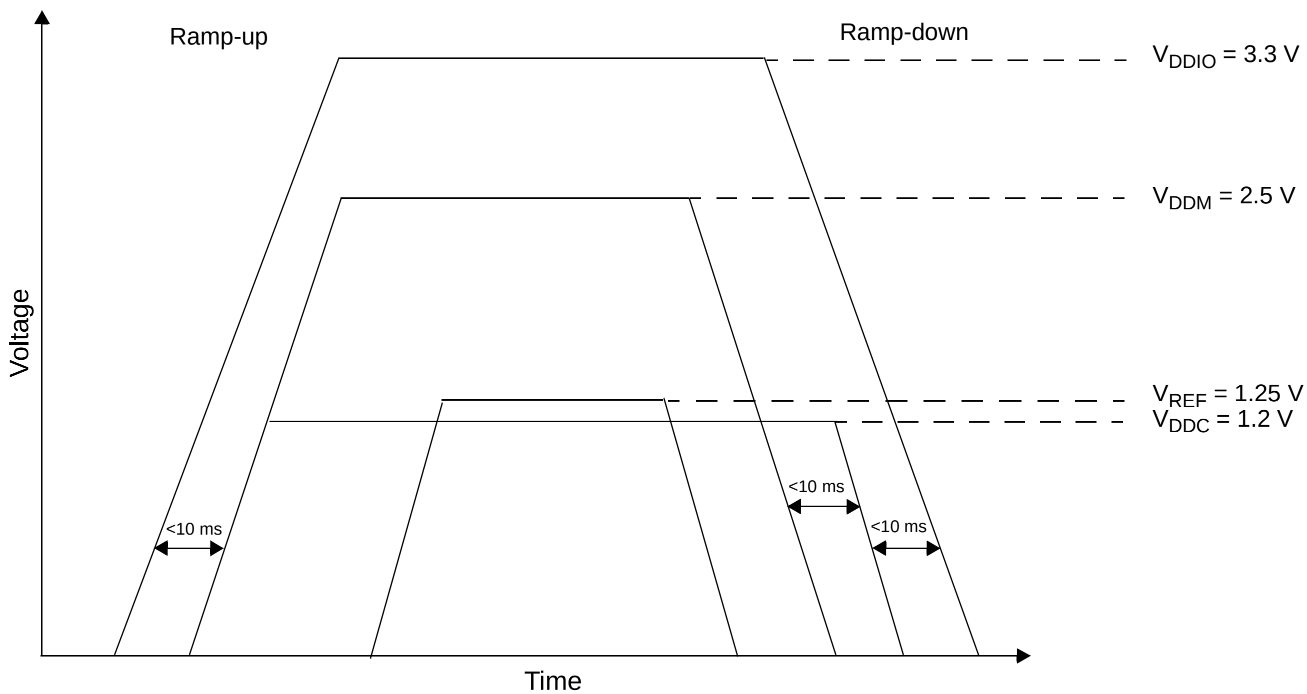



**Figure 31. Voltage Sequencing Case 2**

### 3.2.3 Power Planes

Each power supply pin ($V_{DDC}$, $V_{DDM}$, and $V_{DDIO}$) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC7113 $V_{DDC}$ power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 3.5** for DDR Controller power guidelines.

### 3.2.4 Decoupling

Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a 0.01 µF high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one 10 µF and one 47 µF, (with low ESR and ESL) mounted as closely as possible to the MSC7113 voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A.

### 3.2.5 PLL Power Supply Filtering

The MSC7113 $V_{DDPLL}$ power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. $V_{DDPLL}$ can be connected to $V_{DDC}$ through a 2 Ω resistor. $V_{SSPLL}$ can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 35** is recommended. The PLL loop filter should be placed as closely as possible to the $V_{DDPLL}$ pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits.The 0.01 µF capacitor should be closest to $V_{DDPLL}$, followed by the 0.1 µF capacitor, the 10 µF capacitor, and finally the 2-Ω resistor to $V_{DDC}$. These traces should be kept short.

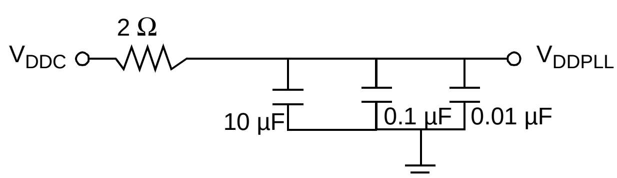



**Figure 35. PLL Power Supply Filter Circuits**

### 3.2.6 Power Consumption

You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:

- *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
- *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
- *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
- *Peripheral subsystem*. Halt the individual on-device peripherals such as the DDR memory controller, Ethernet MAC, HDI16, TDM, UART, $I^2C$, and timer modules.

For details, see the “Clocks and Power Management” chapter of the *MSC711x Reference Manual*.

### 3.3.2 Peripheral Power

Peripherals include the DDR memory controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the $I^2C$ module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 100 MH or 133 MHz. This yields:

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 100\ MHz \times 10^{-3} = 2.88\ mW\ per\ peripheral \qquad \text{Eqn. 7}$$

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 133\ MHz \times 10^{-3} = 3.83\ mW\ per\ peripheral \qquad \text{Eqn. 8}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption.

### 3.3.3 External Memory Power

Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC7113 device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. The dynamic power is computed, however, using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$P_{DDRIO} = P_{STATIC} + P_{DYNAMIC} \qquad \text{Eqn. 9}$$

$$P_{STATIC} = (unused\ pins \times \%\ driven\ high) \times 16\ mA \times 2.5\ V \qquad \text{Eqn. 10}$$

$$P_{DYNAMIC} = (pin\ activity\ value) \times 20\ pF \times (0.4\ V)^2 \times 200\ MHz \times 10^{-3}\ mW \qquad \text{Eqn. 11}$$

$$P_{DYNAMIC} = (pin\ activity\ value) \times 20\ pF \times (0.4\ V)^2 \times 266\ MHz \times 10^{-3}\ mW \qquad \text{Eqn. 12}$$

$$pin\ activity\ value = (active\ data\ lines \times \%\ activity \times \%\ data\ switching) + (active\ address\ lines \times \%\ activity) \qquad \text{Eqn. 13}$$

As an example, assume the following:

unused pins = 16 (DDR uses 16-pin mode)
% driven high = 50%
active data lines = 16
% activity = 60%
% data switching = 50%
active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 200 \times 10^{-3}) = 324.2\ mW \qquad \text{Eqn. 14}$$

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 266 \times 10^{-3}) = 326.3\ mW \qquad \text{Eqn. 15}$$

### 3.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz or 33 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 25\ MHz \times 10^{-3} = 5.44\ mW\ per\ I/O\ line \qquad \text{Eqn. 16}$$

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 33\ MHz \times 10^{-3} = 7.19\ mW\ per\ I/O\ line \qquad \text{Eqn. 17}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

**Note:** The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

### 3.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

### 3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL}\ (200\ MHz\ core) = 216 + (4 \times 2.88) + 324{,}2 + (10 \times 5.44) + 64 = 670.12\ mW \qquad \text{Eqn. 18}$$

$$P_{TOTAL}\ (266\ MHz\ core) = 287 + (4 \times 3.83) + 326.3 + (10 \times 7.19) + 64 = 764.52\ mW \qquad \text{Eqn. 19}$$

## 3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7113 at reset and boot.

### 3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7113 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

### 3.4.2 Reset Configuration Pins

**Table 34** shows the MSC7113 reset configuration signals. These signals are sampled at the deassertion (rising edge) of PORESET. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

**Table 34. Reset Configuration Signals**

| Signal | Description | Settings | |
|---|---|---|---|
| BM[1–0] | Determines boot mode. | 0 | Boot from HDI16 port. |
| | | 01 | Boot from I2C. |
| | | 1x | Reserved. |
| SWTE | Determines watchdog functionality. | 0 | Watchdog timer disabled. |
| | | 1 | Watchdog timer enabled. |
| HDSP | Configures HDI16 strobe polarity. | 0 | Host Data strobes active low. |
| | | 1 | Host Data strobes active high. |
| H8BIT | Configures HDI16 operation mode. | 0 | HDI16 port configured for 16-bit operation. |
| | | 1 | HDI16 port configured for 8-bit operation. |

### 3.4.3 Boot

After a power-on reset, the PLL is bypassed and the device is directly clocked from the CLKIN pin. Using this input clock, the system initializes using the boot loader program that resides in the internal ROM. After initialization, the DSP core can enable the PLL and start the device operating at a higher speed. The MSC7113 can boot from an external host through the HDI16 or download a user program through the $I^2C$ port. The boot operating mode is set by configuring the BM[1–0] signals sampled at the rising edge of PORESET, as shown in **Table 35**.

**Table 35. Boot Mode Settings**

| BM1 | BM0 | Boot Source |
|---|---|---|
| 0 | 0 | External host via HDI16 with the PLL disabled. |
| 0 | 1 | $I^2C$. |
| 1 | 0 | External host via the HDI16 with the PLL enabled. |
| 1 | 1 | Reserved. |

#### 3.4.3.1 HDI16 Boot

If the MSC7113 device boots from an external host through the HDI16, the port is configured as follows:

- Operate in Non-DMA mode.
- Operate in polled mode on the device side.
- Operate in polled mode on the external host side.
- External host must write four 16-bit values at a time with the first word as the most significant and the fourth word as the least significant.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

**Note:** When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.