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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

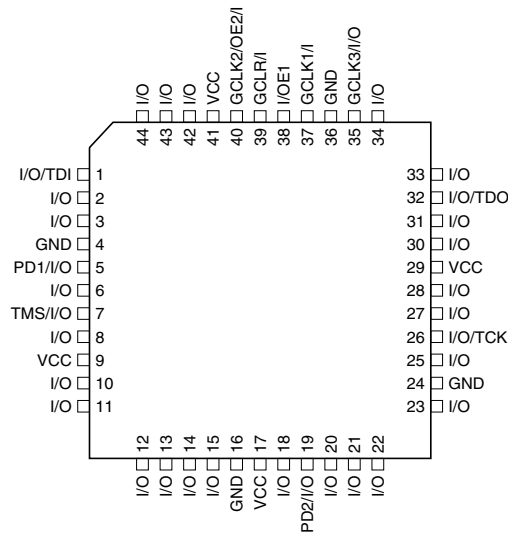
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1502asv-15ji44">https://www.e-xfl.com/product-detail/microchip-technology/atf1502asv-15ji44</a>

## 1. Description

The ATF1502ASV is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1502ASV's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1502ASV has up to 32 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

**Figure 1-1.** 44-lead TQFP Top View



**Figure 1-2.** 44-lead PLCC Top View

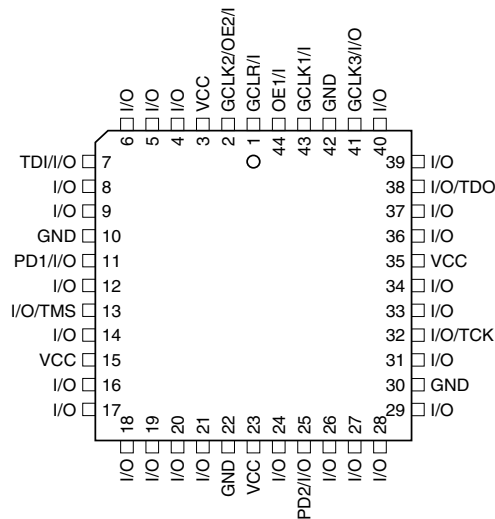
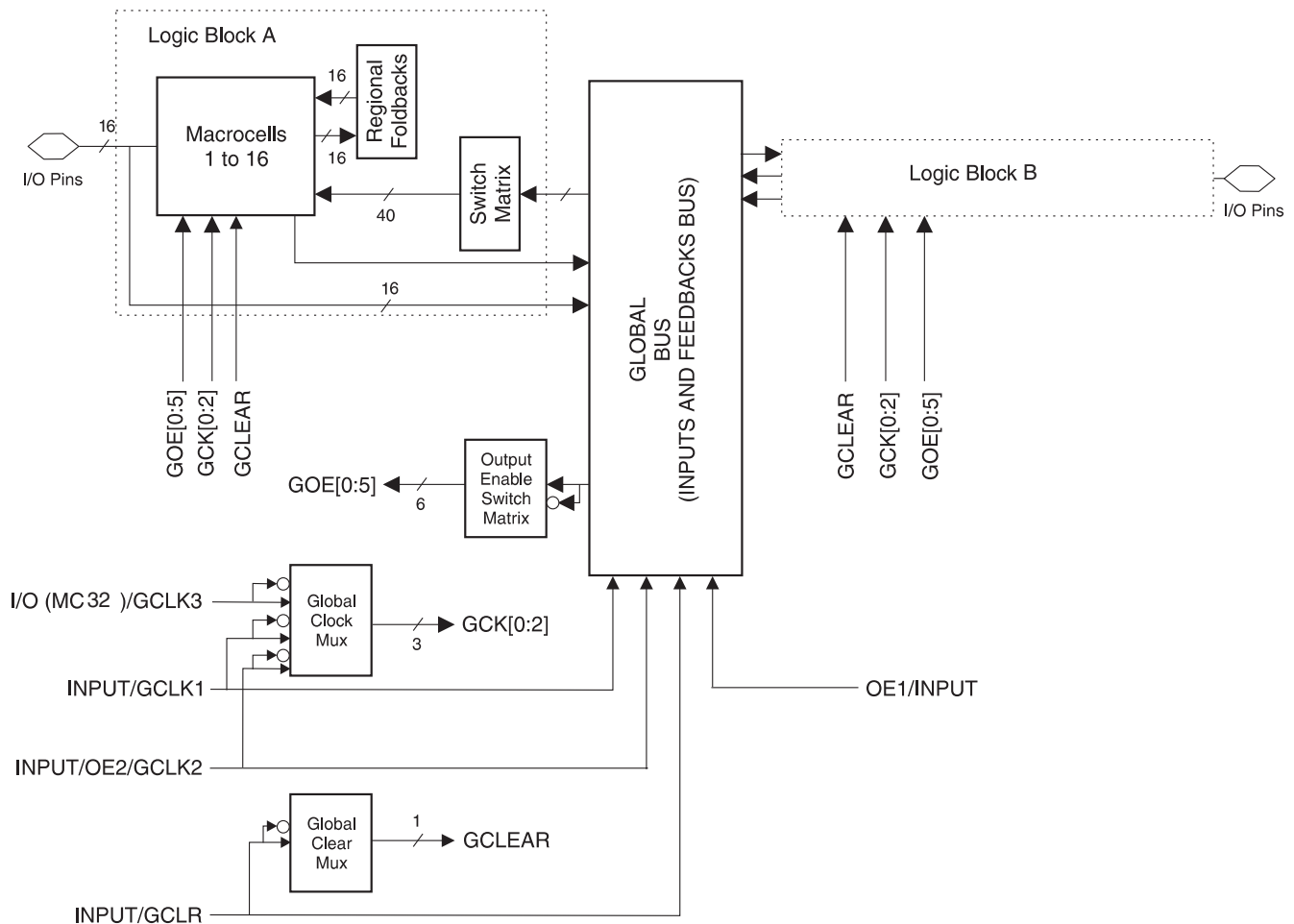


Figure 1-3. Block Diagram



Each of the 32 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1502ASV allows fast, efficient generation of complex logic functions. The ATF1502ASV contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1502ASV macrocell, shown in Figure 1, is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1502ASV. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1502ASV device is an in-system programmable (ISP) device. It uses the industry standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from

### **1.3 Flip-flop**

The ATF1502ASV's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either one of the Global CLK signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

### **1.4 Extra Feedback**

The ATF1502ASV macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

### **1.5 I/O Control**

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

### **1.6 Global Bus/Switch Matrix**

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 32 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

### **1.7 Foldback Bus**

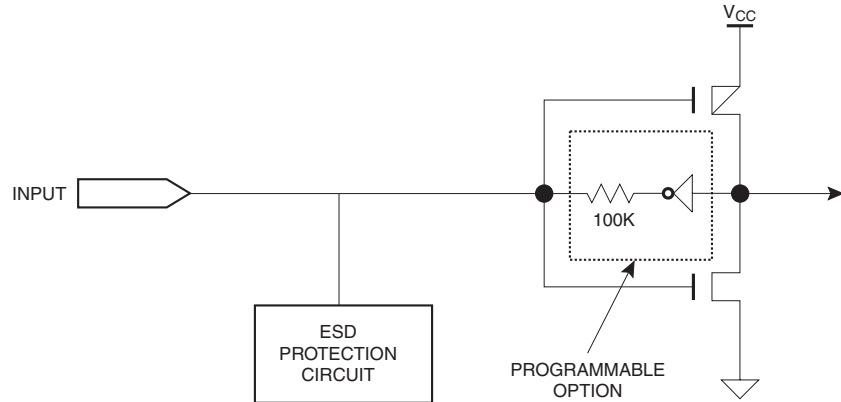
Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The four foldback terms in each region allow generation of high fan-in sum terms (up to nine product terms) with little additional delay.

## **2. Programmable Pin-keeper Option for Inputs and I/Os**

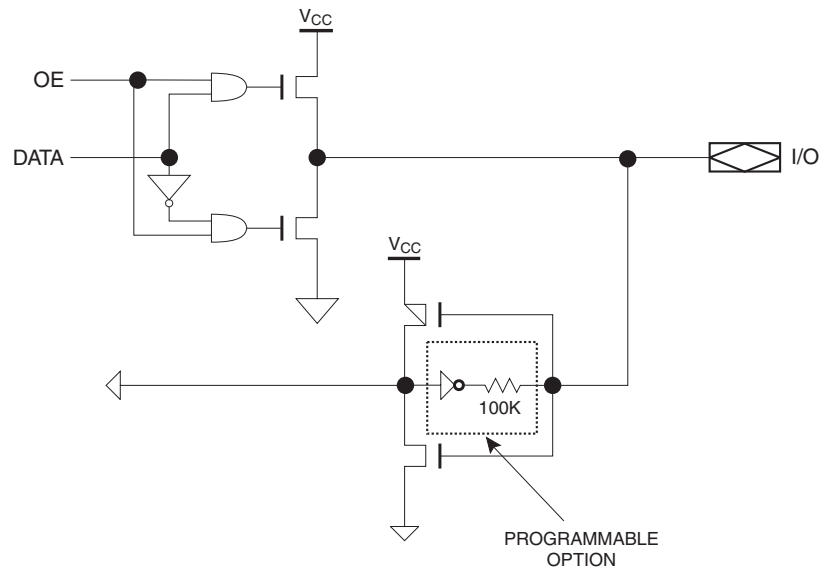
The ATF1502ASV offers the option of programming all input and I/O pins so that pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents unused input and I/O lines from

floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

**Figure 2-1.** Input Diagram



**Figure 2-2.** I/O Diagram



### 3. Speed/Power Management

The ATF1502ASV has several built-in speed and power management features.

To further reduce power, each ATF1502ASV macrocell has a reduced-power bit feature. To reduce power consumption this feature may be activated (by changing the default value of OFF to ON) for any or all macrocells.

The ATF1502ASV also has an optional power-down mode. In this mode, current drops to below 15 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder,  $t_{RPA}$ , must be added to the AC parameters, which include the data paths  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{ACH}$  and  $t_{SEXP}$ .

The ATF1502ASV macrocell also has an option whereby the power can be reduced on a per-macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

## 4. Power-up Reset

The ATF1502ASV is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during  $T_D$ .

The ATF1502ASV has two options for the hysteresis about the reset level,  $V_{RST}$ , Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-up Reset hysteresis set to Large. For conversions, Atmel POF2JED users should include the flag “-power\_reset” on the command line after “filename.POF”. To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If  $V_{CC}$  falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active,  $I_{CC}$  is reduced by several hundred microamps as well.

## 5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1502ASV fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

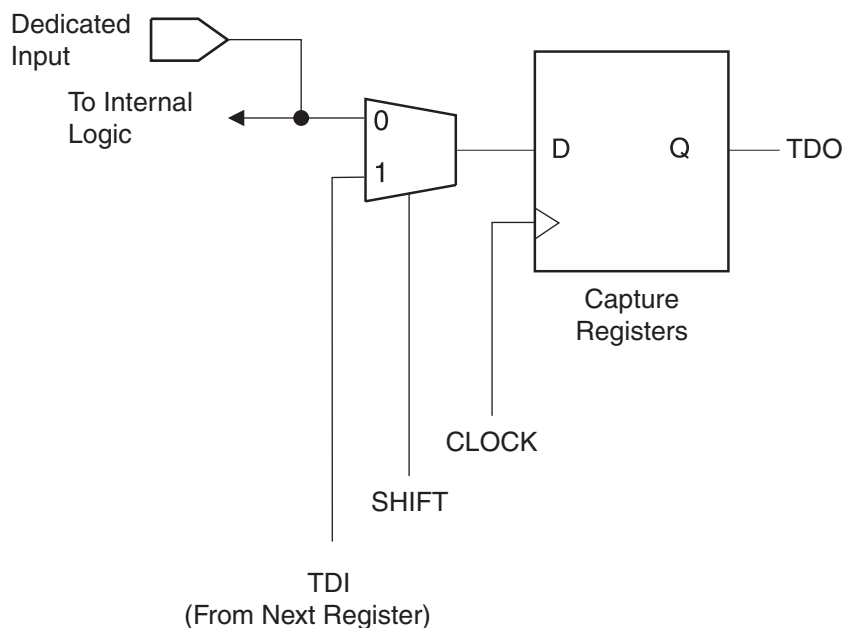
## 6. Programming

ATF1502ASV devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells is shown below.

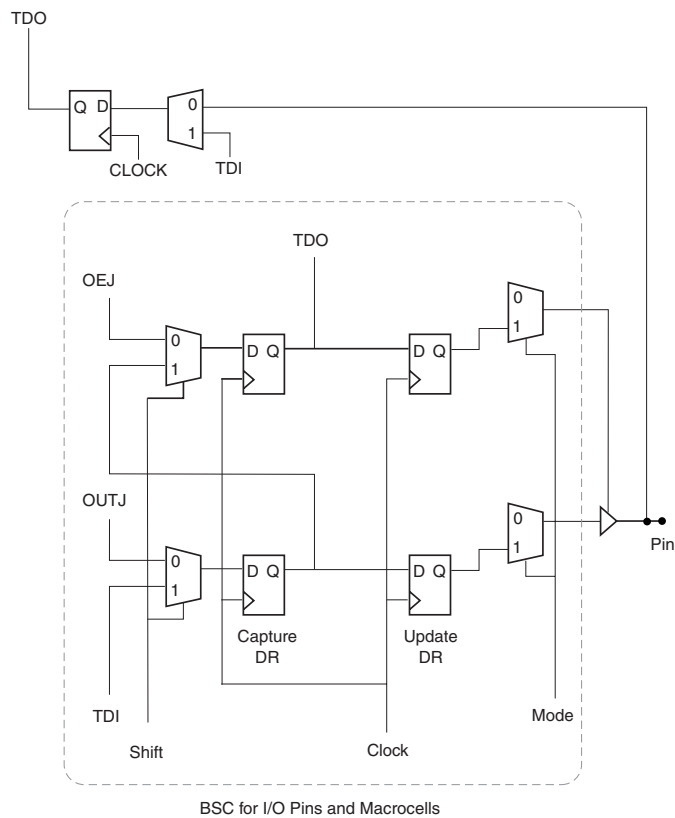
## 7.2 BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)

**Figure 7-1.** BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



**Note:** The ATF1502ASV has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

**Figure 7-2.** BSC Configuration for Macrocells



## 8. Design Software Support

ATF1502ASV designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.



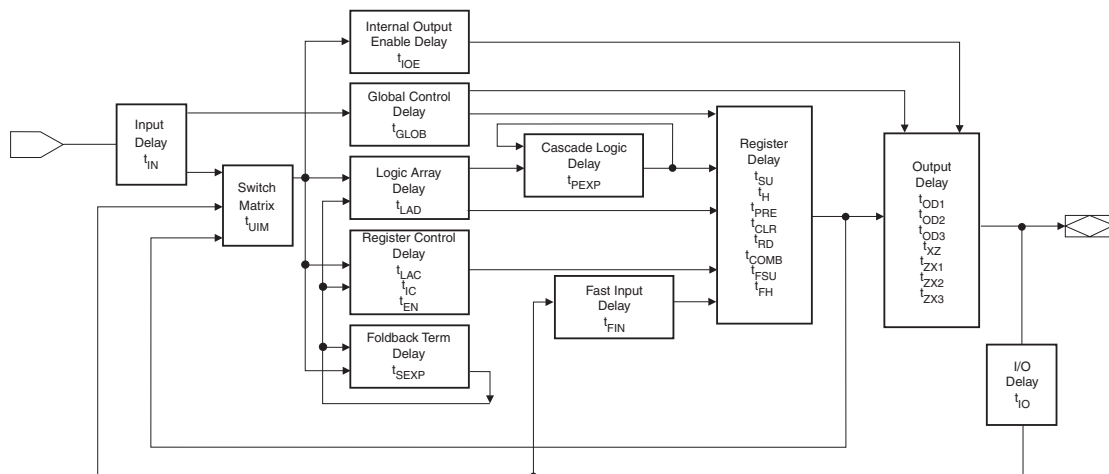
**Table 9-4.** DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>				-2	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current					2	10	
I <sub>OZ</sub>	Tri-state Output Off-state Current	V <sub>O</sub> = V <sub>CC</sub> or GND			-40		40	μA
I <sub>CC1</sub>	Power Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		40		mA
				Ind.		45		mA
I <sub>CC2</sub>	Power Supply Current, Power-down Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	“PD” Mode			0.75	5.0	mA
I <sub>CC3</sub> <sup>(2)</sup>	Reduced-power Mode Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		25		mA
				Ind.		30		mA
V <sub>IL</sub>	Input Low Voltage				-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage				2.0		V <sub>CCINT</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = MIN, I <sub>OL</sub> = 8 mA		Com.			0.45	V
				Ind.			0.45	
	Output Low Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = MIN, I <sub>OL</sub> = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V <sub>OH</sub>	Output High Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = MIN, I <sub>OH</sub> = 2.0 mA				2.4		V
	Output High Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = MIN, I <sub>OH</sub> = -0.1 mA			V <sub>CCIO</sub> - 0.2			

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.  
2.  $I_{CC3}$  refers to the current in the reduced-power mode when macrocell reduced-power is turned on.

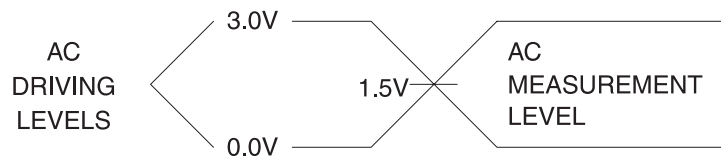
## 10. Timing Model

Figure 10-1. Timing Model



## 11. Input Test Waveforms and Measurement Levels

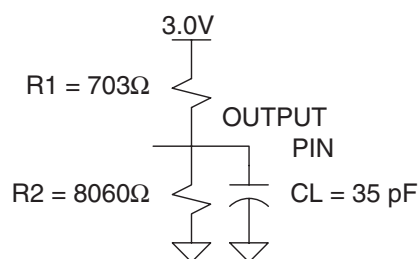
Figure 11-1. Input Test Waveforms and Measurement Levels



$t_R, t_F = 1.5 \text{ ns typical}$

## 12. Output AC Test Loads

Figure 12-1. Output AC Test Loads



## 13. AC Characteristics

Table 13-1. AC Characteristics <sup>(1)</sup>

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
$t_{PD1}$	Input or Feedback to Non-registered Output	3	15		20	ns
$t_{PD2}$	I/O Input or Feedback to Non-registered Feedback	3	12		16	ns
$t_{SU}$	Global Clock Setup Time	11		16		ns
$t_H$	Global Clock Hold Time	0		0		ns
$t_{FSU}$	Global Clock Setup Time of Fast Input	3		3		ns
$t_{FH}$	Global Clock Hold Time of Fast Input	1		1.5		MHz
$t_{COP}$	Global Clock to Output Delay		8		10	ns
$t_{CH}$	Global Clock High Time	5		6		ns
$t_{CL}$	Global Clock Low Time	5		6		ns
$t_{ASU}$	Array Clock Setup Time	4		4		ns
$t_{AH}$	Array Clock Hold Time	4		5		ns
$t_{ACOP}$	Array Clock Output Delay		15		20	ns
$t_{ACH}$	Array Clock High Time	6		8		ns
$t_{ACL}$	Array Clock Low Time	6		8		ns
$t_{CNT}$	Minimum Clock Global Period		13		16	ns
$f_{CNT}$	Maximum Internal Global Clock Frequency	76.9		66		MHz
$t_{ACNT}$	Minimum Array Clock Period		13		16	ns
$f_{ACNT}$	Maximum Internal Array Clock Frequency	76.9		66		MHz
$f_{MAX}$	Maximum Clock Frequency	100		83.3		MHz
$t_{IN}$	Input Pad and Buffer Delay		2		2	ns
$t_{IO}$	I/O Input Pad and Buffer Delay		2		2	ns
$t_{FIN}$	Fast Input Delay		2		2	ns
$t_{SEXP}$	Foldback Term Delay		8		10	ns
$t_{PEXP}$	Cascade Logic Delay		1		1	ns
$t_{LAD}$	Logic Array Delay		6		7	ns
$t_{LAC}$	Logic Control Delay		6		7	ns
$t_{IOE}$	Internal Output Enable Delay		3		3	ns
$t_{OD1}$	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{CC} = 3.3V$ ; $C_L = 35$ pF)		5		5	ns
$t_{ZX1}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$ ; $C_L = 35$ pF)		7		9	ns
$t_{ZX2}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$ ; $C_L = 35$ pF)		7		9	ns

## 14. Power-down Mode

The ATF1502ASV includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 3 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

**Table 14-1.** Power-down AC Characteristics<sup>(1)(2)</sup>

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
$t_{IVDH}$	Valid I, I/O before PD High	15		20		ns
$t_{GVDH}$	Valid OE <sup>(2)</sup> before PD High	15		20		ns
$t_{CVDH}$	Valid Clock <sup>(2)</sup> before PD High	15		20		ns
$t_{DHIX}$	I, I/O Don't Care after PD High		25		30	ns
$t_{DHGX}$	OE <sup>(2)</sup> Don't Care after PD High		25		30	ns
$t_{DHCX}$	Clock <sup>(2)</sup> Don't Care after PD High		25		30	ns
$t_{DLIV}$	PD Low to Valid I, I/O		1		1	μs
$t_{DLGV}$	PD Low to Valid OE <sup>(2)</sup>		1		1	μs
$t_{DLCV}$	PD Low to Valid Clock <sup>(2)</sup>		1		1	μs
$t_{DLOV}$	PD Low to Valid Output		1		1	μs

- Notes: 1. For slow slew outputs, add  $t_{SSO}$ .  
2. Pin or product term.

## 15. ATF1502ASV Dedicated Pinouts

Figure 15-1. ATF1502ASV Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead J-lead
INPUT/OE2/GCLK2	40	2
INPUT/GCLR	39	1
INPUT/OE1	38	44
INPUT/GCLK1	37	43
I/O / GCLK3	35	41
I/O / PD (1,2)	5, 19	11, 25
I/O / TDI (JTAG)	1	7
I/O / TMS (JTAG)	7	13
I/O / TCK (JTAG)	26	32
I/O / TDO (JTAG)	32	38
GND	4, 16, 24, 36	10, 22, 30, 42
V <sub>CCI</sub>	9, 17, 29, 41	3, 15, 23, 35
# of Signal Pins	36	36
# User I/O Pins	32	32

OE (1, 2)

Global OE pins

GCLR

Global Clear pin

GCLK (1, 2, 3)

Global Clock pins

PD (1, 2)

Power-down pins

TDI, TMS, TCK, TDO

JTAG pins used for boundary-scan testing or in-system programming

GND

Ground pins

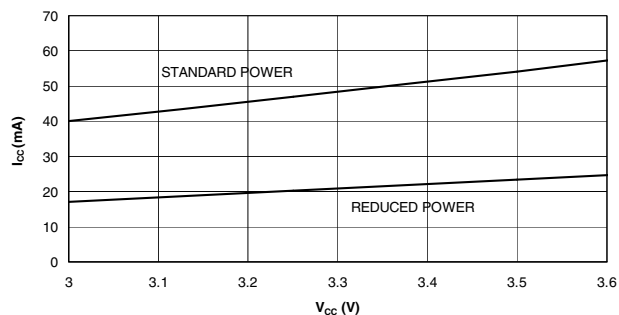
V<sub>CCI</sub>

VCC pins for the device (+3.3V)

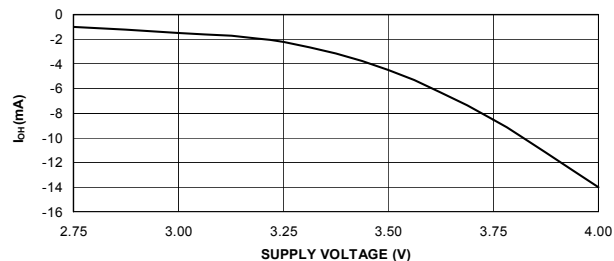
**Figure 15-2.** ATF1502ASV I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP
1	A	4	42
2	A	5	43
3	A	6	44
4/TDI	A	7	1
5	A	8	2
6	A	9	3
7/PD1	A	11	5
8	A	12	6
9/TMS	A	13	7
10	A	14	8
11	A	16	10
12	A	17	11
13	A	18	12
14	A	19	13
15	A	20	14
16	A	21	15
17	B	41	35
18	B	40	34
19	B	39	33
20/TDO	B	38	32
21	B	37	31
22	B	36	30
23	B	34	28
24	B	33	27
25/TCK	B	32	26
26	B	31	25
27	B	29	23
28	B	28	22
29	B	27	21
30	B	26	20
31/PD2	B	25	19
32	B	24	18

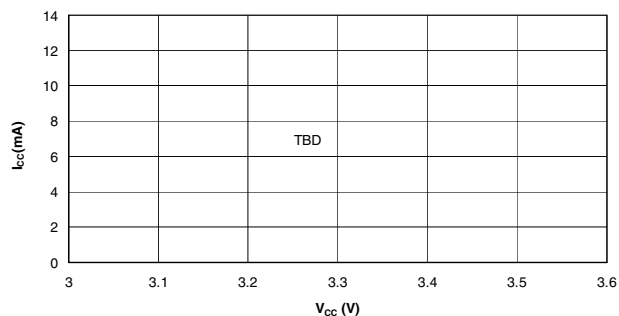
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
ASV VERSION ( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



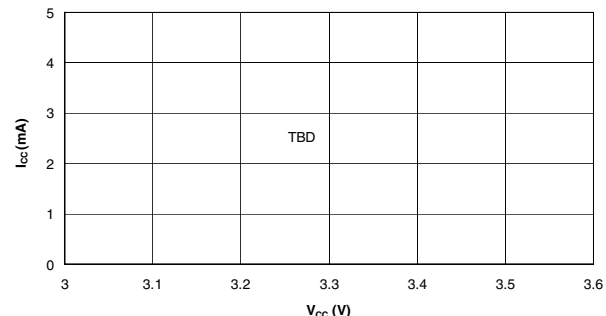
**OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE**  
( $V_{OH} = 2.4\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



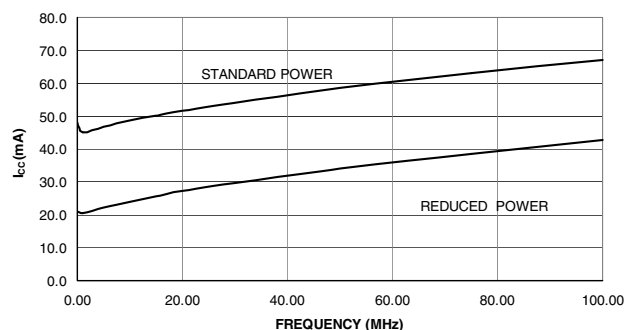
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
PIN-CONTROLLED POWER-DOWN MODE ( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



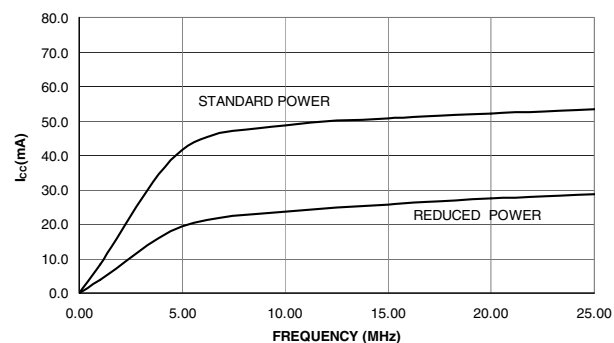
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
ASVL (LOW-POWER) VERSION ( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



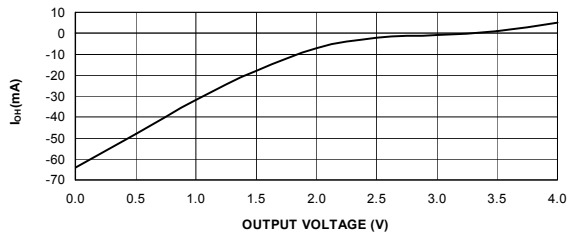
**SUPPLY CURRENT VS. FREQUENCY**  
ASV VERSION ( $T_A = 25^\circ\text{C}$ )



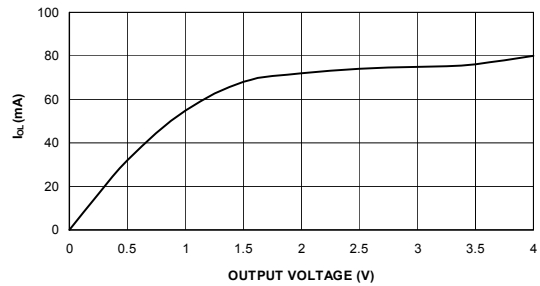
**SUPPLY CURRENT VS. FREQUENCY**  
ASVL (LOW POWER) VERSION ( $T_A = 25^\circ\text{C}$ )



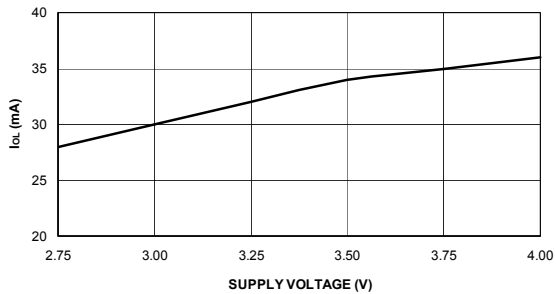
**OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE**  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



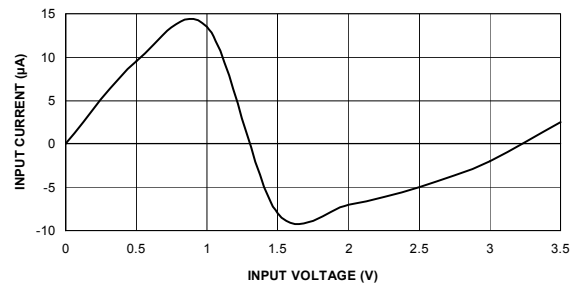
**OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE**  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



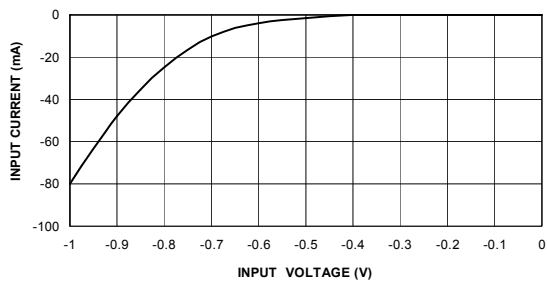
**OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE**  
( $V_{OL} = 0.5V$ ,  $T_A = 25^\circ C$ )



**INPUT CURRENT VS. INPUT VOLTAGE**  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



**INPUT CLAMP CURRENT VS. INPUT VOLTAGE**  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )





## 16. Ordering Information

### 16.1 Standard Package Options

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1502ASV-15AC44	44A	Commercial (0°C to 70°C)
			ATF1502ASV-15JC44	44J	
15	8	100	ATF1502ASV-15AI44	44A	Industrial (-40°C to +85°C)
			ATF1502ASV-15JI44	44J	
20	12	83.3	ATF1502ASV-20AC44	44A	Commercial (0°C to 70°C)
			ATF1502ASV-20JC44	44J	
20	12	83.3	ATF1502ASV-20AI44	44A	Industrial (-40°C to +85°C)
			ATF1502ASV-20JI44	44J	

- Notes:
1. The last-time buy date was September 30, 2005 for shaded parts.
  2. In 2004, Atmel briefly offered lead-free ATF1502ASV-15JJ44. This part is now discontinued and replaced by ATF1502ASV-15JU44, which is both lead- and Halide-free.

### 16.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1502ASV-15AU44	44A	Industrial (-40°C to +85°C)
			ATF1502ASV-15JU44	44J	

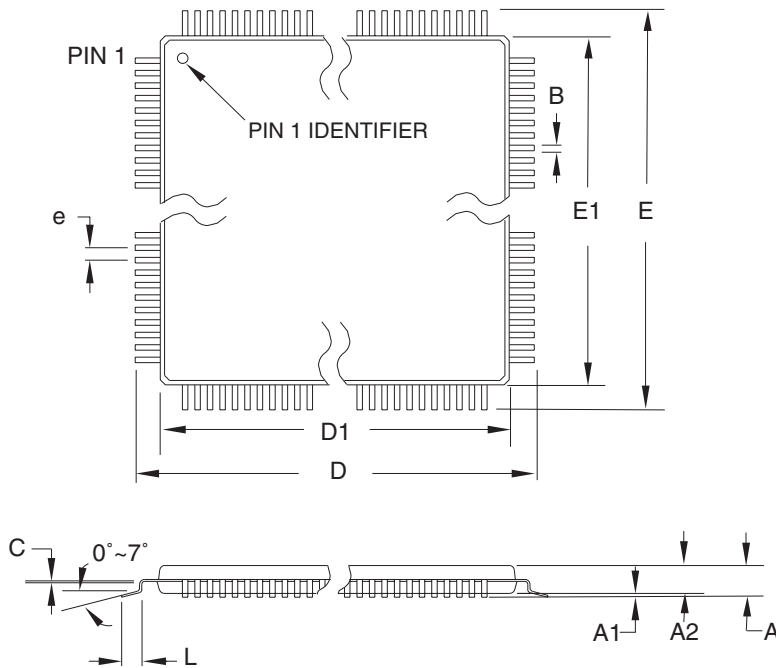
### 16.3 Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the  $V_{CC}$  conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate  $I_{CC}$  by 15%.

Package Type	
<b>44A</b>	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
<b>44J</b>	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)

## 17. Packaging Information

### 17.1 44A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



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#### TITLE

**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,  
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

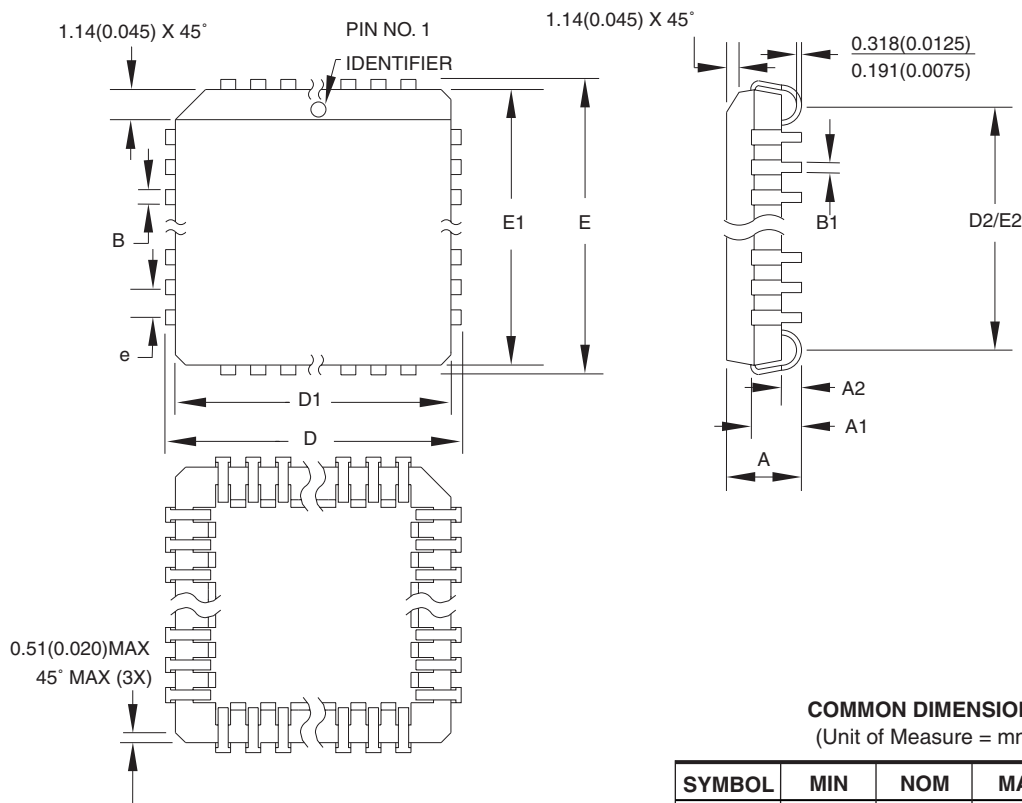
#### DRAWING NO.

44A

#### REV.

B

## 17.2 44J – PLCC



- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	17.399	—	17.653	
D1	16.510	—	16.662	Note 2
E	17.399	—	17.653	
E1	16.510	—	16.662	Note 2
D2/E2	14.986	—	16.002	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

**DRAWING NO.**

44J

**REV.**

B



### 17.3 Revision History

Version Number/Release Date	Comments
Revision I – June 2005	Added Green package options
Revision J – January 2006	Updated ATF1502ASV-15JC44 to last-time buy status



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