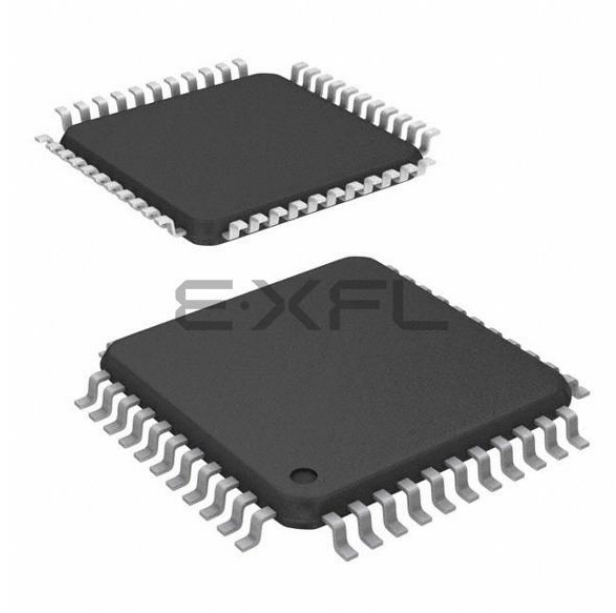

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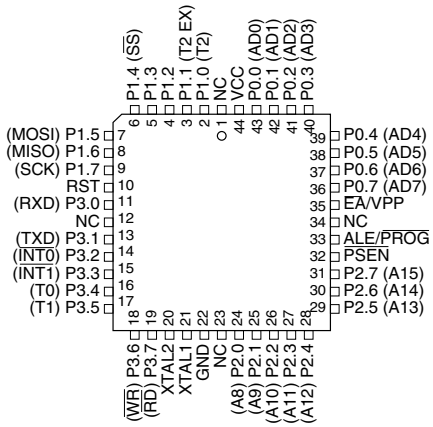
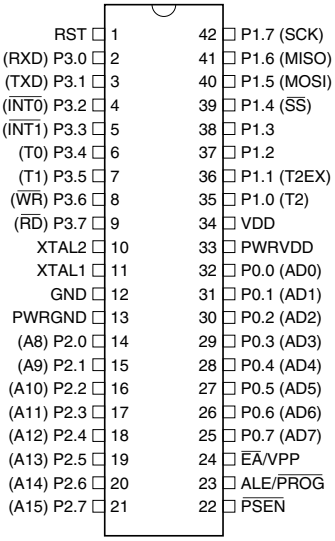
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s8253-24ac

2.3 44J – 44-lead PLCC



2.4 42PS6 – PDIP



3. Pin Description

3.1 VCC

Supply voltage (all packages except 42-PDIP).

3.2 GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program/data memories).

3.3 VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program/data memories.

3.4 PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **must** connect both VDD and PWRVDD to the board supply voltage.

5.1 Auxiliary Register

Table 5-2. AUXR – Auxiliary Register

AUXR Address = 8EH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	Intel_Pwd_Exit	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
Intel_Pwd_Exit	When set, this bit configures the interrupt driven exit from power-down to resume execution on the rising edge of the interrupt signal. When this bit is cleared, the execution resumes after a self-timed interval (nominal 2 ms) referenced from the falling edge of the interrupt signal.
DISALE	When DISALE = 0, ALE is emitted at a constant rate of 1/6 the oscillator frequency (except during MOVX when 1 ALE pulse is missing). When DISALE = 1, ALE is active only during a MOVX or MOVC instruction.

5.2 Clock Register

Table 5-3. CLKREG – Clock Register

CLKREG Address = 8FH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	X2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
X2	When X2 = 0, the oscillator frequency (at XTAL1 pin) is internally divided by 2 before it is used as the device system frequency. When X2 = 1, the divider by 2 is no longer used and the XTAL1 frequency becomes the device system frequency. This enables the user to choose a 6 MHz crystal instead of a 12 MHz crystal, for example, in order to reduce EMI.

5.3 SPI Registers

Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (see Table 14-1 on page 25) and SPSR (see Table 14-2 on page 26). The SPI data bits are contained in the SPDR register. In normal SPI mode, writing the SPI data register during serial data transfer sets the Write Collision bit (WCOL) in the SPSR register. In enhanced SPI mode, the SPDR is also write double-buffered because WCOL works as a Write Buffer Full Flag instead of being a collision flag. The values in SPDR are not changed by Reset.

5.4 Interrupt Registers

The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Four priorities can be set for each of the six interrupt sources in the IP and IPH registers.

IPH bits have the same functions as IP bits, except IPH has higher priority than IP. By using IPH in conjunction with IP, a priority level of 0, 1, 2, or 3 may be set for each interrupt.

5.5 Dual Data Pointer Registers

To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H - 83H and DP1 at 84H - 85H. Bit DPS = 0 in SFR EECON selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

5.6 Power Off Flag

The Power Off Flag (POF), located at bit_4 (PCON.4) in the PCON SFR. POF, is set to “1” during power up. It can be set and reset under software control and is not affected by RESET.

6. Data Memory – EEPROM and RAM

The AT89S8253 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access the SFR space.For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the EECON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to “0”.

During program execution mode (using the MOVX instruction) there is an auto-erase capability at the byte level. This means that the user can update or modify a single EEPROM byte location in real-time without affecting any other bytes.

The EEMWE bit in the EECON register needs to be set to “1” before any byte location in the EEPROM can be written. User software should reset EEMWE bit to “0” if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 4 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{\text{BSY}}$ bit (read-only) in SFR EECON. RDY/$\overline{\text{BSY}}$ = 0 means programming is still in progress and RDY/$\overline{\text{BSY}}$ = 1 means an EEPROM write cycle is completed and another write cycle can be initiated. Bit EELD in EECON controls whether the next MOVX instruction will only load the write buffer of the EEPROM or will actually start the programming cycle. By setting EELD, only load will occur. Before the last MOVX in a given page of 32 bytes, EELD should be cleared so that after the last MOVX the entire page will be programmed at the same time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming.

8. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) counts instruction cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K instruction cycles. The available timer periods are shown in Table 8-1. The WDT time-out period is dependent upon the external clock frequency.

The WDT is disabled by Power-on Reset and during Power-down mode. When WDT times out without being serviced or disabled, an internal RST pulse is generated to reset the CPU. See Table 8-1 for the WDT period selections.

Table 8-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period (Nominal for F_{CLK} = 12 MHz)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8253 operate the same way as Timer 0 and Timer 1 in the AT89S51 and AT89S52. For more detailed information on the Timer/Counter operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (see Table 10-2 on page 15). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-2.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 10-1. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Table 10-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

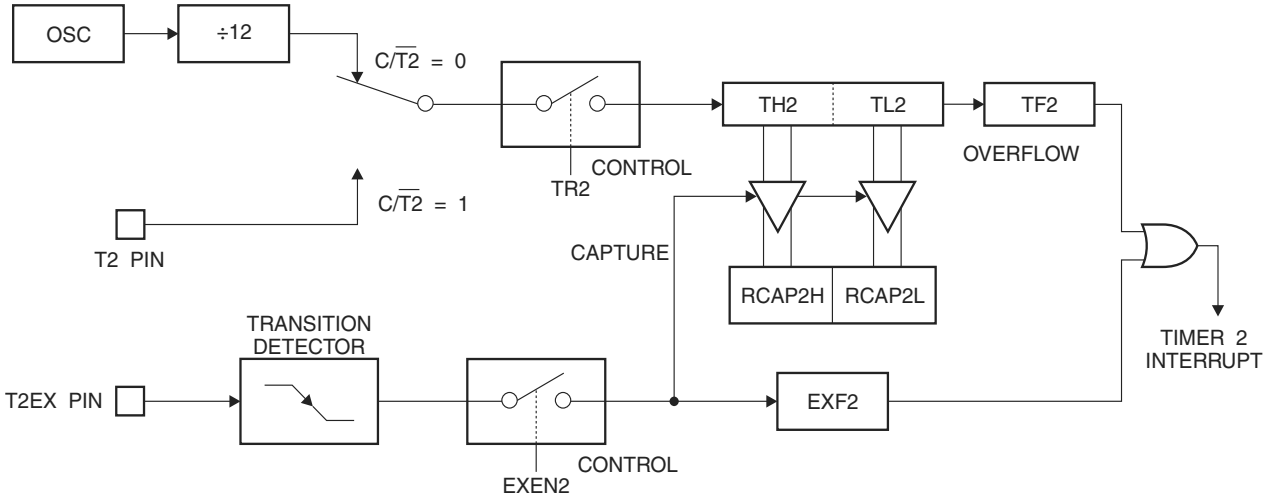
10.1 Timer 2 Registers

Control and status bits are contained in registers T2CON (see Table 10-2) and T2MOD (see Table 10-3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

10.2 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

Figure 10-1. Timer 2 in Capture Mode



10.3 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-3). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Table 10-3. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

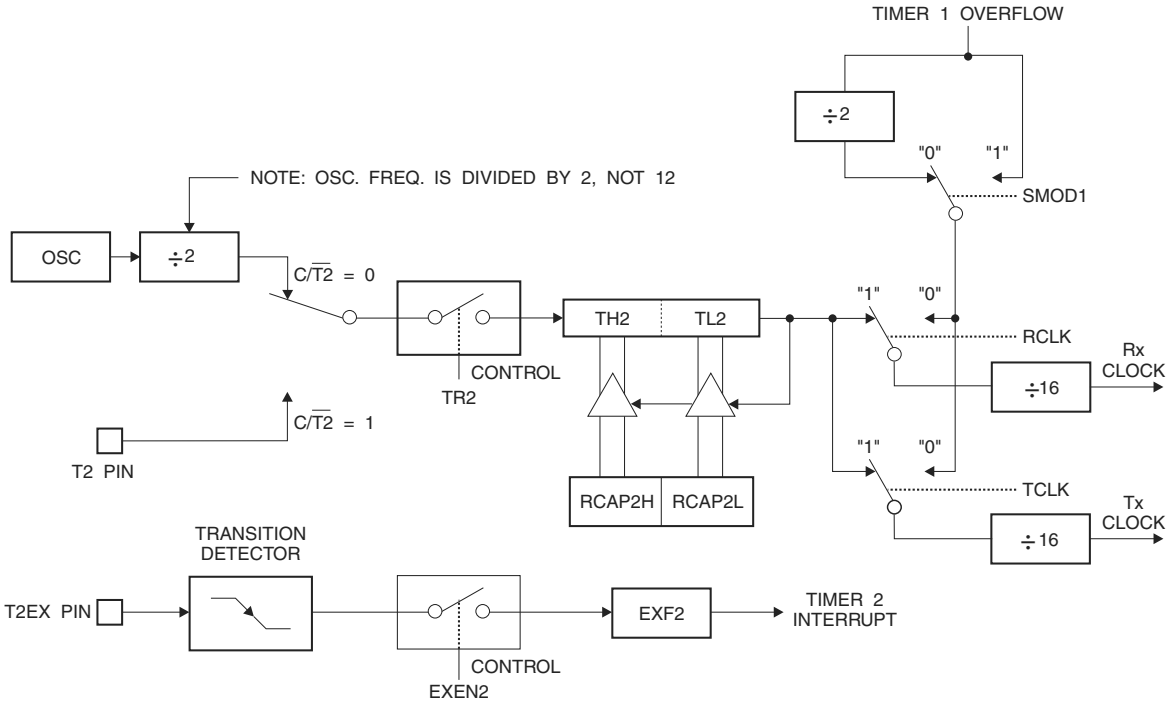
	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 10-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 10-3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit

Figure 10-4. Timer 2 in Baud Rate Generator Mode



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 10-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10-4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

13. UART

The UART in the AT89S8253 operates the same way as the UART in the AT89S51 and AT89S52. For more detailed information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

13.1 Enhanced UART

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

13.1.1 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1 SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1 SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2 SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the previous example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency.

14. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8253 and peripheral devices or between multiple AT89S8253 devices. The AT89S8253 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4 (f/2 if in x2 Clock Mode)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-Buffered Receive
- Double-Buffered Transmit (Enhanced Mode only)
- Wakeup from Idle Mode (Slave Mode only)

The interconnection between master and slave CPUs with SPI is shown in Figure 14-1. The four pins in the interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SCK), and Slave Select ($\overline{SS}$). The SCK pin is the clock output in master mode, but is the clock input in slave mode. The MSTR bit in SPCR determines the directions of MISO and MOSI. Also notice that MOSI connects to MOSI and MISO to MISO. In master mode, $\overline{SS}$/P1.4 is ignored and may be used as a general-purpose input or output. In slave mode, $\overline{SS}$ must be driven low to select an individual device as a slave. When $\overline{SS}$ is driven high, the slave's SPI port is deactivated and the MOSI/P1.5 pin can be used as a general-purpose input.

Figure 14-1. SPI Master-Slave Interconnection

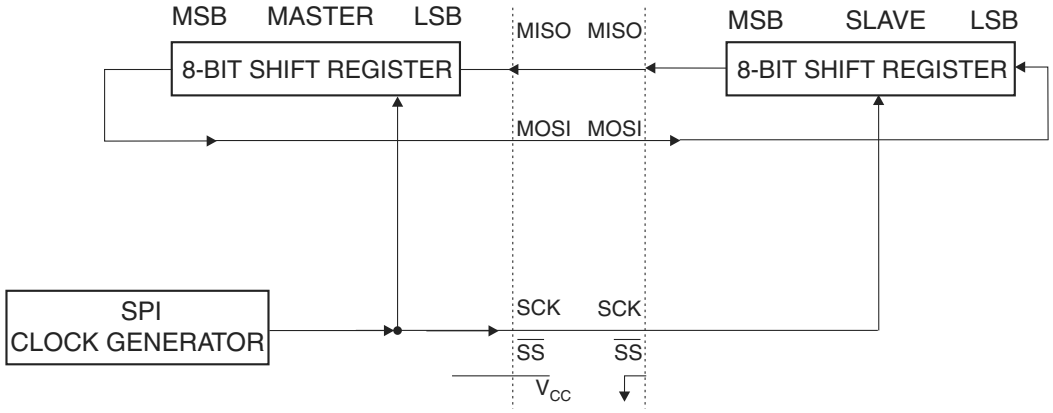
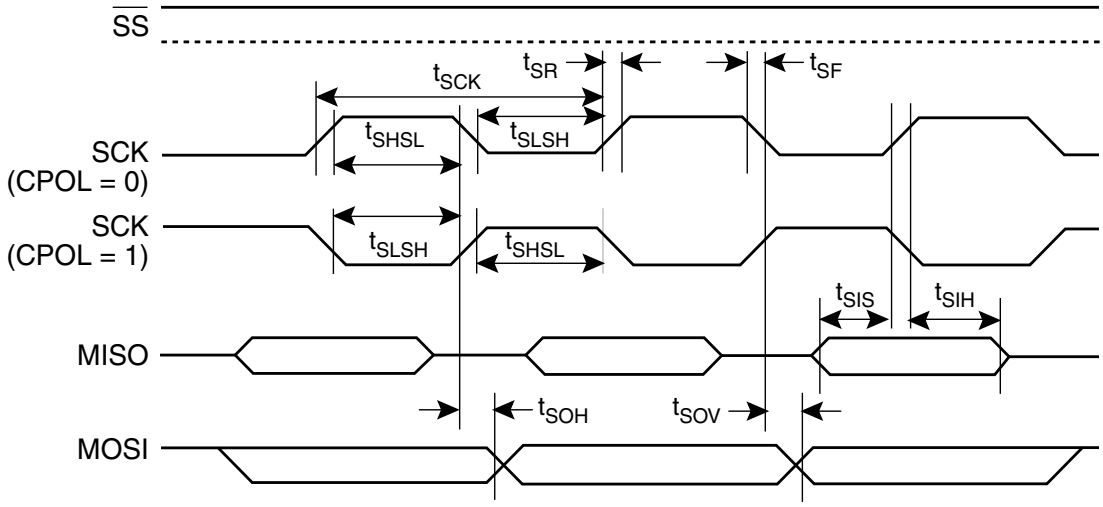


Table 14-5. SPI **Slave** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	1.5 t_{CLCL} - 25		ns
t_{SLSH}	Clock Low Time	1.5 t_{CLCL} - 25		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{SOE}	Output Enable Time		10	ns
t_{SOX}	Output Disable Time		25	ns
t_{SSE}	Slave Enable Lead Time	4 t_{CLCL} +50		ns
t_{SSD}	Slave Disable Lag Time	0		ns

Figure 14-4. SPI Master Timing (CPHA = 0)



Interrupt	Source	Vector Address
System Reset	RST or POR	0000H
External Interrupt 0	IE0	0003H
Timer 0 Overflow	TF0	000BH
External Interrupt 1	IE1	0013H
Timer 1 Overflow	TF1	001BH
Serial Port	RI or TI or SPIF	0023H

Table 15-1. Interrupt Enable (IE) Register

IE Address = A8H — Reset Value = 0X00 0000B

Bit Addressable

EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt, 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Table 15-2. IP – Interrupt Priority Register

IP = B8H — Reset Value = XX00 0000B

Bit Addressable

	–	–	PT2	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PT2	Timer 2 Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 15-3. IPH – Interrupt Priority High Register

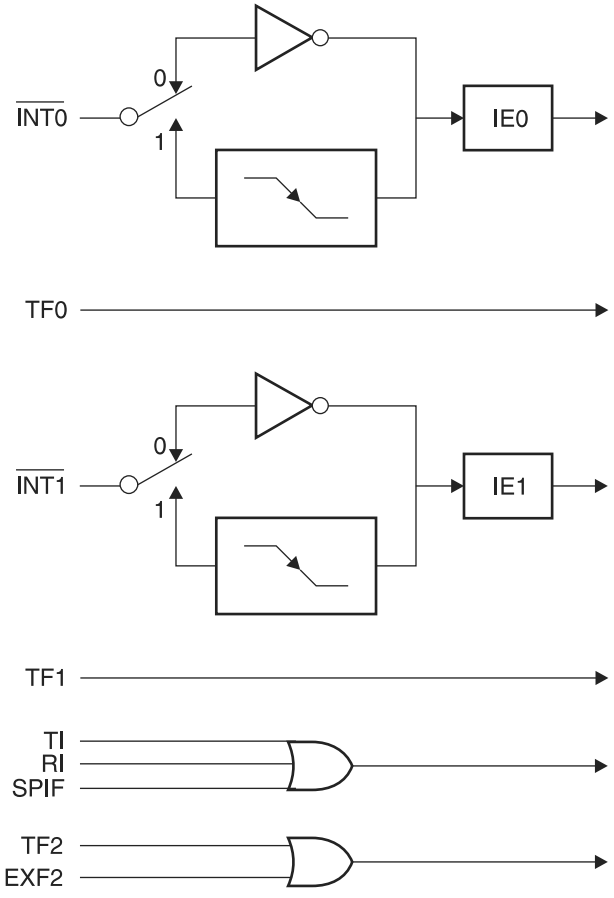
IPH = B7H — Reset Value = XX00 0000B

Not Bit Addressable

	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

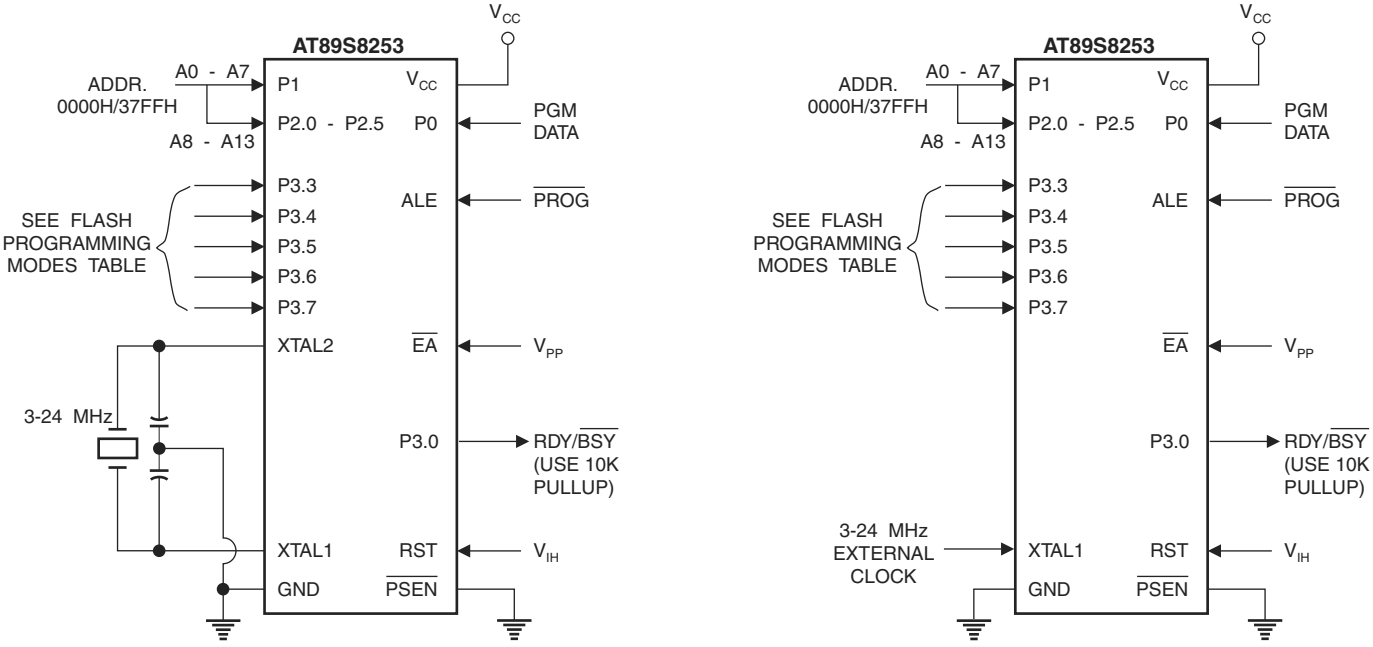
Symbol	Function
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

Figure 15-1. Interrupt Sources



Fuse3 (User Row Access Fuse): This fuse enables/disables writing to the programmable user row.
Fuse4 (Clock Selection Fuse): This fuse selects between an external clock source and a quartz crystal as the clock input.

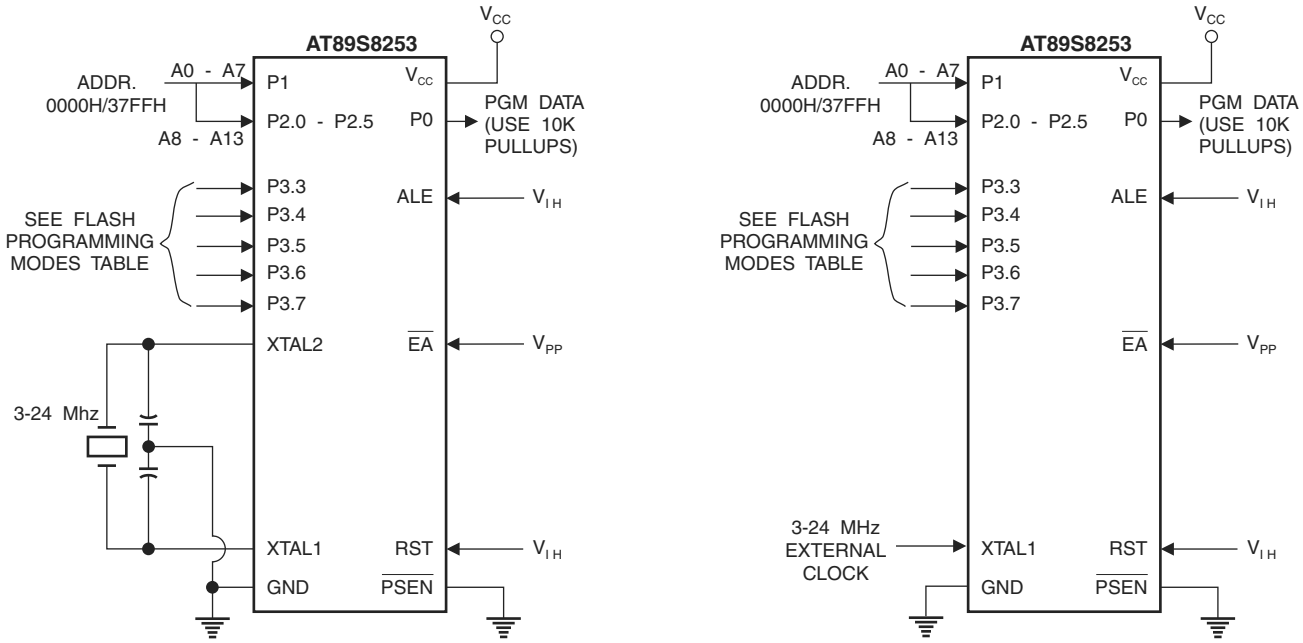
Programming the Flash/EEPROM Memory **(Parallel Mode)**



Oscillator Bypass Fuse (Fuse4) Off

Oscillator Bypass Fuse (Fuse4) On

Figure 25-2. Verifying the Flash/EEPROM Memory **(Parallel Mode)**



Oscillator Bypass Fuse (Fuse4) Off

Oscillator Bypass Fuse (Fuse4) On

29. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

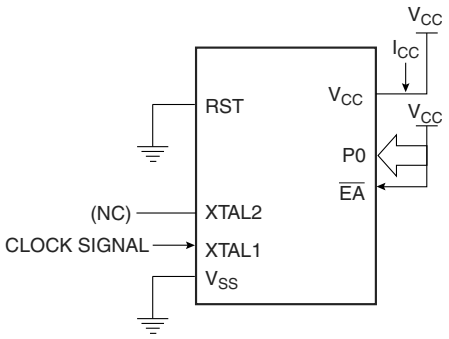
30. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted

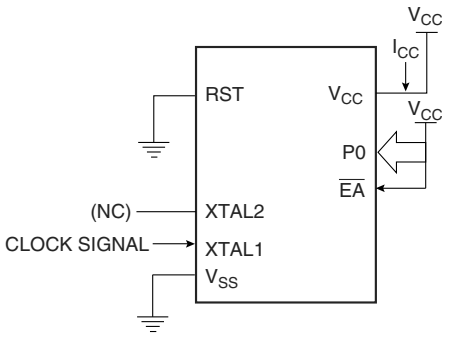
Symbol	Parameter	Condition	Min	Max
V_{IL}	Input Low-voltage	(Except $\overline{EA}$, XTAL1, RST, Port 0)	-0.5V	0.2 V_{CC} - 0.1V
V_{IL1}	Input Low-voltage	($\overline{EA}$, XTAL1, RST, Port 0)	-0.5V	0.3 V_{CC}
V_{IH}	Input High-voltage	(Except $\overline{EA}$, XTAL1, RST, Port 0)	0.5 V_{CC}	V_{CC} + 0.5V
V_{IH1}	Input High-voltage	($\overline{EA}$, XTAL1, RST, Port 0)	0.7 V_{CC}	V_{CC} + 0.5V
V_{OL}	Output Low-voltage[1]	I_{OL} = 10 mA, V_{CC} = 4.0V, T_A = 85°C		0.5V
V_{OH}	Output High-voltage When Weak Pull Ups are Enabled (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, T_A = 85°C	2.4V	
		I_{OH} = -25 µA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 µA, T_A = 85°C	0.9 V_{CC}	
V_{OH1}	Output High-voltage When Strong Pull Ups are Enabled (Port 0 in External Bus Mode, P1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -40 mA, T_A = 85°C	2.4V	
		I_{OH} = -25 mA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}	
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45V, V_{CC} = 5.5V, T_A = -40°C		-50 µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2V, V_{CC} = 5.5V, T_A = -40°C		-352 µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45V< V_{IN} < V_{CC}		±10 µA
RRST	Reset Pull-down Resistor		50 KΩ	150 KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10 pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		10 mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		3.5 mA
	Power-down Mode[2]	V_{CC} = 5.5V, T_A = -40°C		100 µA
		V_{CC} = 4.0V, T_A = -40°C		20 µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA,
   Maximum I_{OL} per 8-bit port:15 mA,
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

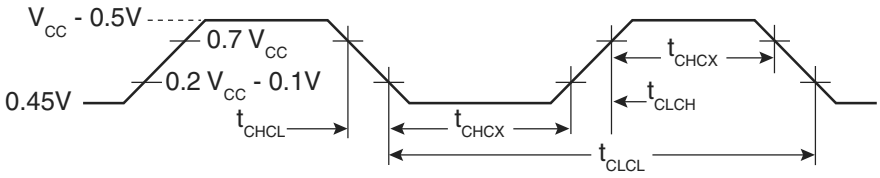
41. I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



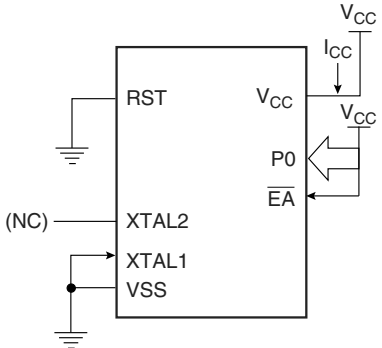
42. I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



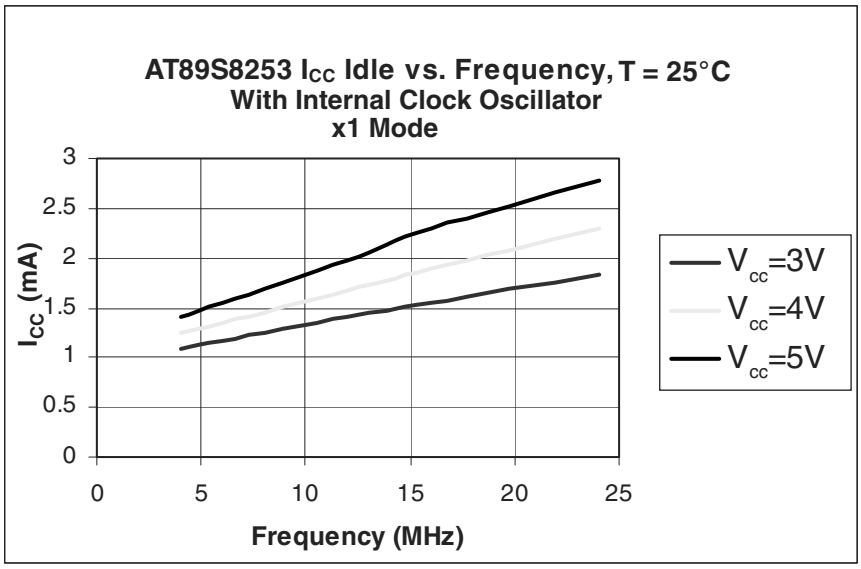
43. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



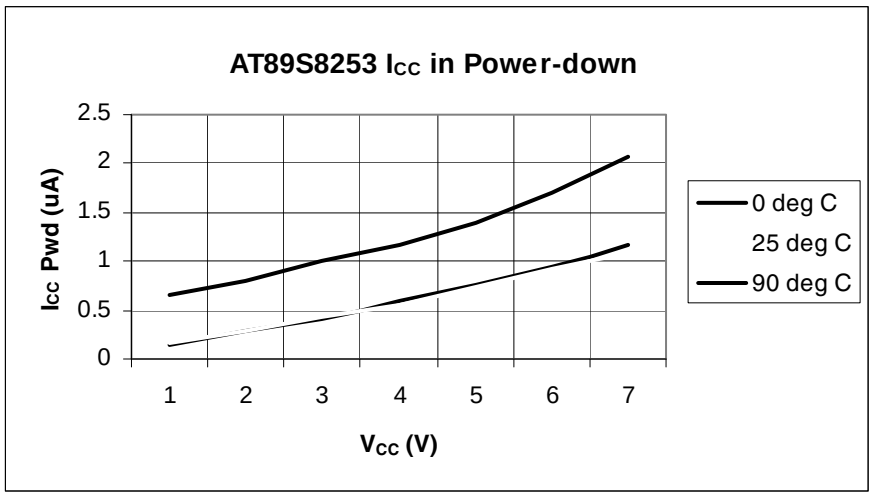
44. I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V



46. I_{CC} (Idle Mode) Measurements



47. I_{CC} (Power Down Mode) Measurements



48. Ordering Information

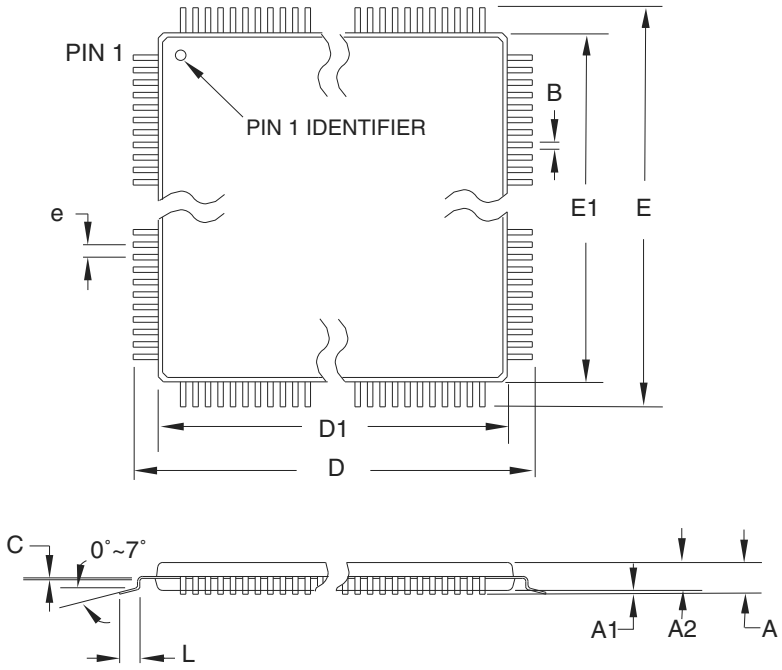
48.1 Green Package (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S8253-24AU AT89S8253-24JU AT89S8253-24PU AT89S8253-24PSU	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flat Package (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

49. Package Information

49.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B