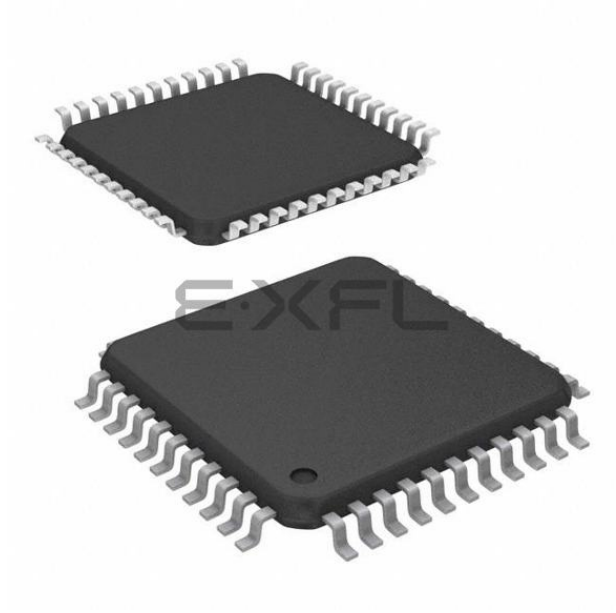

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s8253-24au

3.9 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source six TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL},150 µA typical) because of the weak internal pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8253, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)(1)
P3.3	$\overline{INT1}$ (external interrupt 1)(1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Note: 1. All pins in ports 1 and 2 and almost all pins in port 3 (the exceptions are P3.2 $\overline{INT0}$ and P3.3 $\overline{INT1}$) have their inputs disabled in the Power-down mode. Port pins P3.2 ($\overline{INT0}$) and P3.3 ($\overline{INT1}$) are active even in Power-down mode (to be able to sense an interrupt request to exit the Power-down mode) and as such still have their weak internal pull-ups turned on.

3.10 RST

Reset input. A high on this pin for at least two machine cycles while the oscillator is running resets the device.

3.11 ALE/$\overline{PROG}$

Address Latch Enable. ALE/$\overline{PROG}$ is an output pulse for latching the low byte of the address (on its falling edge) during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of the AUXR SFR at location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

3.12 $\overline{PSEN}$

Program Store Enable. $\overline{PSEN}$ is the read strobe to external program memory (active low).

When the AT89S8253 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

3.13 $\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

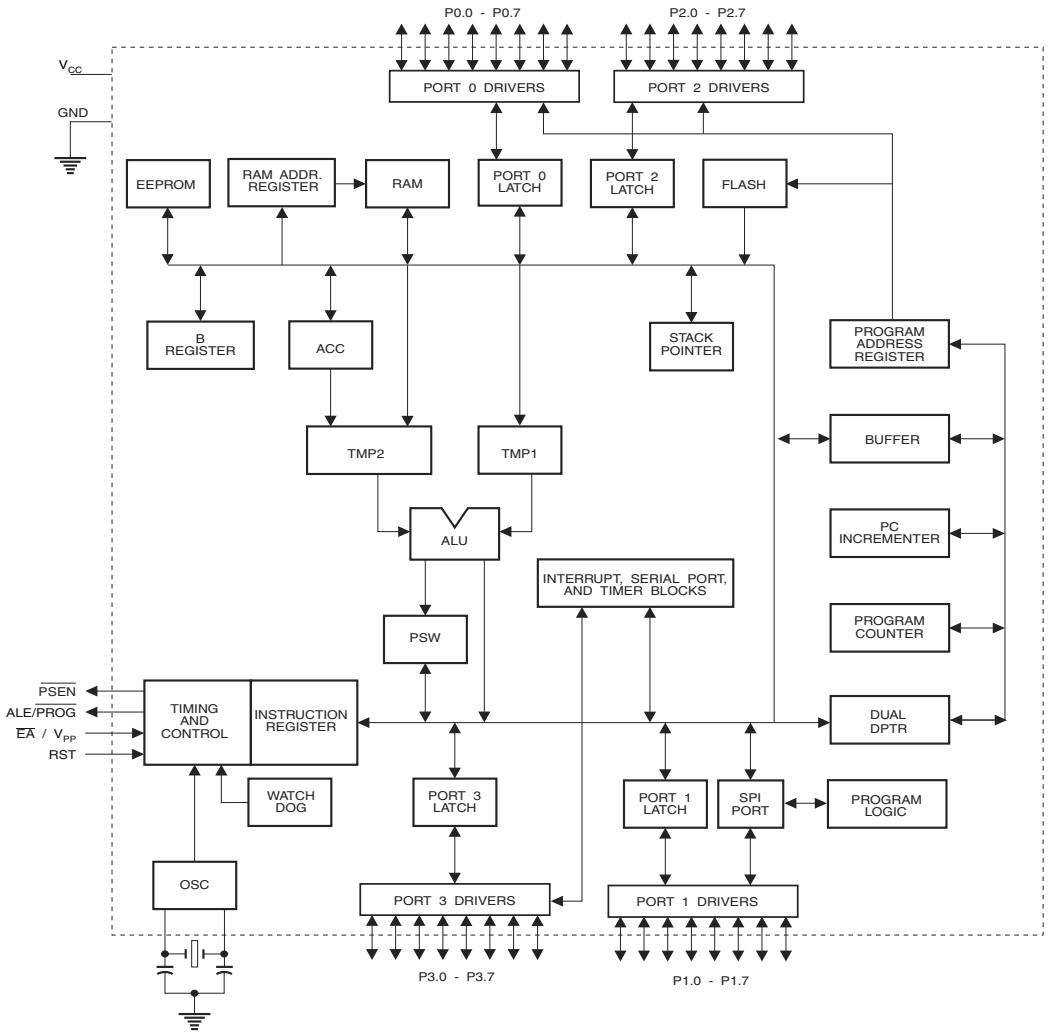
3.14 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

3.15 XTAL2

Output from the inverting oscillator amplifier. XTAL2 should not drive a board-level clock without a buffer.

4. Block Diagram



5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will generally return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 5-1. AT89S8253 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 00000100			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000	SADEN 00000000							0BFH
0B0H	P3 11111111							IPH XX000000	0B7H
0A8H	IE 0X000000	SADDR 00000000	SPSR 000XXX00						0AFH
0A0H	P2 11111111						WDTRST (Write Only)	WDTCON 0000 0000	0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						EECON XX000011		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXXXXXX0	CLKREG XXXXXXX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR ########	PCON 00XX0000	87H

Note: # means: 0 after cold reset and unchanged after warm reset.

5.1 Auxiliary Register

Table 5-2. AUXR – Auxiliary Register

AUXR Address = 8EH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	Intel_Pwd_Exit	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
Intel_Pwd_Exit	When set, this bit configures the interrupt driven exit from power-down to resume execution on the rising edge of the interrupt signal. When this bit is cleared, the execution resumes after a self-timed interval (nominal 2 ms) referenced from the falling edge of the interrupt signal.
DISALE	When DISALE = 0, ALE is emitted at a constant rate of 1/6 the oscillator frequency (except during MOVX when 1 ALE pulse is missing). When DISALE = 1, ALE is active only during a MOVX or MOVC instruction.

5.2 Clock Register

Table 5-3. CLKREG – Clock Register

CLKREG Address = 8FH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	X2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
X2	When X2 = 0, the oscillator frequency (at XTAL1 pin) is internally divided by 2 before it is used as the device system frequency. When X2 = 1, the divider by 2 is no longer used and the XTAL1 frequency becomes the device system frequency. This enables the user to choose a 6 MHz crystal instead of a 12 MHz crystal, for example, in order to reduce EMI.

5.3 SPI Registers

Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (see Table 14-1 on page 25) and SPSR (see Table 14-2 on page 26). The SPI data bits are contained in the SPDR register. In normal SPI mode, writing the SPI data register during serial data transfer sets the Write Collision bit (WCOL) in the SPSR register. In enhanced SPI mode, the SPDR is also write double-buffered because WCOL works as a Write Buffer Full Flag instead of being a collision flag. The values in SPDR are not changed by Reset.

5.4 Interrupt Registers

The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Four priorities can be set for each of the six interrupt sources in the IP and IPH registers.

IPH bits have the same functions as IP bits, except IPH has higher priority than IP. By using IPH in conjunction with IP, a priority level of 0, 1, 2, or 3 may be set for each interrupt.

8. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) counts instruction cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K instruction cycles. The available timer periods are shown in Table 8-1. The WDT time-out period is dependent upon the external clock frequency.

The WDT is disabled by Power-on Reset and during Power-down mode. When WDT times out without being serviced or disabled, an internal RST pulse is generated to reset the CPU. See Table 8-1 for the WDT period selections.

Table 8-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period (Nominal for F_{CLK} = 12 MHz)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Table 10-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

10.1 Timer 2 Registers

Control and status bits are contained in registers T2CON (see Table 10-2) and T2MOD (see Table 10-3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

10.2 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 10-2. Timer 2 in Auto Reload Mode (DCEN = 0)

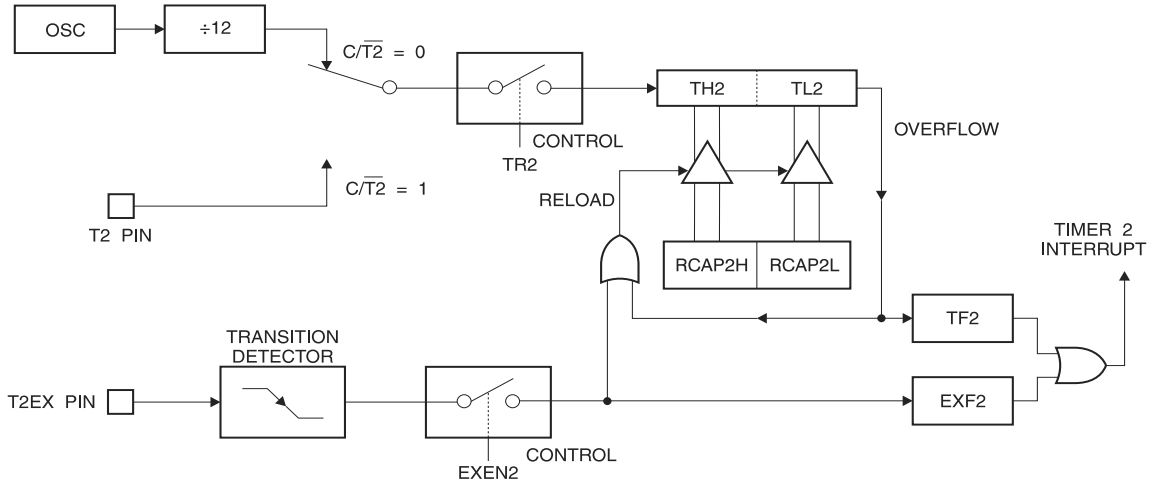
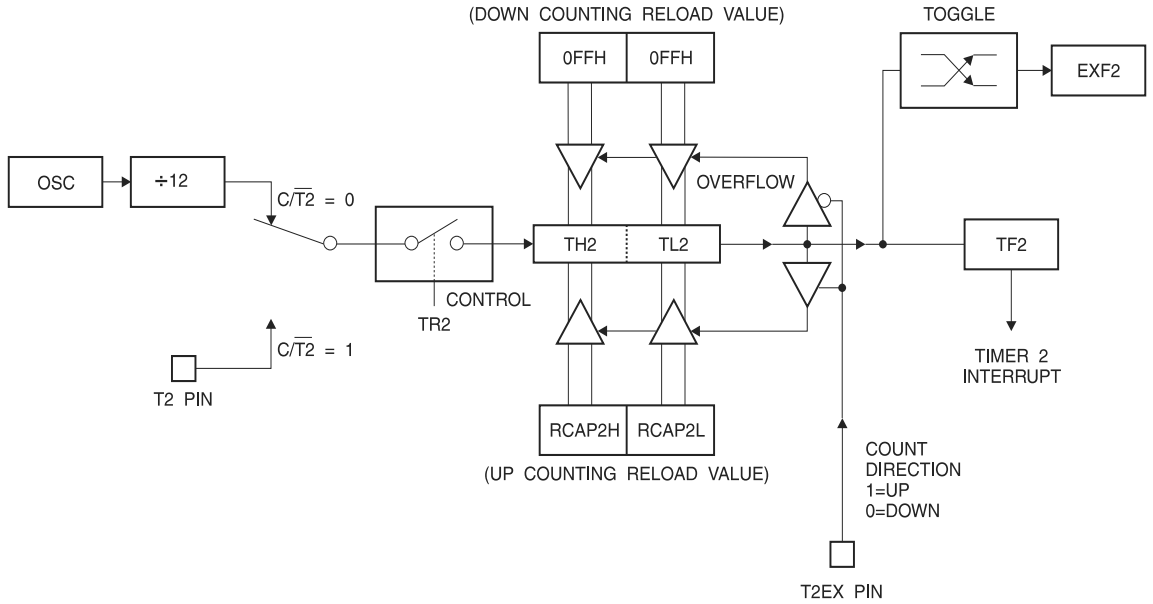


Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1 Timer 2 Auto Reload Mode (DCEN = 1)



Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency.

14. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8253 and peripheral devices or between multiple AT89S8253 devices. The AT89S8253 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4 (f/2 if in x2 Clock Mode)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-Buffered Receive
- Double-Buffered Transmit (Enhanced Mode only)
- Wakeup from Idle Mode (Slave Mode only)

The interconnection between master and slave CPUs with SPI is shown in Figure 14-1. The four pins in the interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SCK), and Slave Select ($\overline{SS}$). The SCK pin is the clock output in master mode, but is the clock input in slave mode. The MSTR bit in SPCR determines the directions of MISO and MOSI. Also notice that MOSI connects to MOSI and MISO to MISO. In master mode, $\overline{SS}$/P1.4 is ignored and may be used as a general-purpose input or output. In slave mode, $\overline{SS}$ must be driven low to select an individual device as a slave. When $\overline{SS}$ is driven high, the slave's SPI port is deactivated and the MOSI/P1.5 pin can be used as a general-purpose input.

Figure 14-1. SPI Master-Slave Interconnection

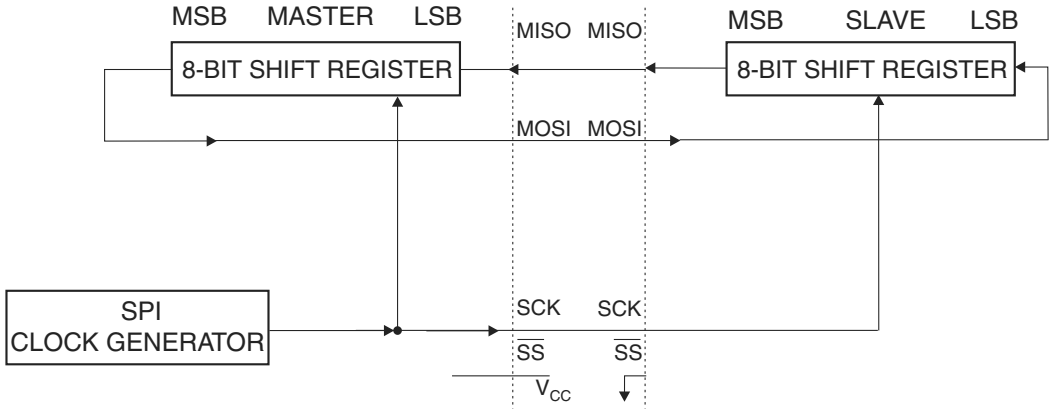
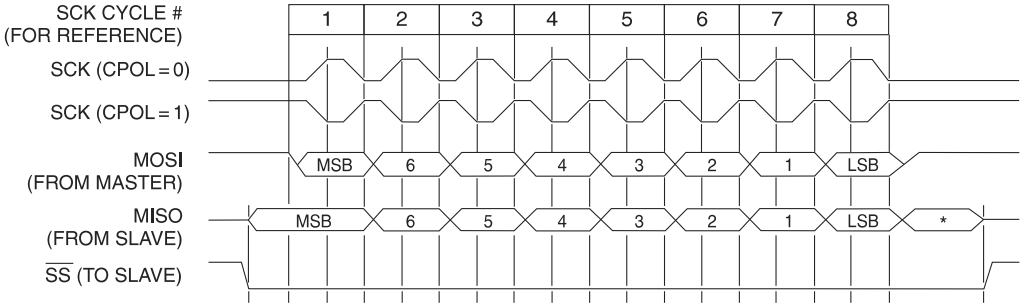
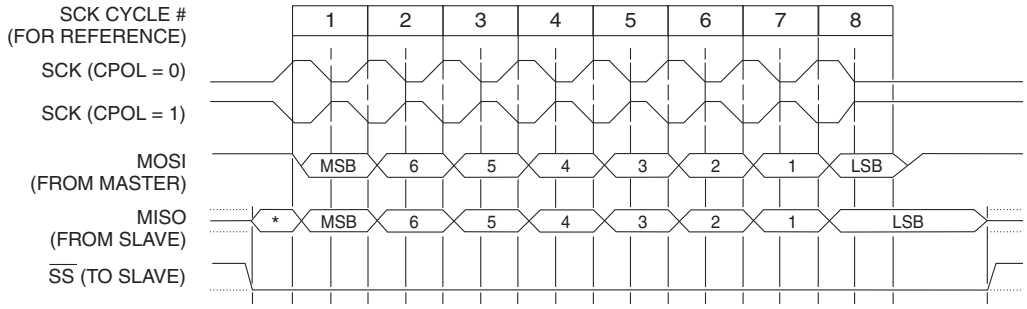


Figure 14-8. SPI Transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 14-9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character

15. Interrupts

The AT89S8253 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 15-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 15-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The serial interrupt is the logical OR of bits RI and TI in register SCON and also bit SPIF in SPSR (if SPIE in SPCR is set). None of these flags is cleared by hardware when the service routine is vectored to. The service routine may have to determine whether the UART or SPI generated the interrupt.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 15-3. IPH – Interrupt Priority High Register

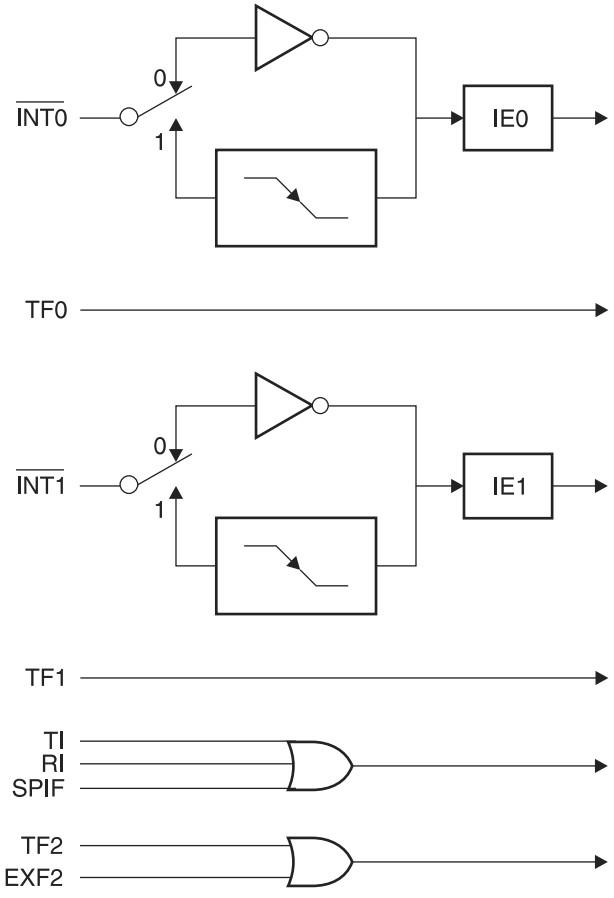
IPH = B7H — Reset Value = XX00 0000B

Not Bit Addressable

	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

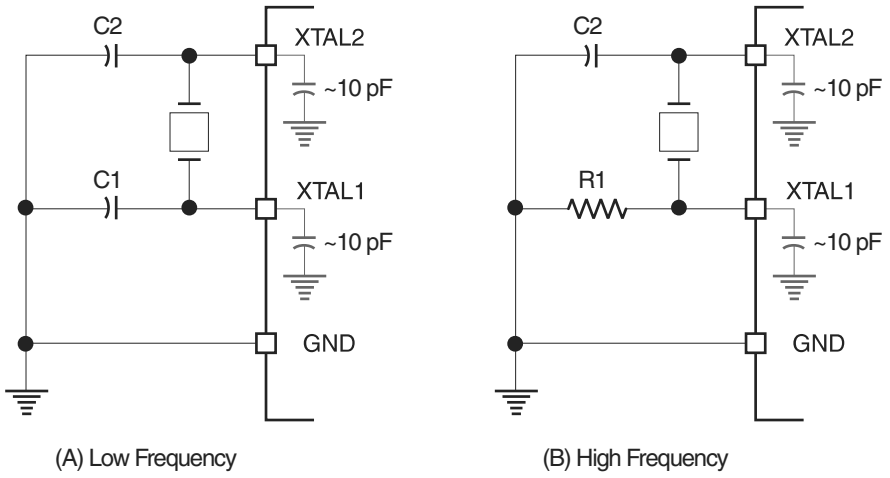
Figure 15-1. Interrupt Sources



16. Oscillator Characteristics

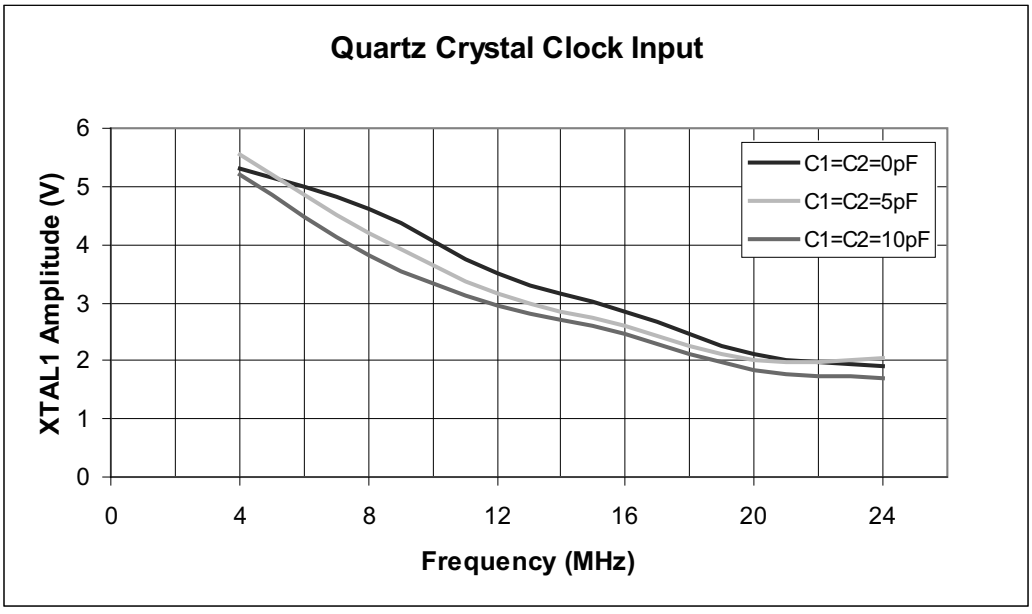
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1 (A) and (B). Either a quartz crystal or ceramic resonator may be used. For frequencies above 16MHz it is recommended that C1 be replaced with R1 for improved startup performance. Note that the internal structure of the devices adds about 10 pF of capacitance to both XTAL1 and XTAL2. The total capacitance on XTAL1 or XTAL2, including the external load capacitor (C1/C2) plus internal device load, board trace and crystal loadings, should not exceed 20 pF. Figure 16-2, 16-3, 16-4 and 16-5 illustrate the relationship between clock loading and the respective resulting clock amplitudes.

Figure 16-1. Oscillator Connections



Note: C1, C2 = 0–10 pF for Crystals
= 0–10 pF for Ceramic Resonators
R1 = 4–5 MΩ

Figure 16-2. Quartz Crystal Clock Source (A)



26. Flash Programming and Verification Characteristics – Parallel Mode

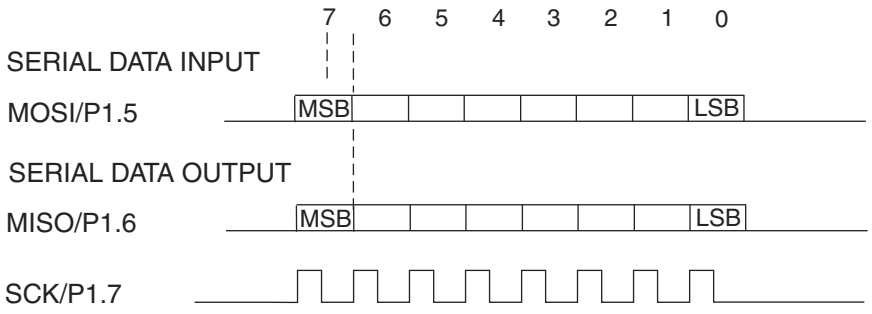
T_A = 20°C to 30°C, V_{CC} = 4.0V to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{PWRUP}	Power On to RST High (1)	10		µs
t_{RHX}	RST High to XTAL Start	10		µs
t_{OSTL}	Oscillator Settling Time	10		ms
t_{HSTL}	High Voltage Settling Time	10		µs
t_{MSTP}	Mode Setup to $\overline{PROG}$ Low	1		µs
t_{ASTP}	Address Setup to $\overline{PROG}$ Low	1		µs
t_{DSTP}	Data Setup to $\overline{PROG}$ Low	1		µs
t_{PGW}	$\overline{PROG}$ Width	1		µs
t_{AHLD}	Address Hold after $\overline{PROG}$	1		µs
t_{DHLD}	Data Hold after $\overline{PROG}$	1		µs
t_{BLT}	Byte Load Period	1	150	µs
t_{PHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		256	µs
t_{WC}	Write Cycle Time(2)		4.5	ms
t_{MHLD}	Mode Hold After $\overline{BUSY}$ Low	10		µs
t_{VFY}	Address to Data Verify Valid		1	µs
t_{PSTP}	$\overline{PROG}$ Setup to V_{PP} High	10		µs
t_{PHLD}	$\overline{PROG}$ Hold after V_{PP} Low	10		µs
t_{PLX}	$\overline{PROG}$ Low to XTAL Halt	1		µs
t_{XRL}	XTAL Halt to RST Low	1		µs
t_{PWRDN}	RST Low to Power Off	1		µs

Notes: 1. Power On occurs once V_{CC} reaches 2.4V.

2. 9 ms if Chip Erase.

27. Serial Downloading Waveforms (SPI Mode 1 → CPOL = 0, CPHA = 1)



28. Serial Programming Characteristics

Figure 28-1. Serial Programming Timing

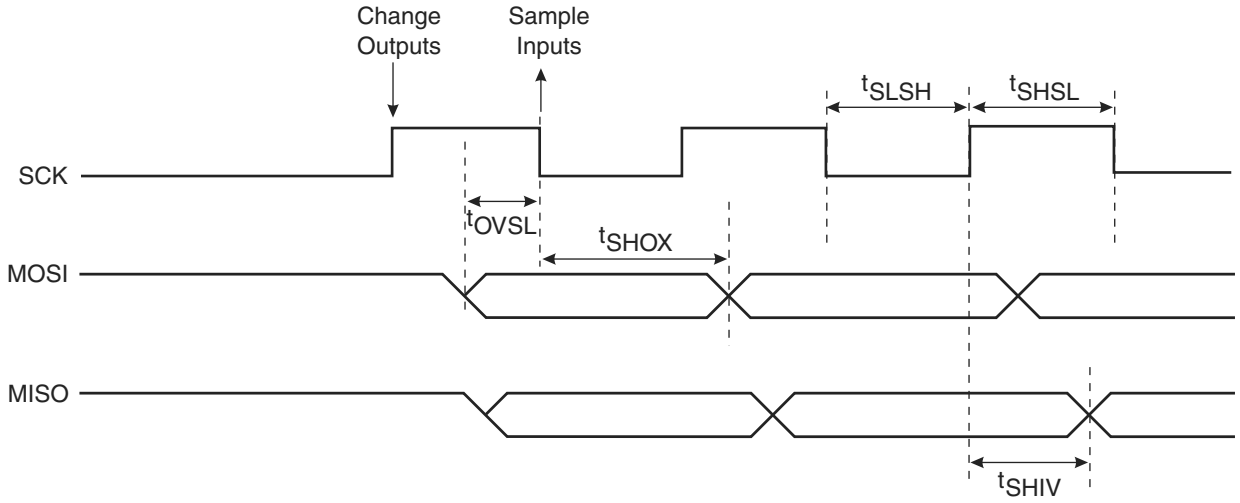


Table 28-1. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 2.7V - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		24	MHz
t_{CLCL}	Oscillator Period	41.6		33.3	ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSL}	MOSI Setup to SCK Low	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK Low	2 t_{CLCL}			ns
t_{SHIV}	SCK High to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			9	ms
t_{SWC}	Serial Page Write Cycle Time			4.5	ms

31. AC Characteristics

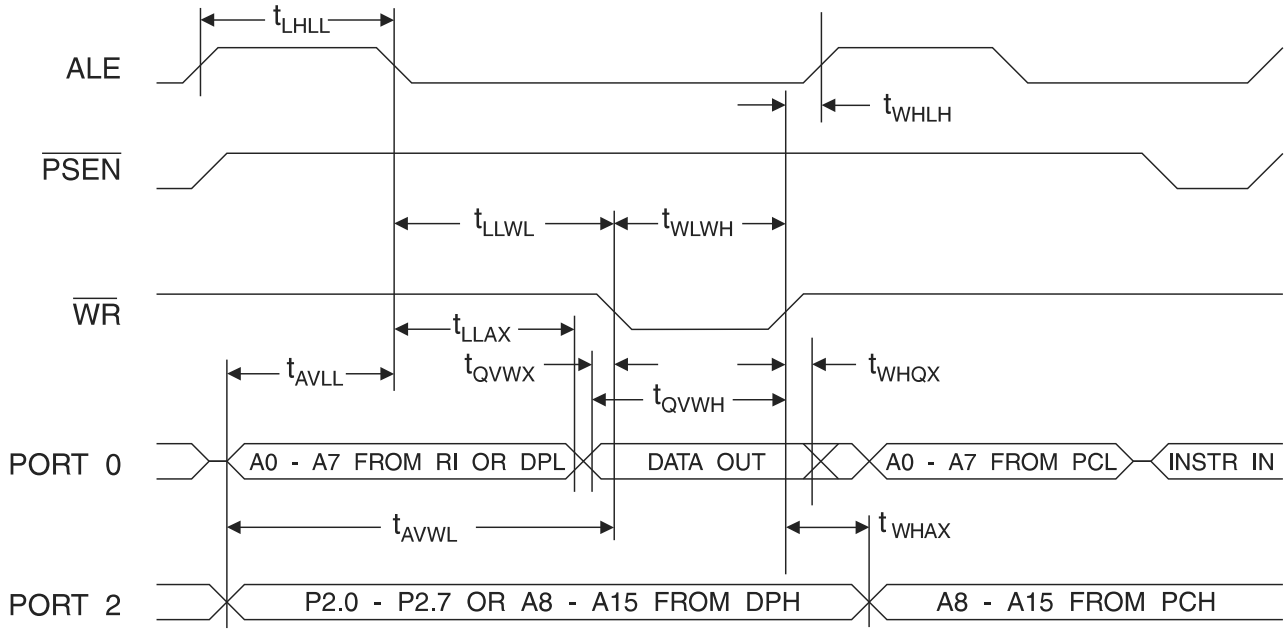
The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted.

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

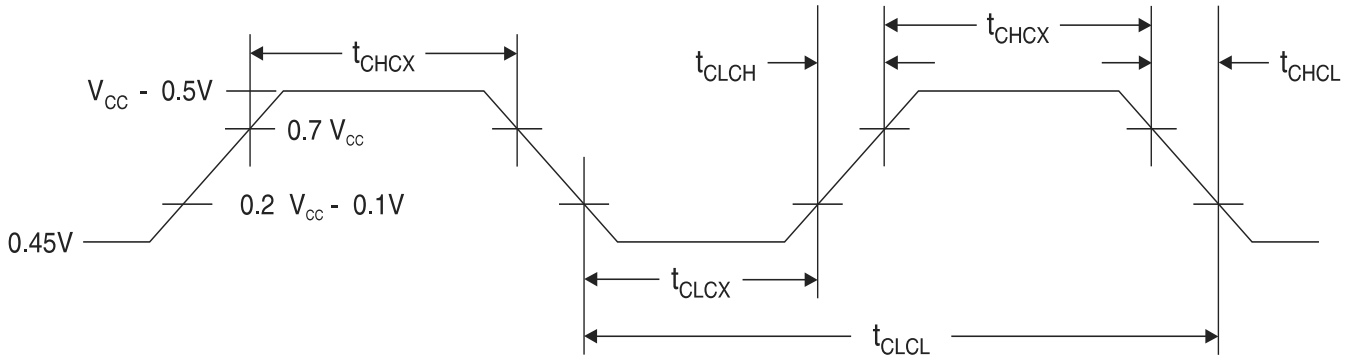
31.1 External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 12		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 12		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 16		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 50	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 12		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 12		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 50	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	-10		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 20	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 4		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 50	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		20	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 50	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 20	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 50	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 50	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 24	$3t_{CLCL}$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 12		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	$2t_{CLCL}$ - 24		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$8t_{CLCL}$ - 24		ns
t_{WHQX}	Data Hold after $\overline{WR}$	$2t_{CLCL}$ - 24		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 10	t_{CLCL} + 20	ns
t_{WHAX}	Address Hold after $\overline{RD}$ or $\overline{WR}$ High	t_{CLCL} - 10		ns

34. External Data Memory Write Cycle



35. External Clock Drive Waveforms



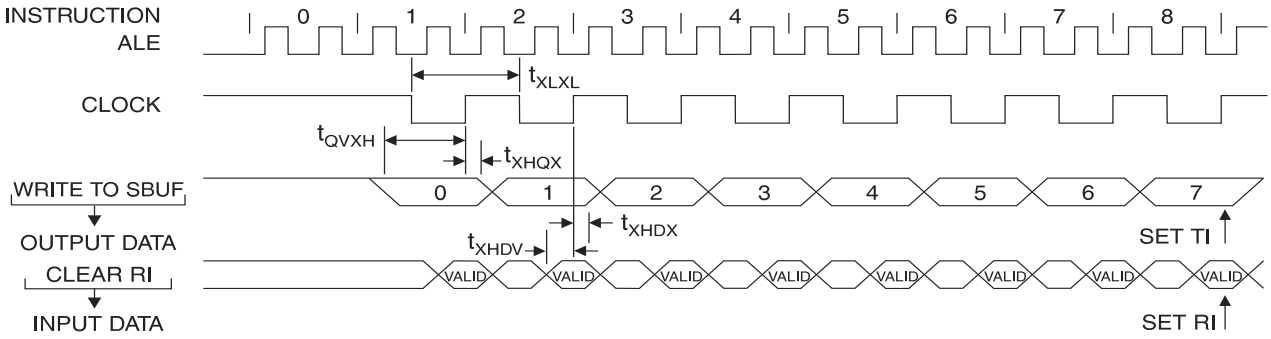
36. External Clock Drive

Symbol	Parameter	V_{CC} = 2.7V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

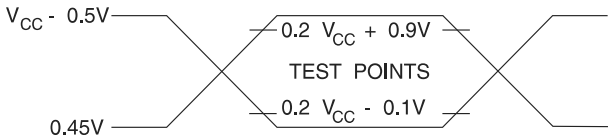
37. Serial Port Timing: Shift Register Mode Test Conditions

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	

38. Shift Register Mode Timing Waveforms

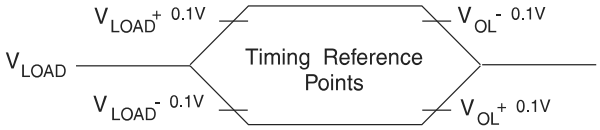


39. AC Testing Input/Output Waveforms(1)

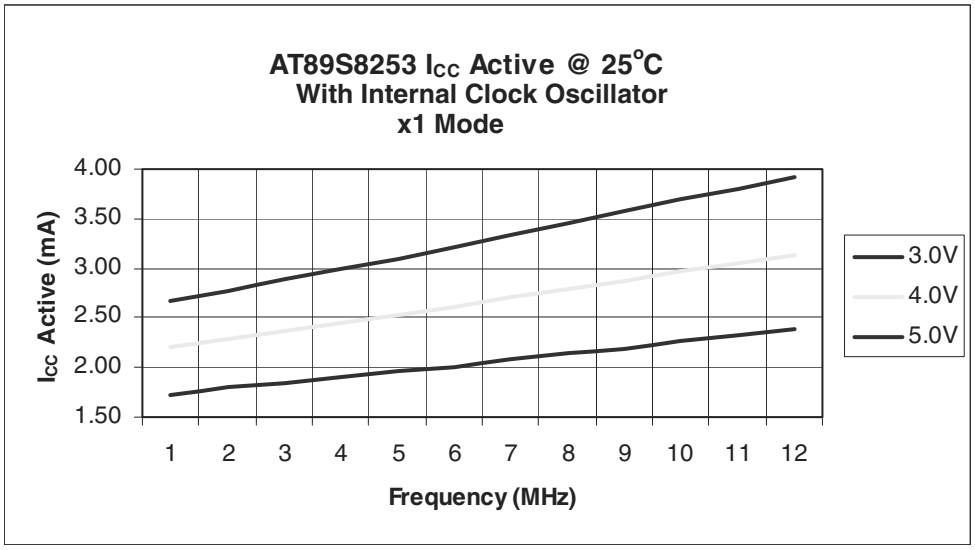


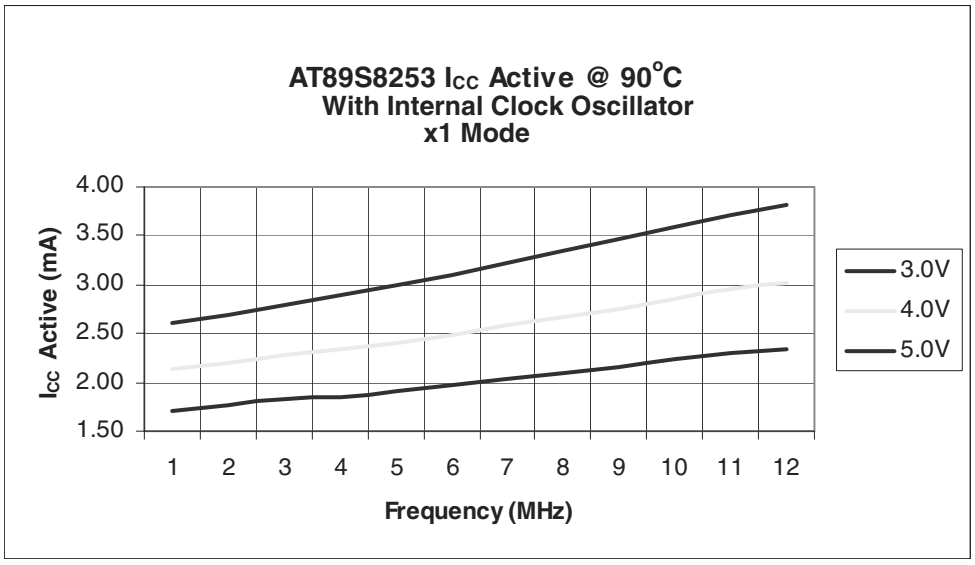
Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

40. Float Waveforms(1)

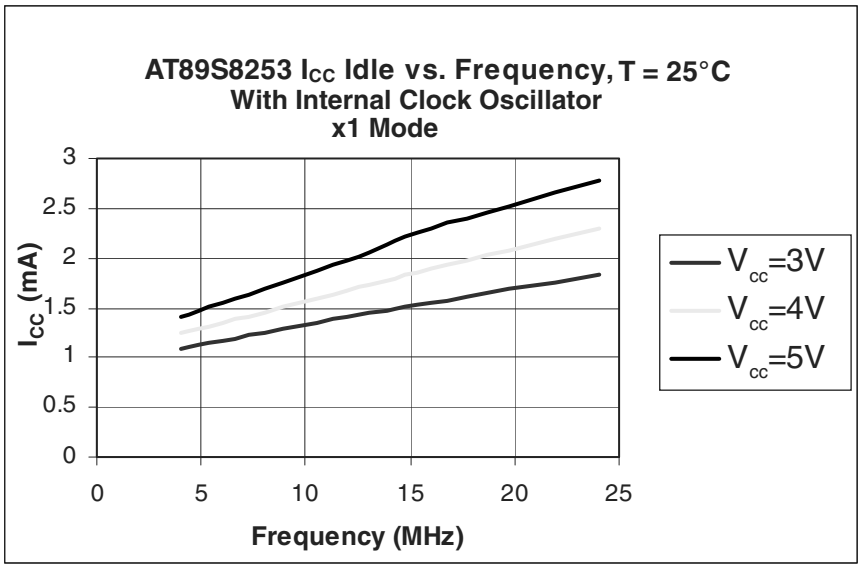


45. I_{CC} (Active Mode) Measurements

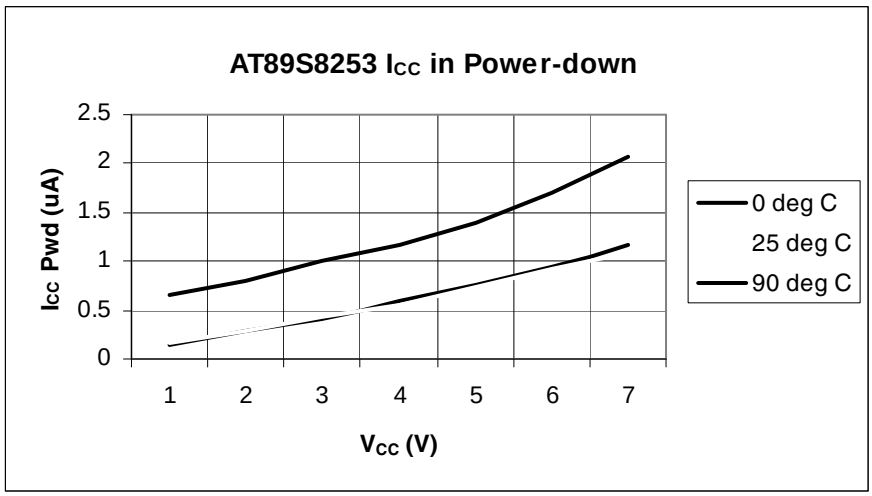




46. I_{CC} (Idle Mode) Measurements



47. I_{CC} (Power Down Mode) Measurements



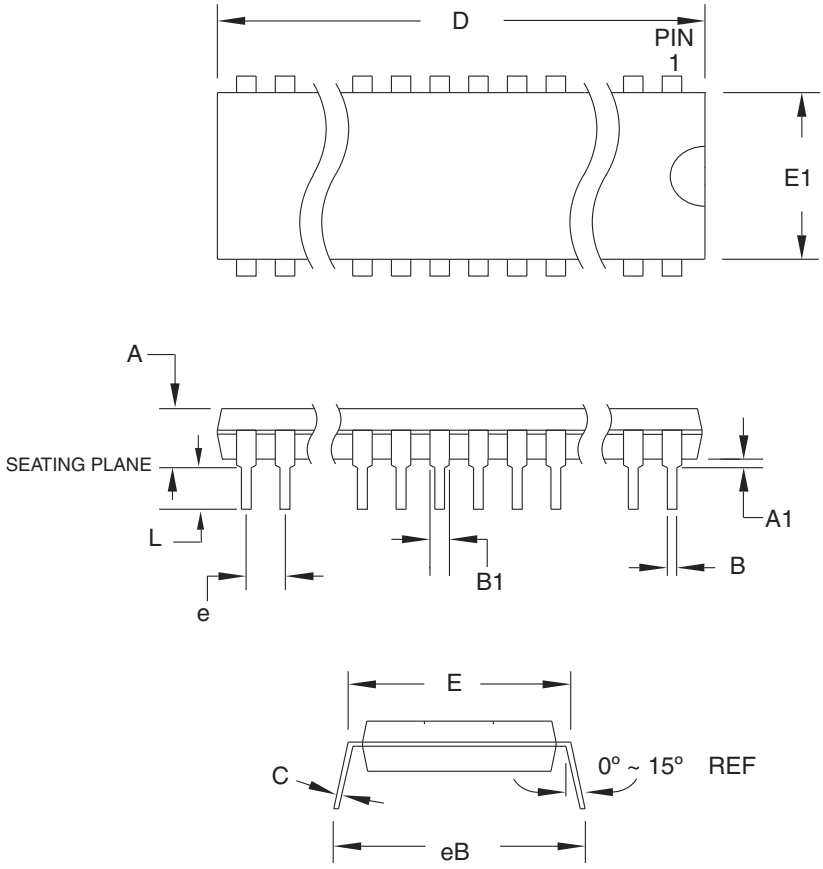
48. Ordering Information

48.1 Green Package (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S8253-24AU AT89S8253-24JU AT89S8253-24PU AT89S8253-24PSU	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flat Package (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

49.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B