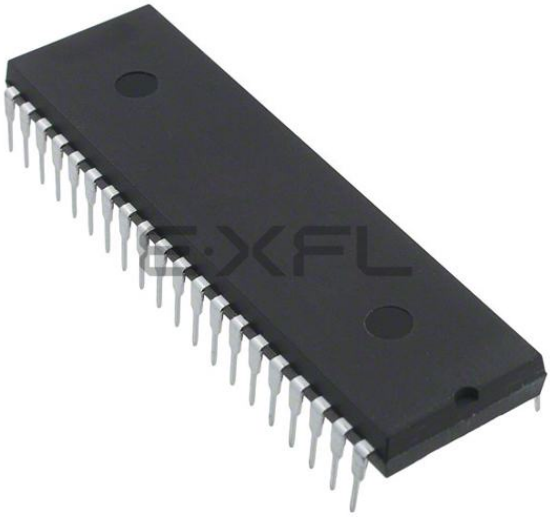

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s8253-24pu

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will generally return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 5-1. AT89S8253 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 00000100			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000	SADEN 00000000							0BFH
0B0H	P3 11111111							IPH XX000000	0B7H
0A8H	IE 0X000000	SADDR 00000000	SPSR 000XXX00						0AFH
0A0H	P2 11111111						WDTRST (Write Only)	WDTCON 0000 0000	0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						EECON XX000011		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXXXXXX0	CLKREG XXXXXXX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR ########	PCON 00XX0000	87H

Note: # means: 0 after cold reset and unchanged after warm reset.

5.1 Auxiliary Register

Table 5-2. AUXR – Auxiliary Register

AUXR Address = 8EH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	Intel_Pwd_Exit	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
Intel_Pwd_Exit	When set, this bit configures the interrupt driven exit from power-down to resume execution on the rising edge of the interrupt signal. When this bit is cleared, the execution resumes after a self-timed interval (nominal 2 ms) referenced from the falling edge of the interrupt signal.
DISALE	When DISALE = 0, ALE is emitted at a constant rate of 1/6 the oscillator frequency (except during MOVX when 1 ALE pulse is missing). When DISALE = 1, ALE is active only during a MOVX or MOVC instruction.

5.2 Clock Register

Table 5-3. CLKREG – Clock Register

CLKREG Address = 8FH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	X2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
X2	When X2 = 0, the oscillator frequency (at XTAL1 pin) is internally divided by 2 before it is used as the device system frequency. When X2 = 1, the divider by 2 is no longer used and the XTAL1 frequency becomes the device system frequency. This enables the user to choose a 6 MHz crystal instead of a 12 MHz crystal, for example, in order to reduce EMI.

5.3 SPI Registers

Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (see Table 14-1 on page 25) and SPSR (see Table 14-2 on page 26). The SPI data bits are contained in the SPDR register. In normal SPI mode, writing the SPI data register during serial data transfer sets the Write Collision bit (WCOL) in the SPSR register. In enhanced SPI mode, the SPDR is also write double-buffered because WCOL works as a Write Buffer Full Flag instead of being a collision flag. The values in SPDR are not changed by Reset.

5.4 Interrupt Registers

The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Four priorities can be set for each of the six interrupt sources in the IP and IPH registers.

IPH bits have the same functions as IP bits, except IPH has higher priority than IP. By using IPH in conjunction with IP, a priority level of 0, 1, 2, or 3 may be set for each interrupt.

5.5 Dual Data Pointer Registers

To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H - 83H and DP1 at 84H - 85H. Bit DPS = 0 in SFR EECON selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

5.6 Power Off Flag

The Power Off Flag (POF), located at bit_4 (PCON.4) in the PCON SFR. POF, is set to “1” during power up. It can be set and reset under software control and is not affected by RESET.

6. Data Memory – EEPROM and RAM

The AT89S8253 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access the SFR space.For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the EECON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to “0”.

During program execution mode (using the MOVX instruction) there is an auto-erase capability at the byte level. This means that the user can update or modify a single EEPROM byte location in real-time without affecting any other bytes.

The EEMWE bit in the EECON register needs to be set to “1” before any byte location in the EEPROM can be written. User software should reset EEMWE bit to “0” if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 4 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{\text{BSY}}$ bit (read-only) in SFR EECON. RDY/$\overline{\text{BSY}}$ = 0 means programming is still in progress and RDY/$\overline{\text{BSY}}$ = 1 means an EEPROM write cycle is completed and another write cycle can be initiated. Bit EELD in EECON controls whether the next MOVX instruction will only load the write buffer of the EEPROM or will actually start the programming cycle. By setting EELD, only load will occur. Before the last MOVX in a given page of 32 bytes, EELD should be cleared so that after the last MOVX the entire page will be programmed at the same time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

6.1 Memory Control Register

The EECON register contains control bits for the 2K bytes of on-chip data EEPROM. It also contains the control bit for the dual data pointer.

Table 6-1. EECON – Data EEPROM Control Register

EECON Address = 96H — Reset Value = XX00 0011B

Not Bit Addressable

Bit	–	–	EELD	EEMWE	EEMEN	DPS	RDY/$\overline{BSY}$	$\overline{WRTINH}$
	7	6	5	4	3	2	1	0

Symbol	Function
EELD	EEPROM data memory load enable bit. Used to implement Page Mode Write. A MOVX instruction writing into the data EEPROM will not initiate the programming cycle if this bit is set, rather it will just load data into the volatile data buffer of the data EEPROM memory. Before the last MOVX, reset this bit and the data EEPROM will program all the bytes previously loaded on the same page of the address given by the last MOVX instruction.
EEMWE	EEPROM data memory write enable bit. Set this bit to 1 before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to 0 after EEPROM write is completed.
EEMEN	Internal EEPROM access enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory if the address used is less than 2K. When EEMEN = 0 or the address used is ≥ 2K, MOVX with DPTR accesses external data memory.
DPS	Data pointer register select. DPS = 0 selects the first bank of data pointer register, DP0, and DPS = 1 selects the second bank, DP1.
RDY/$\overline{BSY}$	RDY/$\overline{BSY}$ (Ready/$\overline{Busy}$) flag for the data EEPROM memory. This is a read-only bit which is cleared by hardware during the programming cycle of the on-chip EEPROM. It is also set by hardware when the programming is completed. Note that RDY/$\overline{BSY}$ will be cleared long after the completion of the MOVX instruction which has initiated the programming cycle.
$\overline{WRTINH}$	$\overline{WRTINH}$ (Write Inhibit) is a READ-ONLY bit which is cleared by hardware when V_{cc} is too low for the programming cycle of the on-chip EEPROM to be executed. When this bit is cleared, an ongoing programming cycle will be aborted or a new programming cycle will not start.

Figure 6-1. Data EEPROM Write Sequence

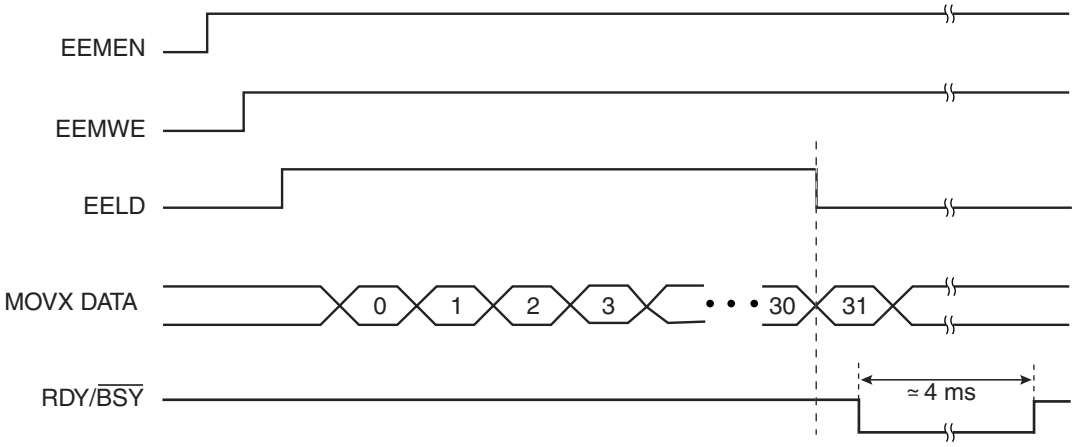
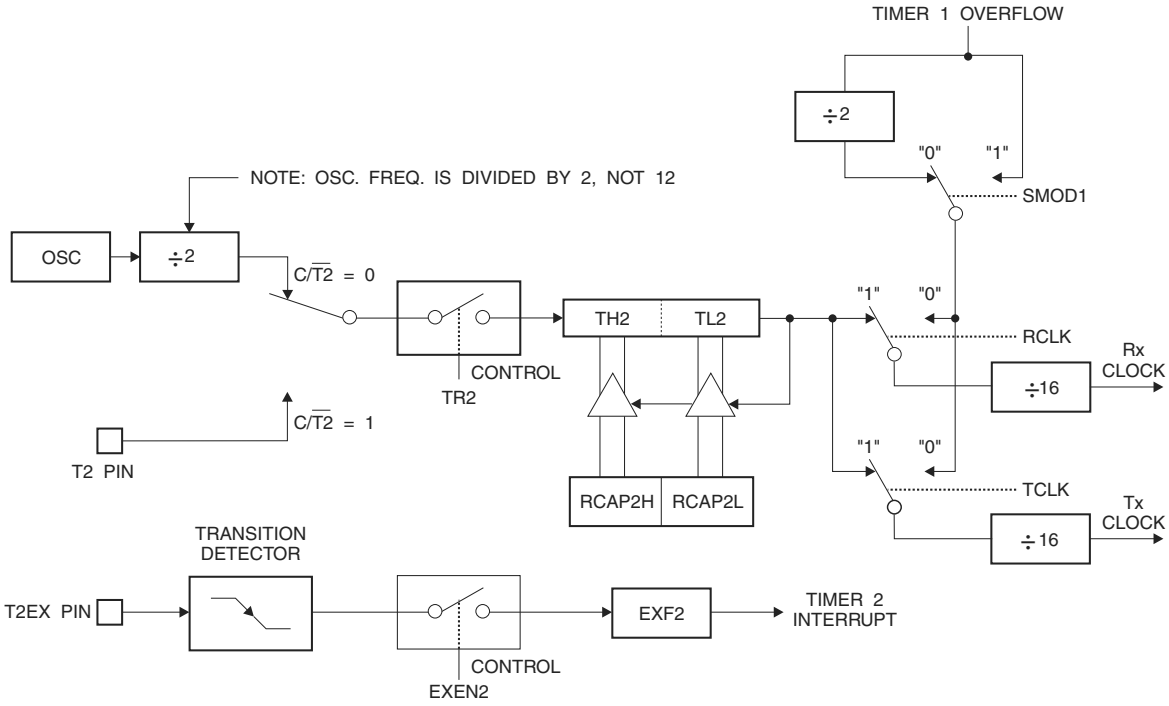


Figure 10-4. Timer 2 in Baud Rate Generator Mode



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 10-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10-4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Table 14-1. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 0100B

Not Bit Addressable

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI interrupt enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: **SPR1SPR0SCK** 00f/4 (f/2 in x2 mode) 01f/16 (f/8 in x2 mode) 10f/64 (f/32 in x2 mode) 11f/128 (f/64 in x2 mode)

Notes: 1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on next Tx if not loaded with new data.

Table 14-2. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 000X XX00B

Not Bit Addressable

	SPIF	WCOL	LDEN	–	–	–	DISSO	ENH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI interrupt flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register **followed by** reading/writing the SPI data register.
WCOL	When ENH = 0: Write collision flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register **followed by** reading/writing the SPI data register. When ENH = 1: WCOL works in Enhanced mode as Tx Buffer Full. Writing during WCOL = 1 in enhanced mode will overwrite the waiting data already present in the Tx Buffer. In this mode, WCOL is no longer reset by the SPIF reset but is reset when the write buffer has been unloaded into the serial shift register.
LDEN	Load enable for the Tx buffer in enhanced SPI mode. When ENH is set, it is safe to load the Tx Buffer while LDEN = 1 and WCOL = 0. LDEN is high during bits 0 - 3 and is low during bits 4 - 7 of the SPI serial byte transmission time frame.
DISSO	Disable slave output bit. When set, this bit causes the MISO pin to be tri-stated so more than one slave device can share the same interface with a single master. Normally, the first byte in a transmission could be the slave address and only the selected slave should clear its DISSO bit.
ENH	Enhanced SPI mode select bit. When ENH = 0, SPI is in normal mode, i.e. without write double buffering. When ENH = 1, SPI is in enhanced mode with write double buffering. The Tx buffer shares the same address with the SPDR register.

Table 14-3. SPDR – SPI Data Register

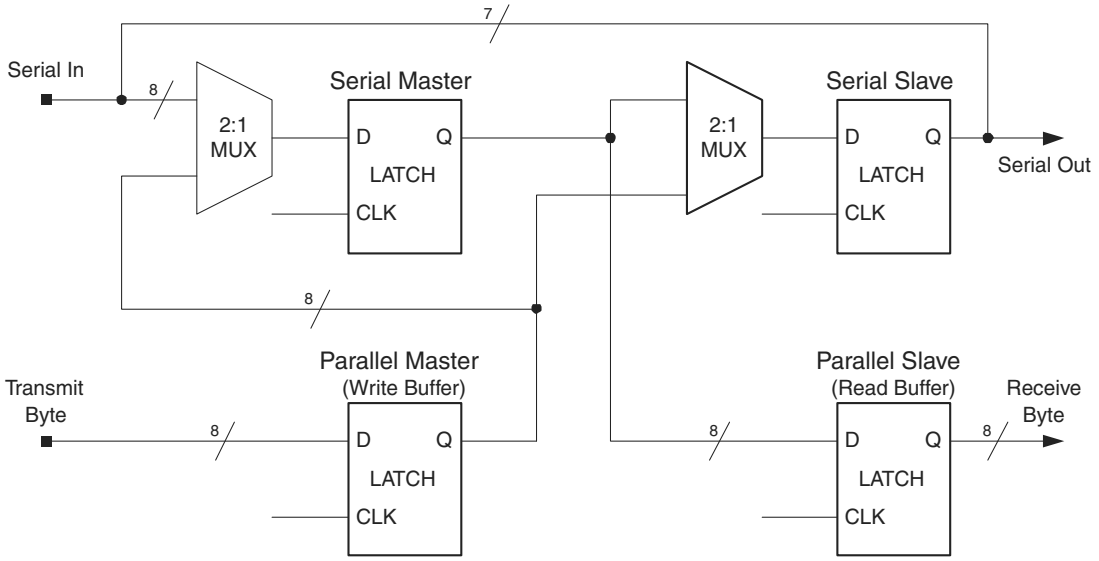
SPDR Address = 86H

Not Bit Addressable

Reset Value = 00H (after cold reset)
unchanged (after warm reset)

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Figure 14-3. SPI Shift Register Diagram



The CPHA (Clock PHAse), CPOL (Clock POLarity), and SPR (Serial Peripheral clock Rate = baud rate) bits in SPCR control the shape and rate of SCK. The two SPR bits provide four possible clock rates when the SPI is in master mode. In slave mode, the SPI will operate at the rate of the incoming SCK as long as it does not exceed the maximum bit rate. There are also four possible combinations of SCK phase and polarity with respect to the serial data. CPHA and CPOL determine which format is used for transmission. The SPI data transfer formats are shown in Figure 14-4 and Figure 14-5. To prevent glitches on SCK from disrupting the interface, CPHA, CPOL, and SPR should be set up before the interface is enabled, and the master device should be enabled before the slave device(s).

Table 14-4. SPI **Master** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	$t_{SCK}/2 - 25$		ns
t_{SLSH}	Clock Low Time	$t_{SCK}/2 - 25$		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns

Table 14-5. SPI **Slave** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	1.5 t_{CLCL} - 25		ns
t_{SLSH}	Clock Low Time	1.5 t_{CLCL} - 25		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{SOE}	Output Enable Time		10	ns
t_{SOX}	Output Disable Time		25	ns
t_{SSE}	Slave Enable Lead Time	4 t_{CLCL} +50		ns
t_{SSD}	Slave Disable Lag Time	0		ns

Figure 14-4. SPI Master Timing (CPHA = 0)

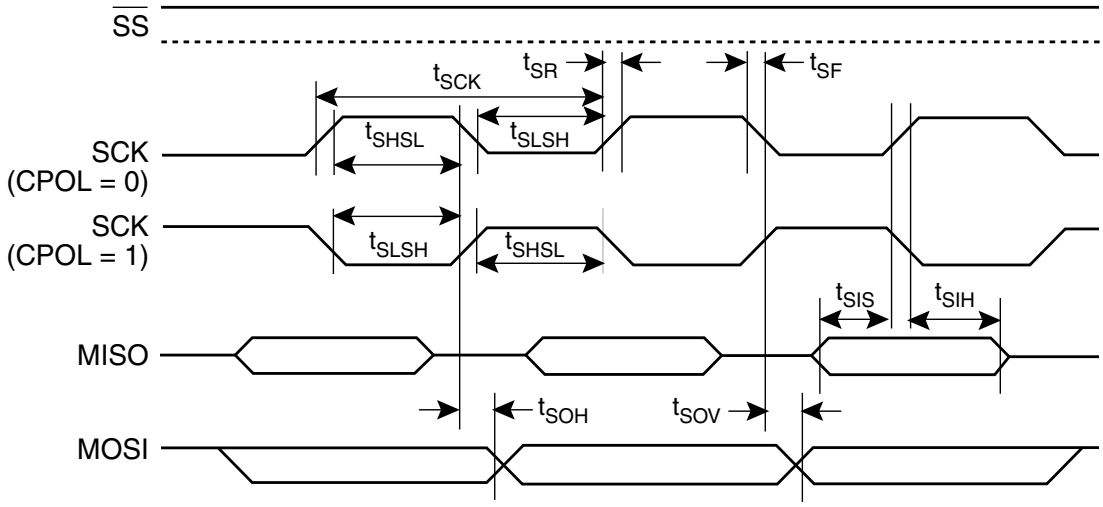
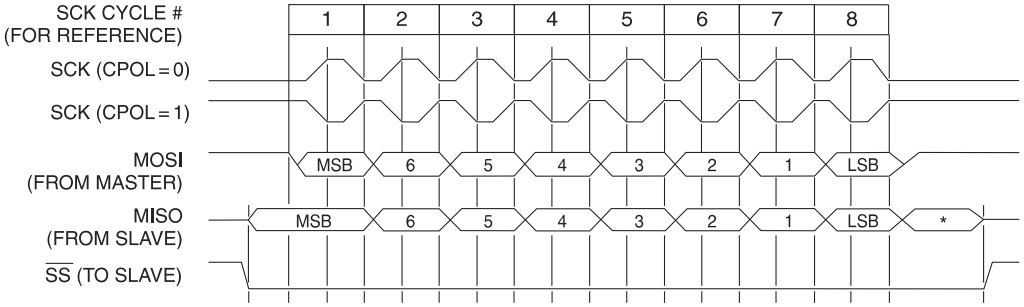
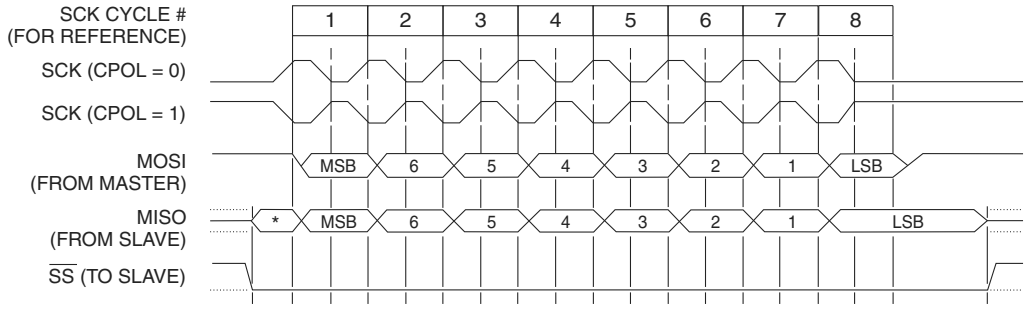


Figure 14-8. SPI Transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 14-9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character

15. Interrupts

The AT89S8253 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 15-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 15-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

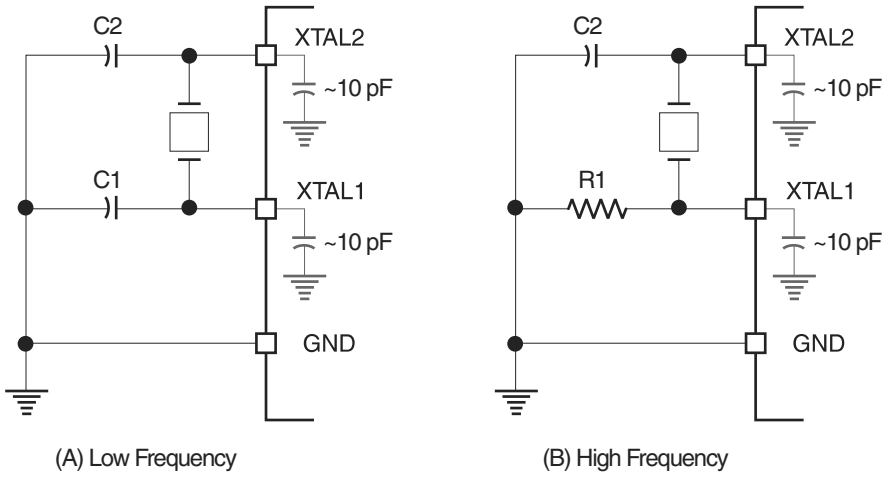
The serial interrupt is the logical OR of bits RI and TI in register SCON and also bit SPIF in SPSR (if SPIE in SPCR is set). None of these flags is cleared by hardware when the service routine is vectored to. The service routine may have to determine whether the UART or SPI generated the interrupt.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

16. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1 (A) and (B). Either a quartz crystal or ceramic resonator may be used. For frequencies above 16MHz it is recommended that C1 be replaced with R1 for improved startup performance. Note that the internal structure of the devices adds about 10 pF of capacitance to both XTAL1 and XTAL2. The total capacitance on XTAL1 or XTAL2, including the external load capacitor (C1/C2) plus internal device load, board trace and crystal loadings, should not exceed 20 pF. Figure 16-2, 16-3, 16-4 and 16-5 illustrate the relationship between clock loading and the respective resulting clock amplitudes.

Figure 16-1. Oscillator Connections



Note: C1, C2 = 0–10 pF for Crystals
= 0–10 pF for Ceramic Resonators
R1 = 4–5 MΩ

Figure 16-2. Quartz Crystal Clock Source (A)

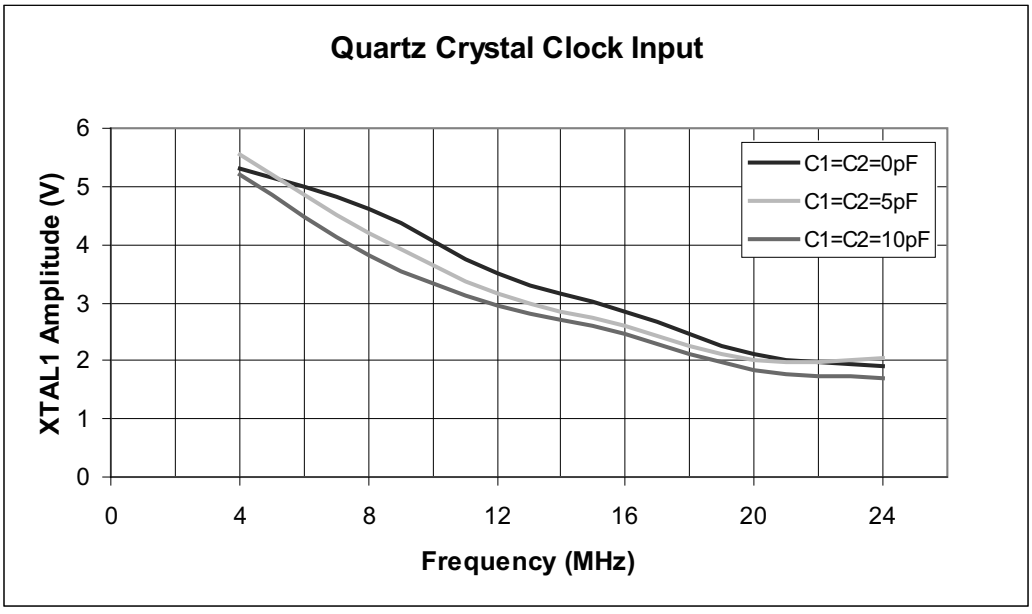


Table 17-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

18. Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, external interrupt pin P3.2 or P3.3 must be kept low for at least the specified required crystal oscillator start up time. Afterwards, the interrupt service routine starts at the **rising edge** of the external interrupt pin if the SFR bit AUXR.1 is set. If AUXR.1 is reset (cleared), execution starts after a self-timed interval of 2 ms (nominal) from the **falling edge** of the external interrupt pin. The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

19. Program Memory Lock Bits

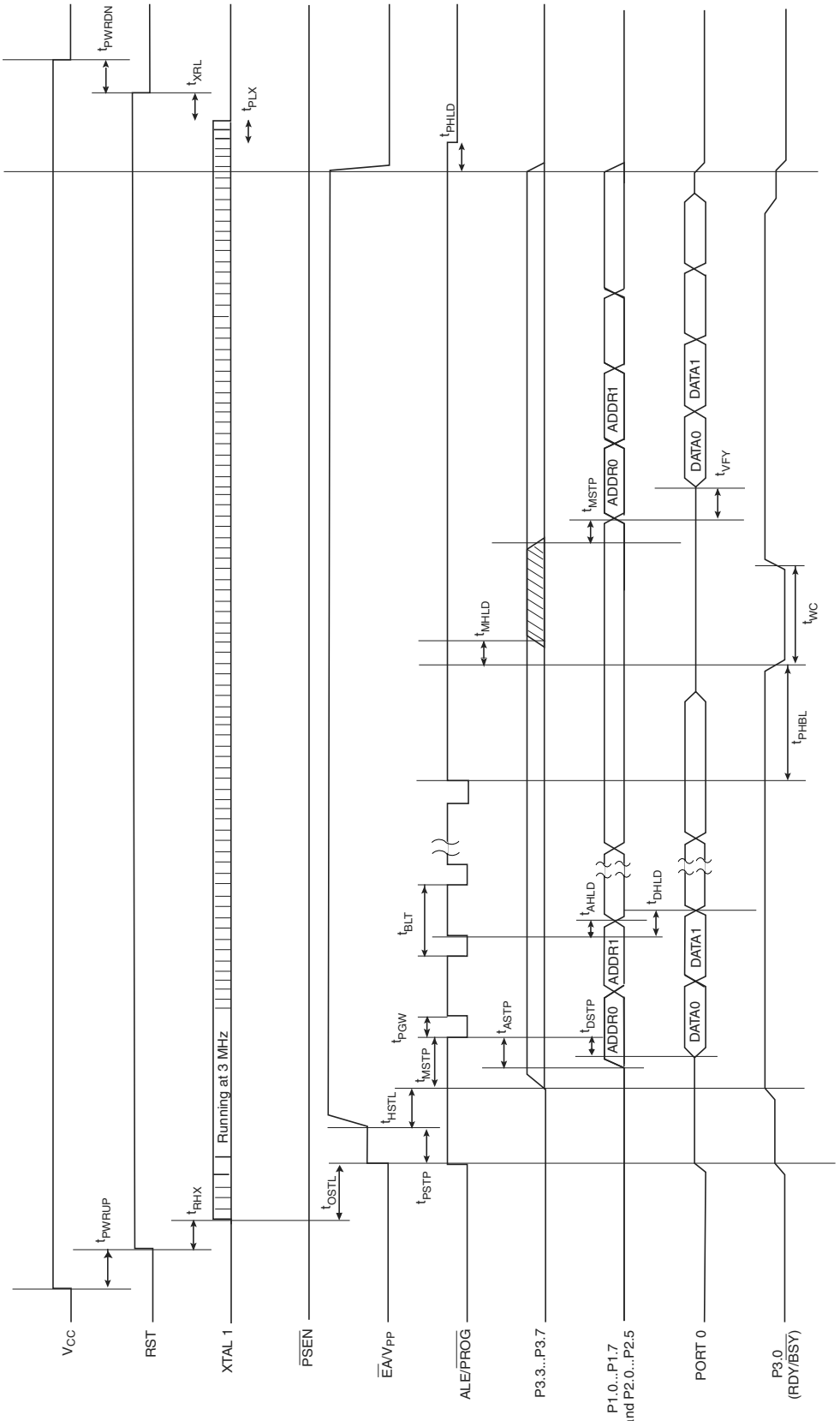
The AT89S8253 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 19-1. When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly. Once programmed, the lock bits can only be unprogrammed with the Chip Erase operation in either the parallel or serial modes.

Table 19-1. Lock Bit Protection Modes[1]

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Note: 1. U = Unprogrammed; P = Programmed

Figure 26-1. Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



29. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

30. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted

Symbol	Parameter	Condition	Min	Max
V_{IL}	Input Low-voltage	(Except $\overline{EA}$, XTAL1, RST, Port 0)	-0.5V	0.2 V_{CC} - 0.1V
V_{IL1}	Input Low-voltage	($\overline{EA}$, XTAL1, RST, Port 0)	-0.5V	0.3 V_{CC}
V_{IH}	Input High-voltage	(Except $\overline{EA}$, XTAL1, RST, Port 0)	0.5 V_{CC}	V_{CC} + 0.5V
V_{IH1}	Input High-voltage	($\overline{EA}$, XTAL1, RST, Port 0)	0.7 V_{CC}	V_{CC} + 0.5V
V_{OL}	Output Low-voltage[1]	I_{OL} = 10 mA, V_{CC} = 4.0V, T_A = 85°C		0.5V
V_{OH}	Output High-voltage When Weak Pull Ups are Enabled (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, T_A = 85°C	2.4V	
		I_{OH} = -25 µA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 µA, T_A = 85°C	0.9 V_{CC}	
V_{OH1}	Output High-voltage When Strong Pull Ups are Enabled (Port 0 in External Bus Mode, P1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -40 mA, T_A = 85°C	2.4V	
		I_{OH} = -25 mA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}	
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45V, V_{CC} = 5.5V, T_A = -40°C		-50 µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2V, V_{CC} = 5.5V, T_A = -40°C		-352 µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45V< V_{IN} < V_{CC}		±10 µA
RRST	Reset Pull-down Resistor		50 KΩ	150 KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10 pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		10 mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		3.5 mA
	Power-down Mode[2]	V_{CC} = 5.5V, T_A = -40°C		100 µA
		V_{CC} = 4.0V, T_A = -40°C		20 µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA,
   Maximum I_{OL} per 8-bit port:15 mA,
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

31. AC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted.

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

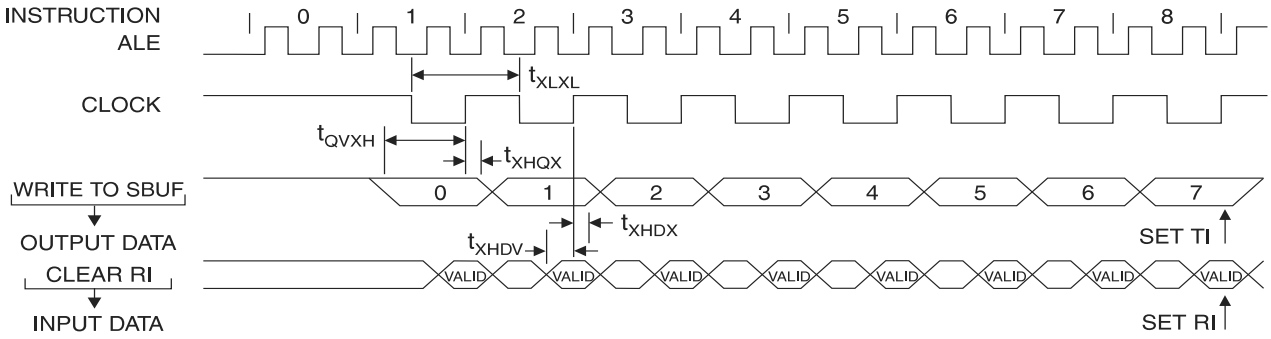
31.1 External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 12		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 12		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 16		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 50	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 12		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 12		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 50	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	-10		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 20	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 4		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 50	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		20	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 50	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 20	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 50	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 50	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 24	$3t_{CLCL}$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 12		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	$2t_{CLCL}$ - 24		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$8t_{CLCL}$ - 24		ns
t_{WHQX}	Data Hold after $\overline{WR}$	$2t_{CLCL}$ - 24		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 10	t_{CLCL} + 20	ns
t_{WHAX}	Address Hold after $\overline{RD}$ or $\overline{WR}$ High	t_{CLCL} - 10		ns

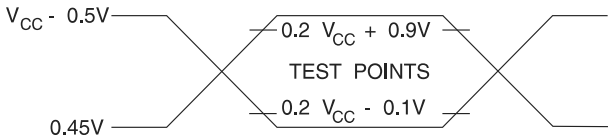
37. Serial Port Timing: Shift Register Mode Test Conditions

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	

38. Shift Register Mode Timing Waveforms

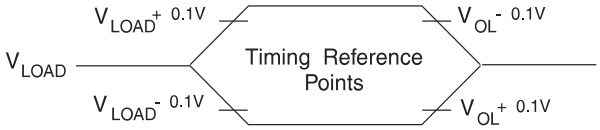


39. AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

40. Float Waveforms(1)



48. Ordering Information

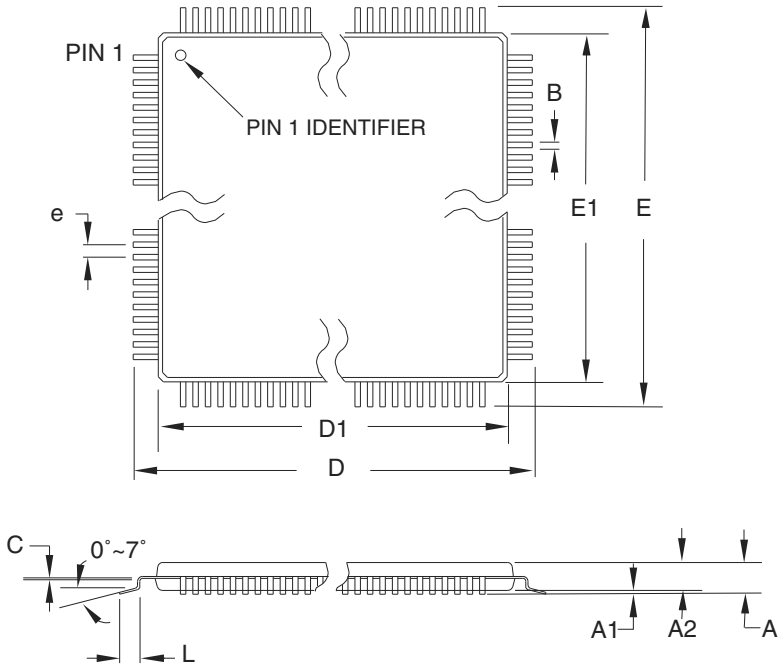
48.1 Green Package (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S8253-24AU AT89S8253-24JU AT89S8253-24PU AT89S8253-24PSU	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flat Package (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

49. Package Information

49.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

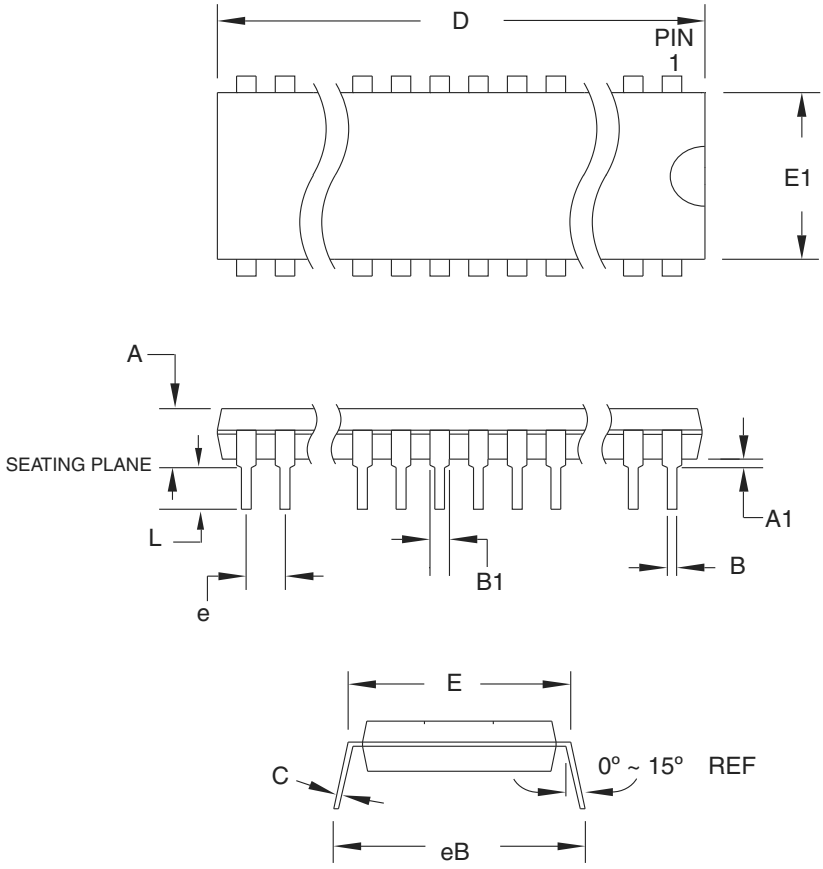
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

49.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

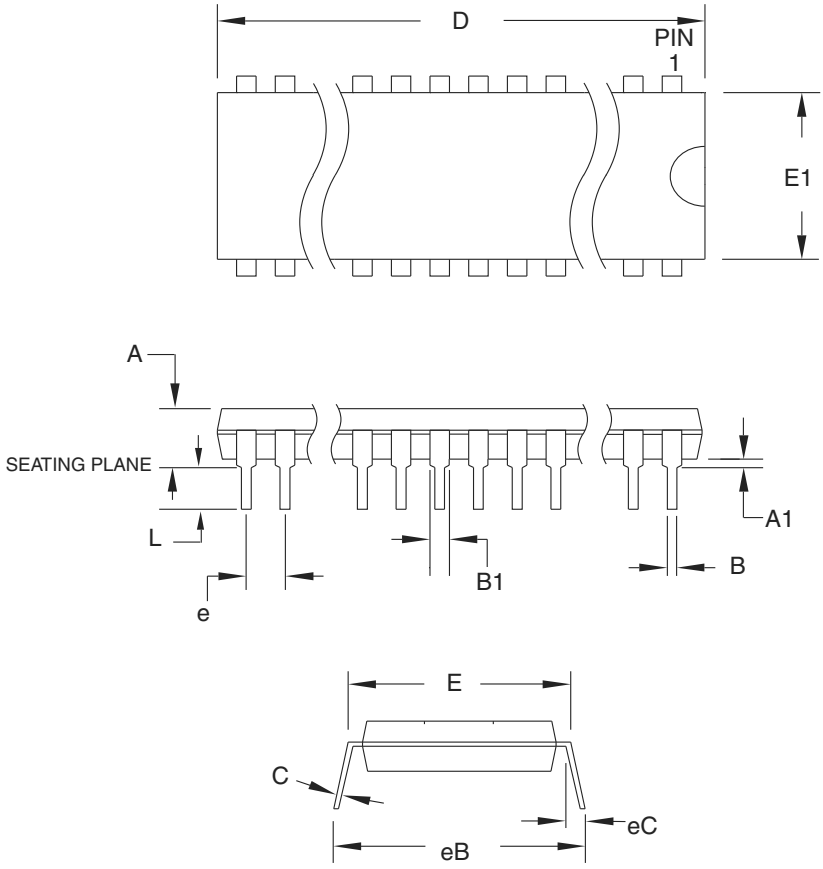
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

49.4 42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = Inch)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.200	
A1	0.020	–	–	
D	1.440	1.450	1.460	Note 2
E	0.600	–	0.630	
E1	0.500	0.540	0.570	Note 2
B	0.015	0.018	0.022	
B1	0.035	0.040	0.045	
L	0.100	0.130	0.140	
C	0.009	0.010	0.015	
eB	–	–	0.730	
eC	0.000	–	0.060	
e	0.70 TYP			

Notes: 1. This package conforms to JEDEC reference MS-020, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/3/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (Shrink 0.070"/0.600" Row Space) Plastic Dual Inline Package (PDIP)	42PS6	B