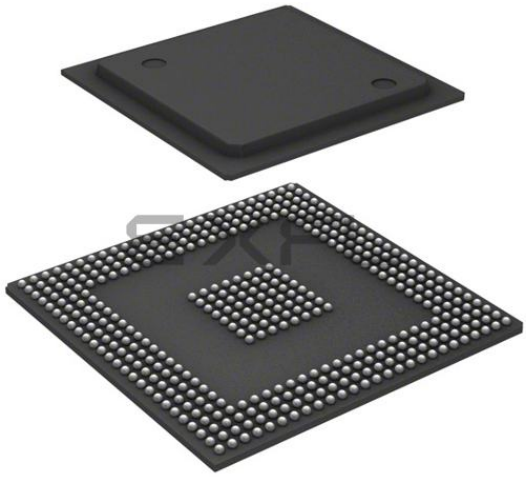

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Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	-
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5676rdk3mvu1

Table of Contents

4.4 ESD Characteristics

Table 6. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Table 7. PMC Operating conditions

Spec	Name	Parameter	Condition	Min	Typ	Max	Unit
1	V_{DDREG}	Supply voltage VDDREG 5 V nominal[1]	LDO5V / SMPS5V mode	4.5	5	5.5	V
2	V_{DDREG}	Supply voltage VDDREG 3 V nominal[1]	LDO3V mode	3.0	3.3	3.6	V
3	V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3 V nominal[2]	LDO3V mode	3.0	3.3	3.6	V
4	V_{DD}	Supply voltage VDD 1.2 V nominal[3]	—	1.14	1.2	1.32	V

1 Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

2 Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

3 Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, “untrimmed” means “at reset” and “trimmed” means “after reset”.

Table 8. PMC Electrical Specifications

Spec	Name	Symbol	Condition	Min	Typ	Max	Unit
1	Nominal bandgap reference voltage	V_{BG}	—	0.59	0.620	0.65	V
1a	Bandgap reference voltage during power on reset	—	—	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
1b	Bandgap reference voltage at nominal voltage / nominal temperature after power on reset	—	—	V_{BG} – 2%	V_{BG}	V_{BG} + 2%	V

Table 18. Oscillator Electrical Specifications[1] (continued)

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[4]$)$	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$(2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[4]$)$	pF

1 All values given are initial design targets and subject to change.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.

3 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

4 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

4.9 eQADC Electrical Characteristics

Table 19. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles	CC	2 + 13	128 + 14	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	—	±4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	—	±4[4,6]	Counts

Table 19. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	—	±8	Counts
17	Variable gain amplifier accuracy (gain=1)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA1	 –4 –8 -3^{16} -3^{16}	 4 8 3^{16} 3^{16}	Counts[17]
18	Variable gain amplifier accuracy (gain=2)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA2	 –5 –8 –3 –3	 5 8 3 3	Counts
19	Variable gain amplifier accuracy (gain=4)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA4	 –7 –8 –4 –4	 7 8 4 4	Counts

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} - V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

16 Guaranteed 10-bit mono tonicity.

17 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4.9.1 ADC Internal Resource Measurements

Table 20. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	0.59	0.62	0.65	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	1.10	1.22	1.34	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	V_{DD}/2.147	V_{DD} / 2.045	V_{DD}/1.943	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	V_{DD}/1.863	V_{DD} / 1.774	V_{DD}/1.685	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	Vreg3p3 / 5.733—	Vreg3p3 / 5.460	Vreg3p3 / 5.187	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	Vreg3p3 / 4.996	Vreg3p3 / 4.758	Vreg3p3 / 4.520	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	V_{DDREG} / 4.996 V_{DDREG} / 7.384	 V_{DDREG} / 4.758 V_{DDREG}/7.032	V_{DDREG} / 4.520 V_{DDREG} / 6.680	V

Table 21. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias ADC1 channel 195	V_{ADC195}	150	—	360	mV

Table 22. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	—	1.220	—	V

4.11.2 Pad AC Specifications

Table 29. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	200
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 30. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

Table 33. Nexus Debug Port Timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	$\overline{RDY}$ Valid to MCKO[5]	—	—	—	—
14	TDO hold time after TCLK low	t_{NTDOH}	1	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

3 MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.

4 Lower frequency is required to be fully compliant to standard.

5 The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

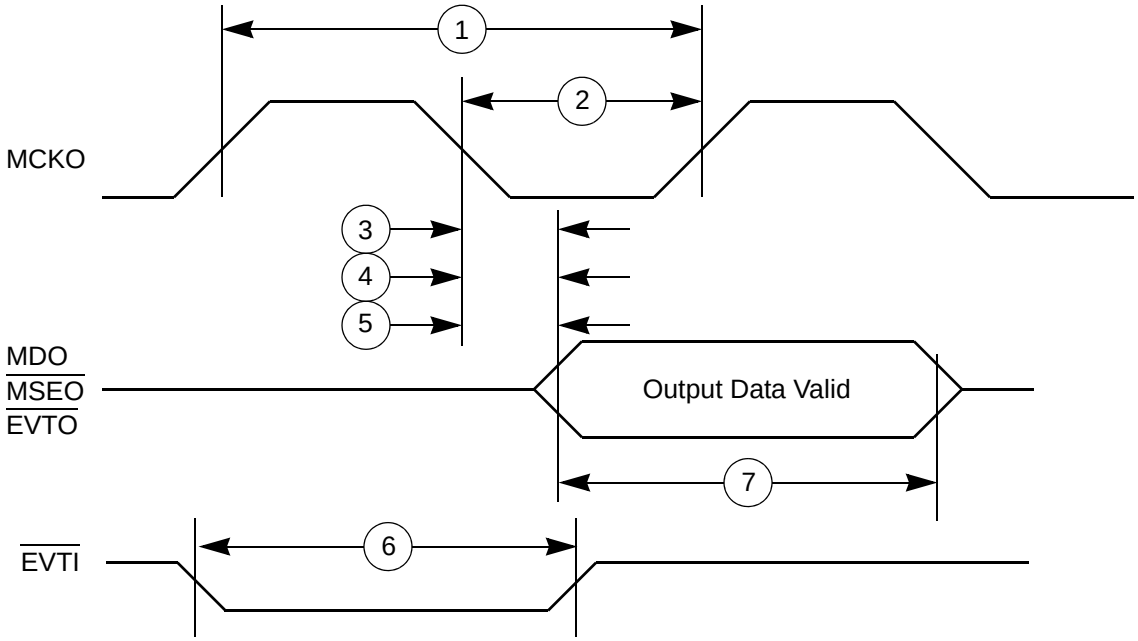

Figure 15. Nexus Timings

Table 34. Bus Operation Timing [1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	8.5/9.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIS}	5.0/4.5	—	ns	Input setup time selectable via SIU_ECCR[EBTS] bit: EBTS = 0; 5.0ns EBTS = 1; 4.5ns
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIH}	1.0	—	ns	
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1 EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM).

3 Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

4 Refer to Fast pad timing in Table 29 and Table 30.

5 ALE hold time spec is temperature dependant. 1.0ns spec applies for temperature range -40 to 0 C. 2.0ns spec applies to temperatures > 0 C. This spec has no dependency on SIU_ECCR[EBTS] bit.

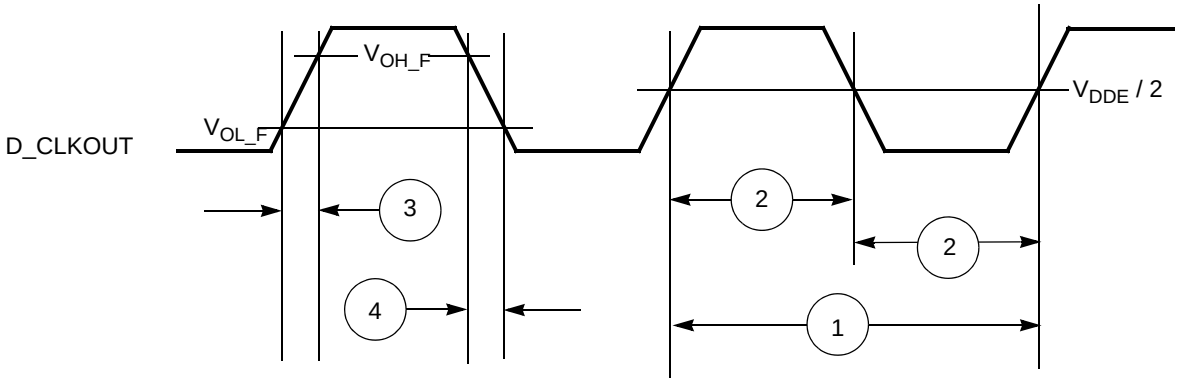

Figure 17. D_CLKOUT Timing

Table 38. DSPI Timing[1,2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 92 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 27 10 7 27	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –3 7 12 –3	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1) Master (LVDS)	t_{SUO}	 — — — — —	 10 30 20 10 5	 ns ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1) Master (LVDS)	t_{HO}	 –6 2.5 3 –7 –5	 — — — — —	 ns ns ns ns ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM).

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 This number is calculated assuming the SMPL_PT bit-field in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

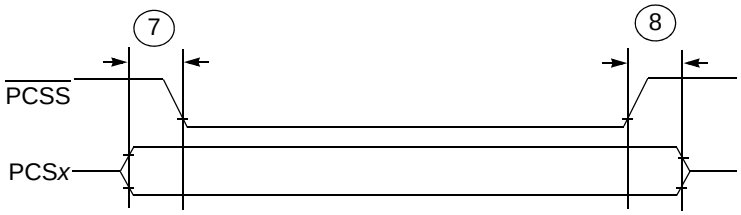

Figure 32. DSPI PCS Strobe (PCSS) Timing

5 Package Information

5.1 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 33 and Figure 34.

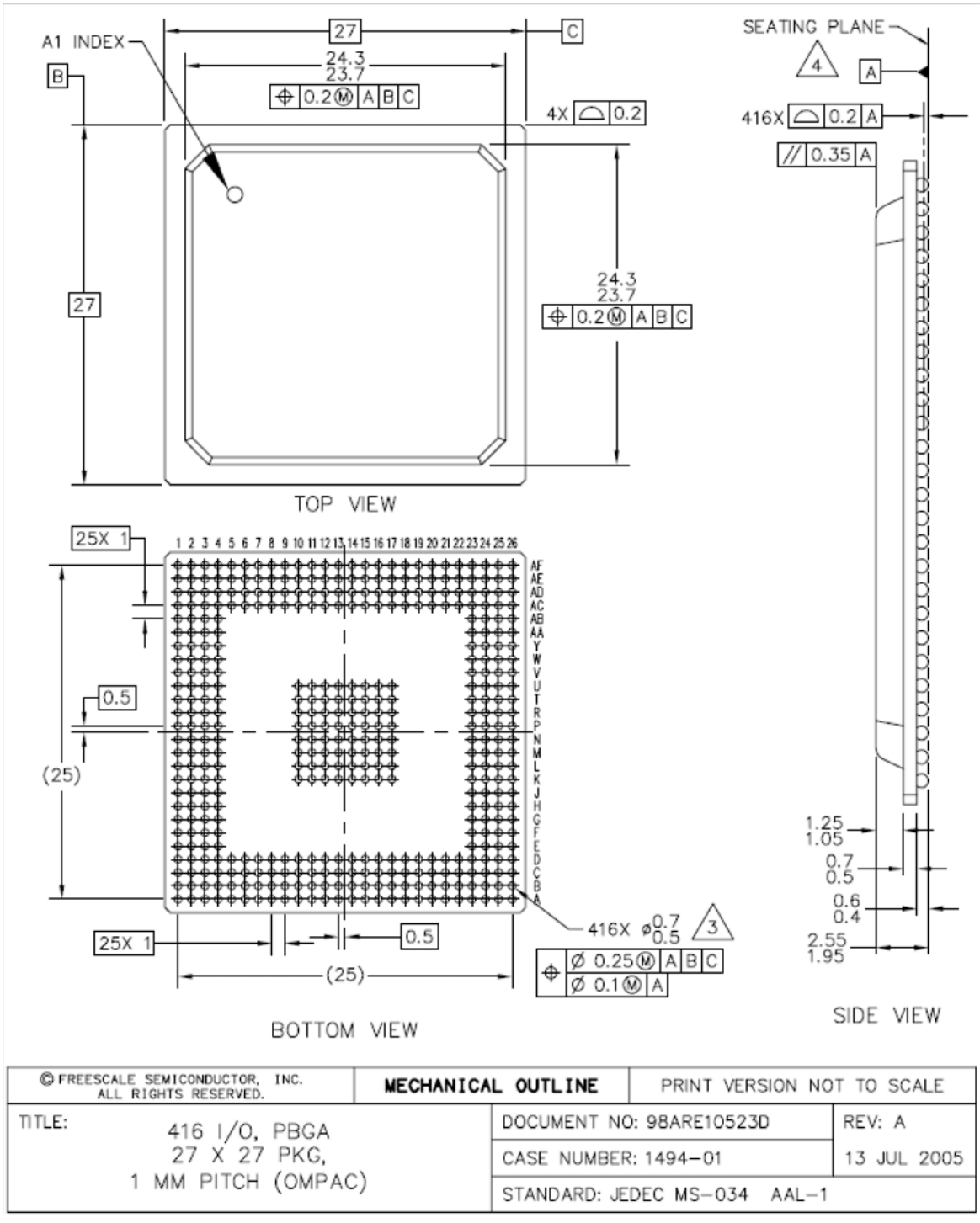

Figure 33. 416 TEPBGA Package (1 of 2)

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO115	GPIO	I/O						
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO116	GPIO	I/O						
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO117	GPIO	I/O						
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO118	GPIO	I/O						
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO119	GPIO	I/O						
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO120	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
466	ETPUC25_PCSD3_ GPIO466	P	ETPUC25	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K25	K21
		A1	PCSD3	DSPI D peripheral chip select	O						
		A2	MAA2	ADC A Mux Address 2	O						
		A3	MAB2	ADC B Mux Address 2	O						
		G	GPIO466	GPIO	I/O						
467	ETPUC26_PCSD2_ GPIO467	P	ETPUC26	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K26	J25
		A1	PCSD2	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO467	GPIO	I/O						
468	ETPUC27_PCSD1_ GPIO468	P	ETPUC27	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L23	J26
		A1	PCSD1	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO468	GPIO	I/O						
469	ETPUC28_PCSD0_ GPIO469	P	ETPUC28	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L24	K22
		A1	PCSD0	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO469	GPIO	I/O						
470	ETPUC29_SCKD_ GPIO470	P	ETPUC29	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L25	K23
		A1	SCKD	DSPI D clock	I/O						
		A2	—	—	—						
		G	GPIO470	GPIO	I/O						
471	ETPUC30_SOUTD_ GPIO471	P	ETPUC30	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L26	K24
		A1	SOUTD	DSPI D data output	O						
		A2	—	—	—						
		G	GPIO471	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE15	AB15
		A1	ETPUB1	eTPU B channel	O						
		A2	FR_DBG[2]	FlexRay debug	O						
		G	GPIO196	GPIO	I/O						
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC15	AD17
		A1	ETPUB2	eTPU B channel	O						
		A2	FR_DBG[1]	FlexRay debug	O						
		G	GPIO197	GPIO	I/O						
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD15	AB16
		A1	ETPUB3	eTPU B channel	O						
		A2	FR_DBG[0]	FlexRay debug	O						
		G	GPIO198	GPIO	I/O						
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF16	AF16
		A1	ETPUB4	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO199	GPIO	I/O						
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE16	AE17
		A1	ETPUB5	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO200	GPIO	I/O						
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC16	AC16
		A1	ETPUB6	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO201	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AB12
		A1	D_ADD_DAT29	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO276	GPIO	I/O						
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AE12
		A1	D_ADD_DAT30	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO277	GPIO	I/O						
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	P25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO278	GPIO	I/O						
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	P26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO279	GPIO	I/O						
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO280	GPIO	I/O						
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO281	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO282	GPIO	I/O						
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO283	GPIO	I/O						
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO284	GPIO	I/O						
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO285	GPIO	I/O						
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO286	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
227	$\overline{\text{EVTO}}$ (the BAM uses this pin to select if auto baud rate is on or off)	–[12]	EVTO	Nexus event out	O	F	V_{DDE2}	ABS/Up	EVTO/HI	U1	V2
219	MCKO	–[12]	MCKO	Nexus message clock out	O	F	V_{DDE2}	O/Low	Disabled[13]	T2	U4
220	MDO0_GPIO220	–[12]	MDO0[14]	Nexus message data out	O	F	V_{DDE2}	See Note[15]	See Note[15]	U3	V3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO220	GPIO	I/O						
221	MDO1_GPIO221	–[12]	MDO1[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U4	W6
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO221	GPIO	I/O						
222	MDO2_GPIO222	–[12]	MDO2[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V1	V4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO222	GPIO	I/O						
223	MDO3_GPIO223	–[12]	MDO3[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V2	V5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO223	GPIO	I/O						
75	MDO4_GPIO75	–[12]	MDO4[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V3	W1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO75	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
76	MDO5_GPIO76	–[12]	MDO5[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V4	W2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO76	GPIO	I/O						
77	MDO6_GPIO77	–[12]	MDO6[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W1	W3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO77	GPIO	I/O						
78	MDO7_GPIO78	–[12]	MDO7[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W2	Y1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO78	GPIO	I/O						
79	MDO8_GPIO79	–[12]	MDO8[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W3	W5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO79	GPIO	I/O						
80	MDO9_GPIO80	–[12]	MDO9[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y1	Y2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO80	GPIO	I/O						
81	MDO10_GPIO81	–[12]	MDO10[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y2	Y3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO81	GPIO	I/O						

Table 40. Revision History (continued)

Revision	Date	Description
Rev 3	10 August 2012	Added minimum and maximum “Nominal bandgap reference voltage” values in the “PMC Electrical Specifications” table. Updated the maximum “Medium I/O Output Low Voltage” value (changed from 0.2 x V_{DDEH} to 0.2 x V_{DDEH} and 0.15 x $_{VDDEH}$) in the “DC Electrical Specifications” table, moved reference to the footnote [10] (I_{OH_S} = {11.6} mA and I_{OL_S} = {17.7} mA for {medium} I/O with V_{DDEH} = 4.5 V; I_{OH_S} = {5.4} mA and I_{OL_S} = {8.1} mA for {medium} I/O with VDDEH = 3.0 V) to “0.2 x V_{DDEH}”, and added a new footnote [11](IOL_S=2 mA) to “0.15 x V_{DDEH}”. Updated footnote[9] (I_{OH_F} = {12,20,30,40} mA and I_{OL_F} = {24,40,50,65} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V): Removed “I_{OH_F} = {7,13,18,25} mA and I_{OL_F} = {18,30,35,50} mA for {00,01,10,11} drive mode with V_{DDE} = 2.25 V; I_{OH_F} = {3,7,10,16}mA and I_{OL_F} = {12,20,27,35} mA for {00,01,10,11} drive mode with V_{DDE} = 1.62 V”. Added minimum and maximum values to all rows of the “Power Management Control (PMC) Specification” table. Updated the “Accuracy” temperature values in the “Temperature Sensor Electrical Specifications” table: Changed “–40 C to 100 C to 40 C to 150 C, removed the correspnding “Typ” value, removed “100 C to 150 C, and added minimum (10) and maximum (+10) values. Added a new section “ADC Internal Resource Measurements” and moved “Power Management Control (PMC) Specification”, “Standby RAM Regulator Electrical Specifications”, “ADC Band Gap Reference / LVI Electrical Specifications”, and “Temperature Sensor Electrical Specifications” tables to the section. Changed “Minimum Data Retention at 25 °C ambient temperature” to “Minimum Data Retention at 85 °C ambient temperature” in the “Flash EEPROM Module Life” table. Added the following note after “Flash Program and Erase Specifications (Pending Si characterization)” table in the “C90 Flash Memory Electrical Characteristics” section: “The low, mid, and high address blocks of the flash arrays are erased (all bits set to 1) before leaving the factory. Updated the “DSPI LVDS Pad Specification” table: Changed maximum “Load” value from “25” to “32”; minimum values for “Differential Output Voltage SRC=0b00 or 0b11, SRC=0b01, SRC=0b10” from “150, 90, 160” to “215, 170, 260”; “Transmission lines (Differential) to “Termination Resistance”; “Z_C” to “R_{Load}”; and added the following footnote: “The termination resistance spec is not meant to specify the receiver termination requirements. They are there to establish the measurement criteria for the specs in this table. As per the TIA/EIA-644A standard, the LVDS receiver termination resistance can vary from 90 to 132 Ω .
Rev 4	21 January 2016	Added a table “Flash Memory AC Timing Specifications”. Updated the min and max values from -10 and +10 to -20 and +20 for “Accuracy” in the “Temperature Sensor Electrical Specifications” table.