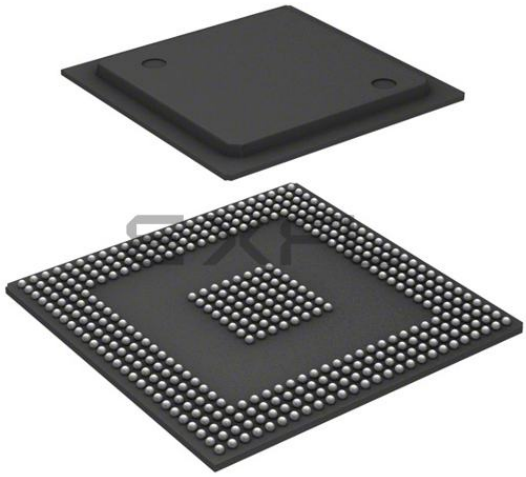


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

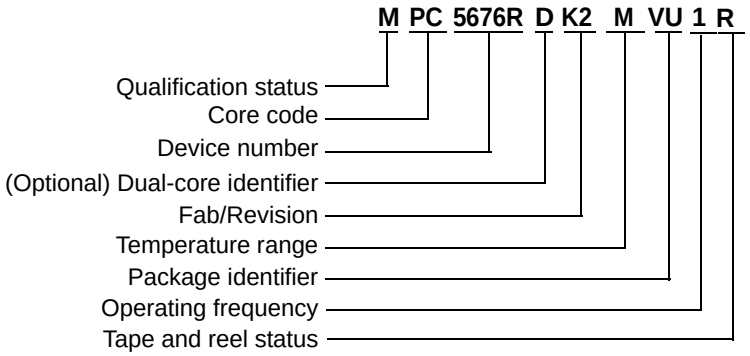
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z7 |
| Core Size | 32-Bit Dual-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, SCI, SPI |
| Peripherals | DMA, POR, PWM |
| Number of I/O | - |
| Program Memory Size | 6MB (6M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 1.32V |
| Data Converters | A/D 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 416-BBGA |
| Supplier Device Package | 416-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5676rdk3mvu1r |

# 1 Ordering Information

## 1.1 Orderable Parts

Figure 1 and Table 1describe and list the orderable part numbers for the MPC5676R.




**Temperature Range**
M = –40 °C to 125 °C

**Package Identifier**
VU = 416 TEPBGA
Pb-Free
VY = 516 TEPBGA
Pb-Free

**Operating Frequency**
1 = 2 x 180 MHz

**Tape and Reel Status**
R = Tape and reel
(blank) = Trays

**Qualification Status**
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

**Note:** Not all options are available on all devices. Refer to Table 1.

**Figure 1. MPC5676R Orderable Part Number Description**

**Table 1. Orderable Part Numbers**

| NXP Part Number[1] | Package Description | Speed (MHz)[2] | | Operating Temperature[3] | |
|---|---|---|---|---|---|
| | | Nominal | Max[4] ($f_{MAX}$) | Min ($T_L$) | Max ($T_H$) |
| SPC5676RDK2MVU1R | MPC5676R 416 package Lead-free (Pb-free) | 180 | 184 | –40 °C | 125 °C |
| SPC5676RDK2MVY1R | MPC5676R 516 package Lead-free (Pb-free) | 180 | 184 | –40 °C | 125 °C |

1 All packaged devices are PPC5676R, rather than MPC5676R or SPC5676R, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.
Not all configurations are available in the PPC parts.

2 For the operating mode frequency of various blocks on the device, see Table 28.

3 The lowest ambient operating temperature is referenced by $T_L$; the highest ambient operating temperature is referenced by $T_H$.

4 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 180 MHz parts allow for 180 MHz system clock + 2% FM.

## 3.3 Pin Muxing and Reset States

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

# 4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5676R.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

## 4.1 Maximum Ratings

**Table 2. Absolute Maximum Ratings[1]**

| Spec | Characteristic | Symbol | Min | Max[2] | Unit |
|---|---|---|---|---|---|
| 1 | 1.2 V Core Supply Voltage[3] | $V_{DD}$ | –0.3 | 1.65 [4] | V |
| 2 | SRAM Standby Voltage | $V_{STBY}$ | –0.3 | 5.5 [5,6] | V |
| 3 | Clock Synthesizer Voltage | $V_{DDSYN}$ | –0.3 | 4.5 [6,7] | V |
| 4 | I/O Supply Voltage (I/O buffers and predrivers) | $V_{DD33}$ | –0.3 | 4.5 [6,7] | V |
| 5 | Analog Supply Voltage (reference to $V_{SSA}$[8]) | $V_{DDA}$[9] | –0.3 | 5.5 [5,6] | V |
| 6 | I/O Supply Voltage (fast I/O pads) | $V_{DDE}$ | –0.3 | 4.5 [6] | V |
| 7 | I/O Supply Voltage (medium I/O pads) | $V_{DDEH}$ | –0.3 | 5.5 [5,6] | V |
| 8 | Voltage Regulator Input Supply Voltage | $V_{DDREG}$ | –0.3 | 5.5[5,6] | V |
| 9 | Analog Reference High Voltage (reference to $V_{RL}$[10]) | $V_{RH}$[11] | –0.3 | 5.5 [5,6] | V |
| 10 | $V_{SS}$ to $V_{SSA}$[8] Differential Voltage | $V_{SS} – V_{SSA}$ | –0.1 | 0.1 | V |
| 11 | $V_{REF}$ Differential Voltage | $V_{RH} – V_{RL}$ | –0.3 | 5.5 [5,6] | V |
| 12 | $V_{RL}$ to $V_{SSA}$ Differential Voltage | $V_{RL} – V_{SSA}$ | –0.3 | 0.3 | V |
| 13 | $V_{DD33}$ to $V_{DDSYN}$ Differential Voltage | $V_{DD33} – V_{DDSYN}$ | –0.1 | 0.1 | V |
| 14 | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage | $V_{SSSYN} – V_{SS}$ | –0.1 | 0.1 | V |
| 15 | Maximum Digital Input Current [12] (per pin, applies to all digital pins) | $I_{MAXD}$ | –3 [13] | 3 [13] | mA |
| 16 | Maximum Analog Input Current [14] (per pin, applies to all analog pins) | $I_{MAXA}$ | –3 [9,13] | 3 [9,13] | mA |

**Table 2. Absolute Maximum Ratings[1] (continued)**

| Spec | Characteristic | Symbol | Min | Max[2] | Unit |
|---|---|---|---|---|---|
| 17 | Maximum Operating Temperature Range [15] – Die Junction Temperature | $T_J$ | –40.0 | 150.0 | $^oC$ |
| 18 | Storage Temperature Range | $T_{stg}$ | –55.0 | 150.0 | $^oC$ |
| 19 | Maximum Solder Temperature [16]<br>Pb-free package<br>SnPb package | $T_{sdr}$ | <br>—<br>— | <br>260.0<br>245.0 | $^oC$ |
| 20 | Moisture Sensitivity Level [17] | MSL | — | 3 | — |

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 1.2 V ±10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

4 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

7 4.5 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

8 MPC5676R has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

9 MPC5676R has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

10 MPC5676R has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

11 MPC5676R has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

12 Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

13 Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or $V_{DDEH}$ supply when under this stress condition.

14 Total injection current for all analog input pins must not exceed 15 mA.

15 Lifetime operation at these specification limits is not guaranteed.

16 Solder profile per CDF-AEC-Q100.

17 Moisture sensitivity per JEDEC test method A112.

## 4.2 Thermal Characteristics

**Table 3. Thermal Characteristics, 416-pin TEPBGA Package[1]**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Junction to Ambient [2,3] Natural Convection (Single layer board) | $R_{\theta JA}$ | 24 | °C/W |
| Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p) | $R_{\theta JA}$ | 16 | °C/W |
| Junction to Ambient (@200 ft./min., Single layer board) | $R_{\theta JMA}$ | 18 | °C/W |

**Table 8. PMC Electrical Specifications**

| Spec | Name | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1c | Bandgap reference voltage / temperature dependence after power on reset | — | — | — | 300 | — | ppm/C |
| 1d | Bandgap reference voltage / voltage dependence ($V_{DDREG}$) after power on reset | — | — | — | 1500 | — | |
| 2 | Nominal VRC regulated 1.2V output VDD[1] | $V_{DD12OUT}$ | — | — | 1.2 | — | V |
| 2a | VRC 1.2V output variation at reset (unloaded)[2] | — | At POR | $V_{DD12OUT}$ – 8% | $V_{DD12OUT}$ | $V_{DD12OUT}$ + 10% | |
| 2b | VRC 1.2V output variation after reset(REGCTL load max. 20mA, VDD load max. 1A) | — | After POR | $V_{DD12OUT}$ – 5% | $V_{DD12OUT}$ | $V_{DD12OUT}$ + 10% | |
| 2c | Trimming step Vdd1p2 | $V_{STEPV12}$ | — | — | 10 | — | mV |
| 3 | POR rising VDD 1.2V | $V_{PORC}$ | — | - | 0.7 | — | V |
| 3a | POR VDD 1.2V variation | — | — | $V_{PORC}$ – 30% | $V_{PORC}$ | $V_{PORC}$ + 30% | |
| 3b | POR 1.2V hysteresis | — | — | — | 75 | — | mV |
| 4 | Nominal rising LVD 1.2V[3] | $V_{LVD12}$ | — | — | 1.100 | — | V |
| 4a | LVD 1.2V variation before band gap trim[4] | — | At POR | $V_{LVD12}$ – 6% | $V_{LVD12}$ | $V_{LVD12}$ + 6% | |
| 4b | LVD 1.2V variation after band gap trim[4] | — | After POR | $V_{LVD12}$ – 3% | $V_{LVD12}$ | $V_{LVD12}$ + 3% | |
| 4c | LVD 1.2V Hysteresis | — | — | 15 | 20 | 25 | mV |
| 4d | Trimming step LVD 1.2V | $V_{LVDSTEP12}$ | — | — | 10 | — | mV |
| 5 | VRC 1.2V max DC output current | $I_{REGCTL}$ | — | — | — | 20 | mA |
| 6 | Voltage regulator 1.2V current consumption VDDREG | — | — | — | 3 | — | mA |
| 7 | Nominal Vreg 3.3V output[5] | $V_{DD33OUT}$ | — | — | 3.3 | — | V |
| 7a | Vreg 3.3V output variation at reset (unloaded)[6] | — | At POR | $V_{DD33OUT}$ – 6% | $V_{DD33OUT}$ | $V_{DD33OUT}$ + 10% | |
| 7b | Vreg 3.3V output variation after reset (max. load 60mA) | — | After POR | $V_{DD33OUT}$ – 5% | $V_{DD33OUT}$ | $V_{DD33OUT}$ + 10% | |
| 7c | Trimming step VDDSYN | $V_{STEPV33}$ | — | — | 30 | — | mV |
| 8 | Nominal rising LVD 3.3V[7] | $V_{LVD33}$ | — | — | 2.950 | — | V |
| 8a | LVD 3.3V variation before band gap trim[6] | — | At POR | $V_{LVD33}$ – 5% | $V_{LVD33}$ | $V_{LVD33}$ + 5% | |
| 8b | LVD 3.3V variation after bad gap trim[6] | — | After POR | $V_{LVD33}$ – 3% | $V_{LVD33}$ | $V_{LVD33}$ + 3% | |

**Table 8. PMC Electrical Specifications**

| Spec | Name | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 8c | LVD 3.3V Hysteresis | — | — | — | 30 | — | mV |
| 8d | Trimming step LVD 3.3V | $V_{LVDSTEP33}$ | — | — | 30 | — | mV |
| 9 | Vreg 3.3V minimum peak DC output current supplied by regulator without causing $V_{LVD33}$[8] | $I_{DD33}$ | — | 60 | — | — | mA |
| 10 | Voltage regulator 3.3V current consumption VDDREG[9] | — | — | — | 2 | — | mA |
| 11 | POR rising on VDDREG | $V_{PORREG}$ | — | — | 2.00 | — | V |
| 11a | POR VDDREG variation | — | — | $V_{PORREG}$ – 30% | $V_{PORREG}$ | $V_{PORREG}$ + 30% | |
| 11b | POR VDDREG hysteresis | — | — | — | 250 | — | mV |
| 12 | Nominal rising LVD VDDREG | $V_{LVDREG}$ | LDO3V / LDO5V mode | — | 2.950 | — | V |
| 12a | LVD VDDREG variation at reset[10] | — | At POR | $V_{LVDREG}$ – 5% | $V_{LVDREG}$ | $V_{LVDREG}$ + 5% | |
| 12b | LVD VDDREG variation after reset[10] | — | After POR | $V_{LVDREG}$ – 3% | $V_{LVDREG}$ | $V_{LVDREG}$ + 3% | |
| 12c | LVD VDDREG Hysteresis | — | LDO3V / LDO5V mode | — | 30 | — | mV |
| 12d | Trimming step LVD VDDREG | $V_{LVDSTEPREG}$ | LDO3V / LDO5V mode | — | 30 | — | mV |
| 13 | Nominal rising LVD VDDREG | $V_{LVDREG}$ | SMPS5V mode | — | 4.360 | — | V |
| 13a | LVD VDDREG variation at reset[10] | — | At POR | $V_{LVDREG}$ – 5% | $V_{LVDREG}$ | $V_{LVDREG}$ + 5% | |
| 13b | LVD VDDREG variation after reset[10] | — | After POR | $V_{LVDREG}$ – 3% | $V_{LVDREG}$ | $V_{LVDREG}$ + 3% | |
| 14 | SMPS regulator output resistance[11] | — | — | — | 15 | 25 | Ohm |
| 15 | SMPS regulator clock frequency | — | After POR | 1.0 | 1.5 | — | MHz |
| 16 | SMPS regulator overshoot at start-up[12] | — | GBD/GBC[13] | — | 1.32 | 1.4 | V |
| 17 | SMPS maximum output current, as required by SoC[14] | — | — | — | 1.0 | — | A |
| 18 | Voltage variation on current step (20% to 80% of maximum current with 4 usec constant time)[14] | — | GBD/GBC[13] | — | — | 0.1 | V |

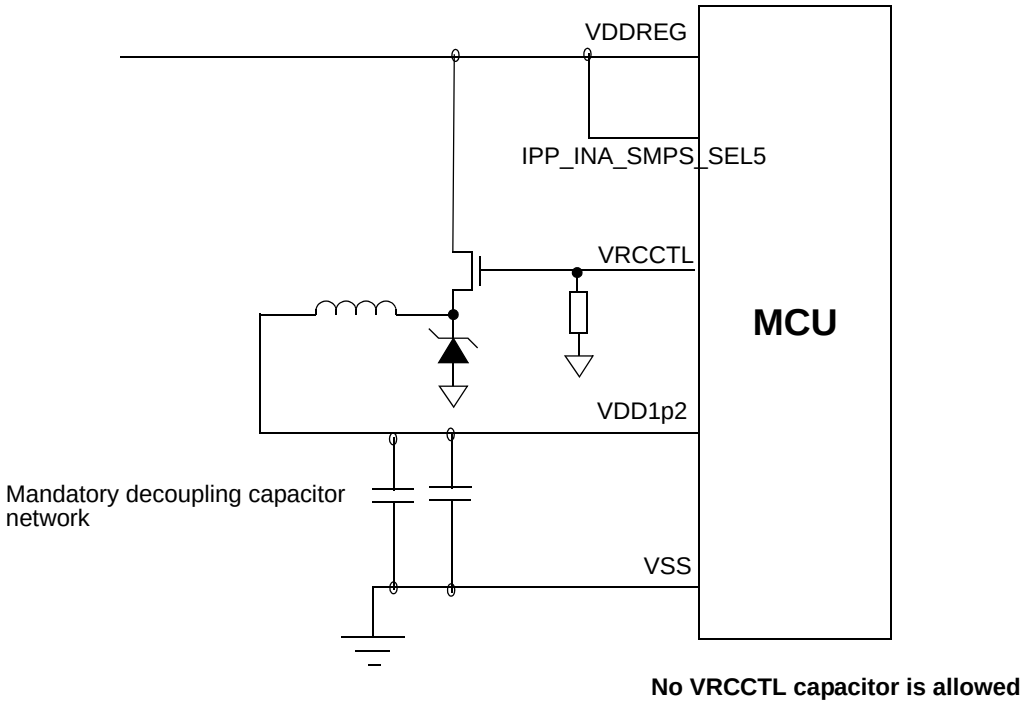



**Figure 6. VRC 1.2V buck SMPS LDO configuration with external MOS - Schottky diode**

**Table 9. VRC LDO recommended external devices**

| Part Name | Part Type | Nominal | Description |
|---|---|---|---|
| NJD2873 | NPN | | ON Semiconductor TM |
| Beta (Bf) | | | From 60 to 550 |
| Vbe | | | From 0.4 V to 1.0 V |
| Vce | | | From 0.2 V to 0.6 V depends on package / power |
| | Capacitor | 6 x 4.7 uF - 20 V | Ceramic low ESR—One for each VDD pin |
| | Capacitor | 6 x 0.1 uF - 20 V | Ceramic —One capacitor for each VDD pin |
| | Capacitor | 20 uF | Supply decoupling cap (close to bipolar collector) |
| | Capacitor | 2.2 uF | Snubber cap, required with NJD2873 (on bipolar base) |
| | Resistor | 12 Ω | Optional ESR for snubber cap |

**Table 15. $V_{DD33}$ Pad Average DC Current[1]**

| Spec | Pad Type | Symbol | Frequency (MHz) | Load[2] (pF) | $V_{DD33}$ (V) | $V_{DDE}$ (V) | Drive/Slew Rate Select | Current (mA) |
|---|---|---|---|---|---|---|---|---|
| 1 | Medium | $I_{33\_MH}$ | — | — | 3.6 | 5.5 | — | 0.0007 |
| 2 | Fast | $I_{33\_FC}$ | 66 | 10 | 3.6 | 3.6 | 00 | 0.92 |
| 3 | | | 66 | 20 | 3.6 | 3.6 | 01 | 1.14 |
| 4 | | | 66 | 30 | 3.6 | 3.6 | 10 | 1.50 |
| 5 | | | 66 | 50 | 3.6 | 3.6 | 11 | 2.19 |
| 6 | | | 66 | 10 | 3.6 | 1.98 | 00 | 0.70 |
| 7 | | | 66 | 20 | 3.6 | 1.98 | 01 | 0.90 |
| 8 | | | 66 | 30 | 3.6 | 1.98 | 10 | 1.08 |
| 9 | | | 66 | 50 | 3.6 | 1.98 | 11 | 1.52 |
| 10 | Fast w/ Slew Control | $I_{33\_FSR}$ | 66 | 50 | 3.6 | 3.6 | 11 | 0.74 |
| 11 | | | 50 | 50 | 3.6 | 3.6 | 10 | 0.52 |
| 12 | | | 33.33 | 50 | 3.6 | 3.6 | 01 | 0.36 |
| 13 | | | 20 | 50 | 3.6 | 3.6 | 00 | 0.19 |
| 14 | | | 20 | 200 | 3.6 | 3.6 | 00 | 0.19 |

1 These are average IDD33 for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

2 All loads are lumped.

## 4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

**Table 16. DSPI LVDS Pad Specification [1, 2]**
**($V_{DD33}$ = 3.0 V to 3.6 V, $V_{DDEH}$ = 4.75 V to 5.25 V, $T_A = T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **Data Rate** | | | | | | |
| 1 | Data Frequency | $f_{LVDSCLK}$ | — | — | 40 | MHz |
| **Driver Specs** | | | | | | |
| 2 | Differential Output Voltage<br>SRC=0b00 or 0b11<br>SRC=0b01<br>SRC=0b10 | $V_{OD}$ | <br>215<br>170<br>260 | — | <br>400<br>320<br>480 | mV |
| 3 | Common Mode Voltage (LVDS), VOS | $V_{OS}$ | 1.075 | 1.2 | 1.325 | V |
| 4 | Rise/Fall Time | $t_R$ or $t_F$ | — | — | 2.5 | ns |
| 5 | Delay, Z to Normal (High/Low) | $t_{DZ}$ | — | — | 100 | ns |

**Table 18. Oscillator Electrical Specifications[1] (continued)**

**($V_{DDSYN}$ = 3.0 V to 3.6 V, $V_{SS}$ = $V_{SSSYN}$ = 0 V, $T_A$ = $T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 7 | Total On-chip stray capacitance on EXTAL | $C_{S\_EXTAL}$ | — | 1.5 | pF |
| 8 | Crystal manufacturer's recommended capacitive load | $C_L$ | See crystal spec | See crystal spec | pF |
| 9 | Discrete load capacitance to be connected to EXTAL | $C_{L\_EXTAL}$ | — | $(2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[4]$)$ | pF |
| 10 | Discrete load capacitance to be connected to XTAL | $C_{L\_XTAL}$ | — | $(2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[4]$)$ | pF |

1 All values given are initial design targets and subject to change.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.

3 $I_{xtal}$ is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

4 $C_{PCB\_EXTAL}$ and $C_{PCB\_XTAL}$ are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

## 4.9 eQADC Electrical Characteristics

**Table 19. eQADC Conversion Specifications (Operating)**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | ADC Clock (ADCLK) Frequency | $f_{ADCLK}$ | 2 | 16 | MHz |
| 2 | Conversion Cycles | CC | 2 + 13 | 128 + 14 | ADCLK cycles |
| 3 | Stop Mode Recovery Time[1] | $T_{SR}$ | 10 | — | µs |
| 4 | Resolution[2] | — | 1.25 | — | mV |
| 5 | INL: 8 MHz ADC Clock[3] | INL8 | –4[4] | 4[4] | LSB[5] |
| 6 | INL: 16 MHz ADC Clock[3] | INL16 | –8[4] | 8[4] | LSB |
| 7 | DNL: 8 MHz ADC Clock[3] | DNL8 | –3[4] | 3[4] | LSB |
| 8 | DNL: 16 MHz ADC Clock[3] | DNL16 | –3[4] | 3[4] | LSB |
| 9 | Offset Error without Calibration | OFFNC | 0[4] | 100[4] | LSB |
| 10 | Offset Error with Calibration | OFFWC | –4[4] | 4[4] | LSB |
| 11 | Full Scale Gain Error without Calibration | GAINNC | –120[4] | 0[4] | LSB |
| 12 | Full Scale Gain Error with Calibration | GAINWC | –4[4,6] | 4[4,6] | LSB |
| 13 | Disruptive Input Injection Current [7, 8, 9, 10] | $I_{INJ}$ | –1 | 1 | mA |
| 14 | Incremental Error due to injection current[11, 12] | $E_{INJ}$ | — | ±4[4] | Counts |
| 15 | TUE value at 8 MHz [13, 14] (with calibration) | TUE8 | — | ±4[4,6] | Counts |

## 4.9.1 ADC Internal Resource Measurements

**Table 20. Power Management Control (PMC) Specification**

| Spec | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **PMC Normal Mode** | | | | | | |
| 1 | Bandgap 0.62 V<br>ADC0 channel 145 | $V_{ADC145}$ | 0.59 | 0.62 | 0.65 | V |
| 2 | Bandgap 1.2 V<br>ADC0 channel 146 | $V_{ADC146}$ | 1.10 | 1.22 | 1.34 | V |
| 3 | Vreg1p2 Feedback<br>ADC0 channel 147 | $V_{ADC147}$ | $V_{DD}$/2.147 | $V_{DD}$ / 2.045 | $V_{DD}$/1.943 | V |
| 4 | LVD 1.2 V<br>ADC0 channel 180 | $V_{ADC180}$ | $V_{DD}$/1.863 | $V_{DD}$ / 1.774 | $V_{DD}$/1.685 | V |
| 5 | Vreg3p3 Feedback<br>ADC0 channel 181 | $V_{ADC181}$ | Vreg3p3 / 5.733— | Vreg3p3 / 5.460 | Vreg3p3 / 5.187 | V |
| 6 | LVD 3.3 V<br>ADC0 channel 182 | $V_{ADC182}$ | Vreg3p3 / 4.996 | Vreg3p3 / 4.758 | Vreg3p3 / 4.520 | V |
| 7 | LVD 5.0 V<br>ADC0 channel 183<br>— LDO mode<br>— SMPS mode | $V_{ADC183}$ | $V_{DDREG}$ / 4.996<br>$V_{DDREG}$ / 7.384 | <br><br>$V_{DDREG}$ / 4.758<br>$V_{DDREG}$/7.032 | $V_{DDREG}$ / 4.520<br>$V_{DDREG}$ / 6.680 | V |

**Table 21. Standby RAM Regulator Electrical Specifications**

| Spec | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Normal Mode** | | | | | | |
| 1 | Standby Regulator Output<br>ADC1 channel 194 | $V_{ADC194}$ | — | 1.2 | — | V |
| 2 | Standby Source Bias<br>ADC1 channel 195 | $V_{ADC195}$ | 150 | — | 360 | mV |

**Table 22. ADC Band Gap Reference / LVI Electrical Specifications**

| Spec | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | 4.75 LVD (from $V_{DDA}$)<br>ADC1 channel 196 | $V_{ADC196}$ | — | 4.75 | — | V |
| 2 | ADC Bandgap<br>ADC0 channel 45<br>ADC1 channel 45 | $V_{ADC45}$ | — | 1.220 | — | V |

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at $V_{DD}$ = 1.08 V to 1.32 V, $V_{DDE}$ = 3.0 V to 3.6 V, $V_{DDEH}$ = 3.0 V to 3.6 V, $V_{DD33}$ and $V_{DDSYN}$ = 3.0 V to 3.6 V, $T_A = T_L$ to $T_H$.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

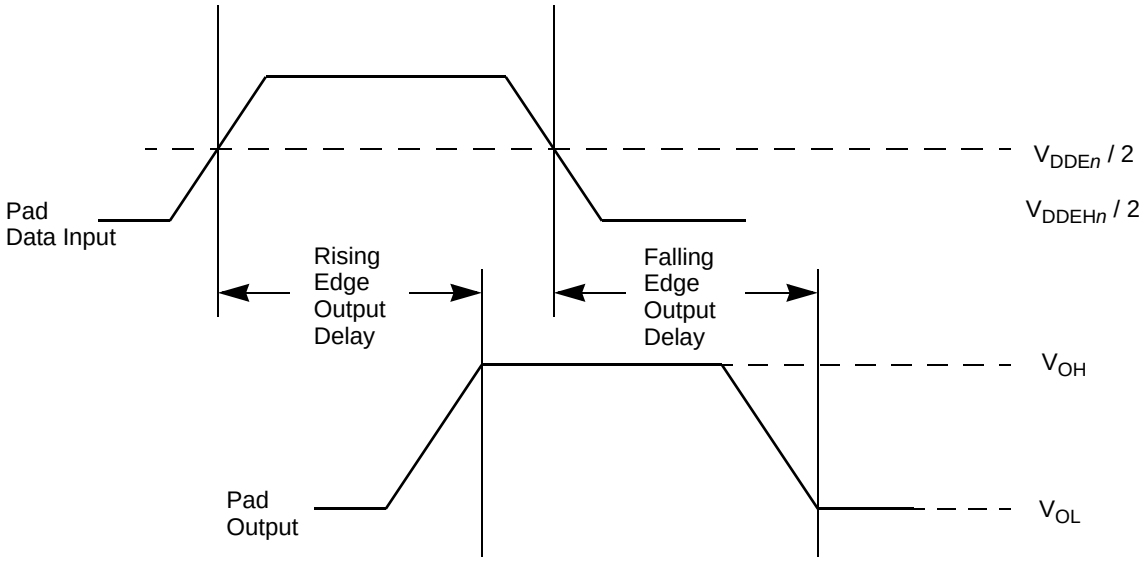



**Figure 7. Pad Output Delay**

## 4.12 AC Timing

### 4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 8 and Figure 9 apply to all I/O pins with pad types F and MH. See Table 39 for the pad type for each pin.

**Table 32. JTAG Pin AC Electrical Characteristics[1] (continued)**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 12 | TCK Falling Edge to Output Valid out of High Impedance | $t_{BSDVZ}$ | — | 50 | ns |
| 13 | TCK Falling Edge to Output High Impedance | $t_{BSDHZ}$ | — | 50 | ns |
| 14 | Boundary Scan Input Valid to TCK Rising Edge | $t_{BSDST}$ | 50 | — | ns |
| 15 | TCK Rising Edge to Boundary Scan Input Invalid | $t_{BSDHT}$ | 50 | — | ns |

1 JTAG timing specified at $V_{DD}$ = 1.08 V to 1.32 V, $V_{DDE}$ = 3.0 V to 3.6 V, $V_{DD33}$ and $V_{DDSYN}$ = 3.0 V to 3.6 V, $T_A = T_L$ to $T_H$, and $C_L$ = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 33 for functional specifications.

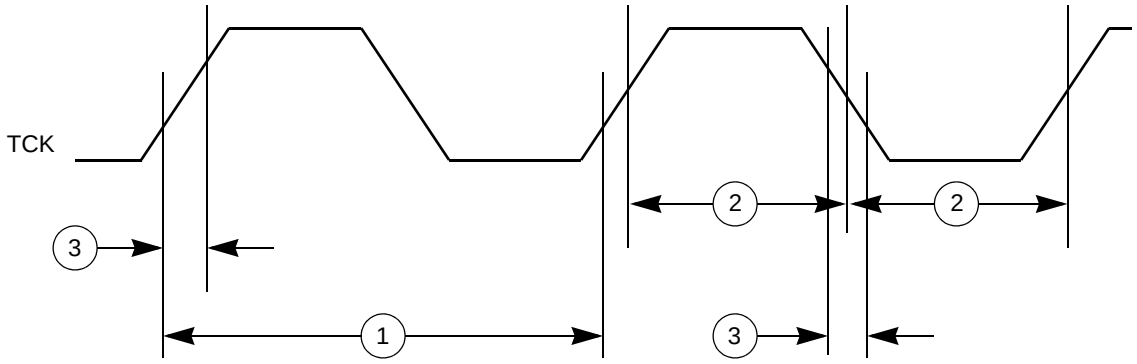



**Figure 11. JTAG Test Clock Input Timing**

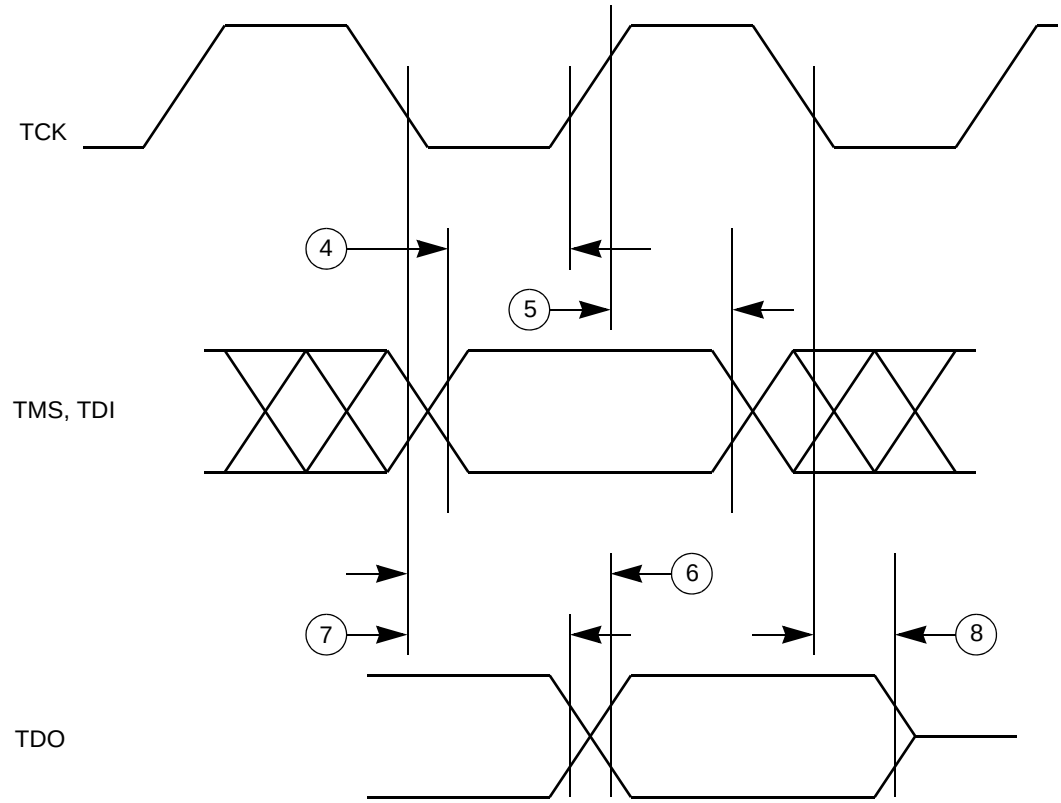



**Figure 12. JTAG Test Access Port Timing**

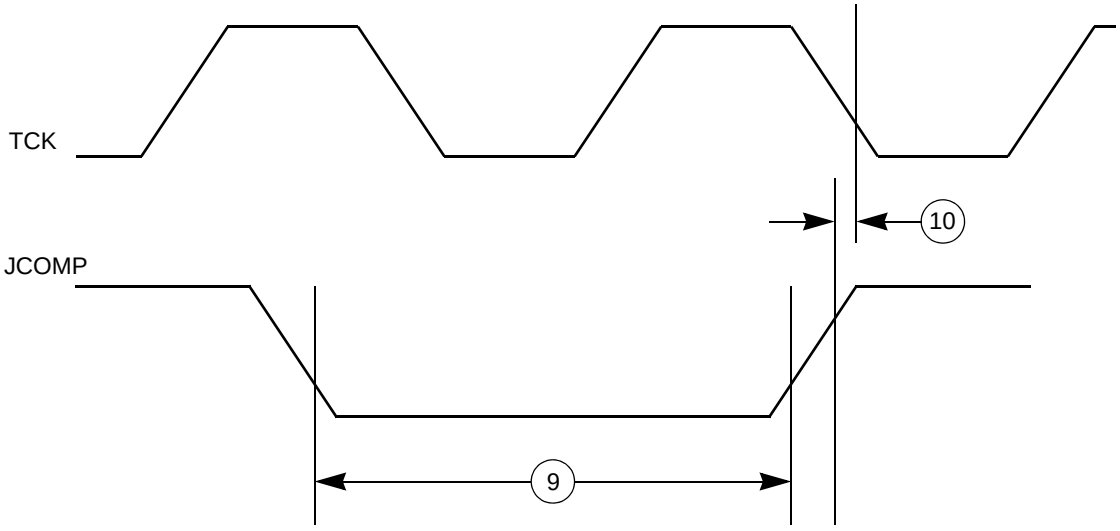



**Figure 13. JTAG JCOMP Timing**

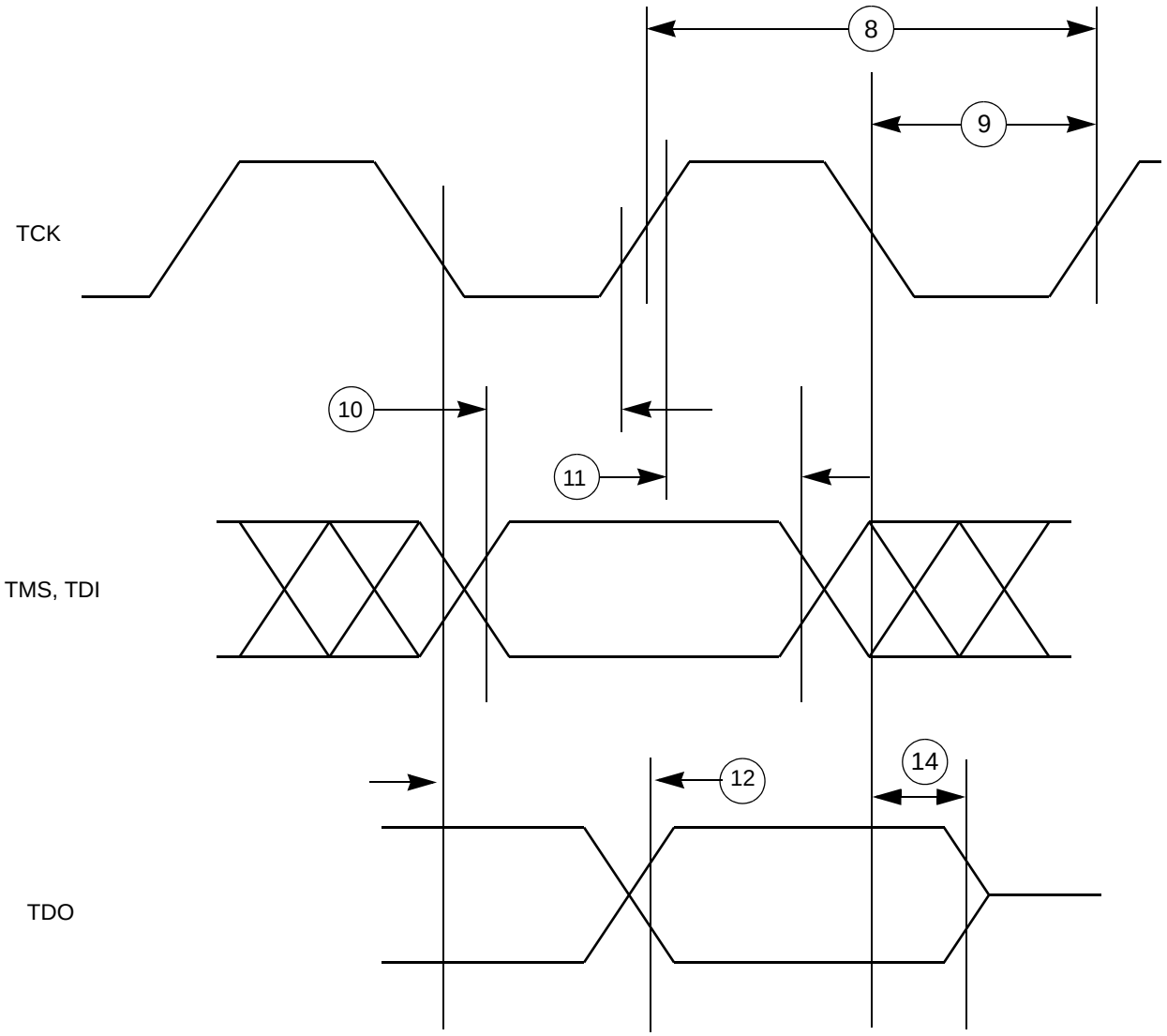



**Figure 16. Nexus TCK, TDI, TMS, TDO Timing**

## 4.12.5 External Bus Interface (EBI) Timing

**Table 34. Bus Operation Timing [1]**

| Spec | Characteristic | Symbol | 66 MHz (Ext. Bus Freq)[2] [3] | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| 1 | D_CLKOUT Period | $t_C$ | 15.2 | — | ns | Signals are measured at 50% $V_{DDE}$. |

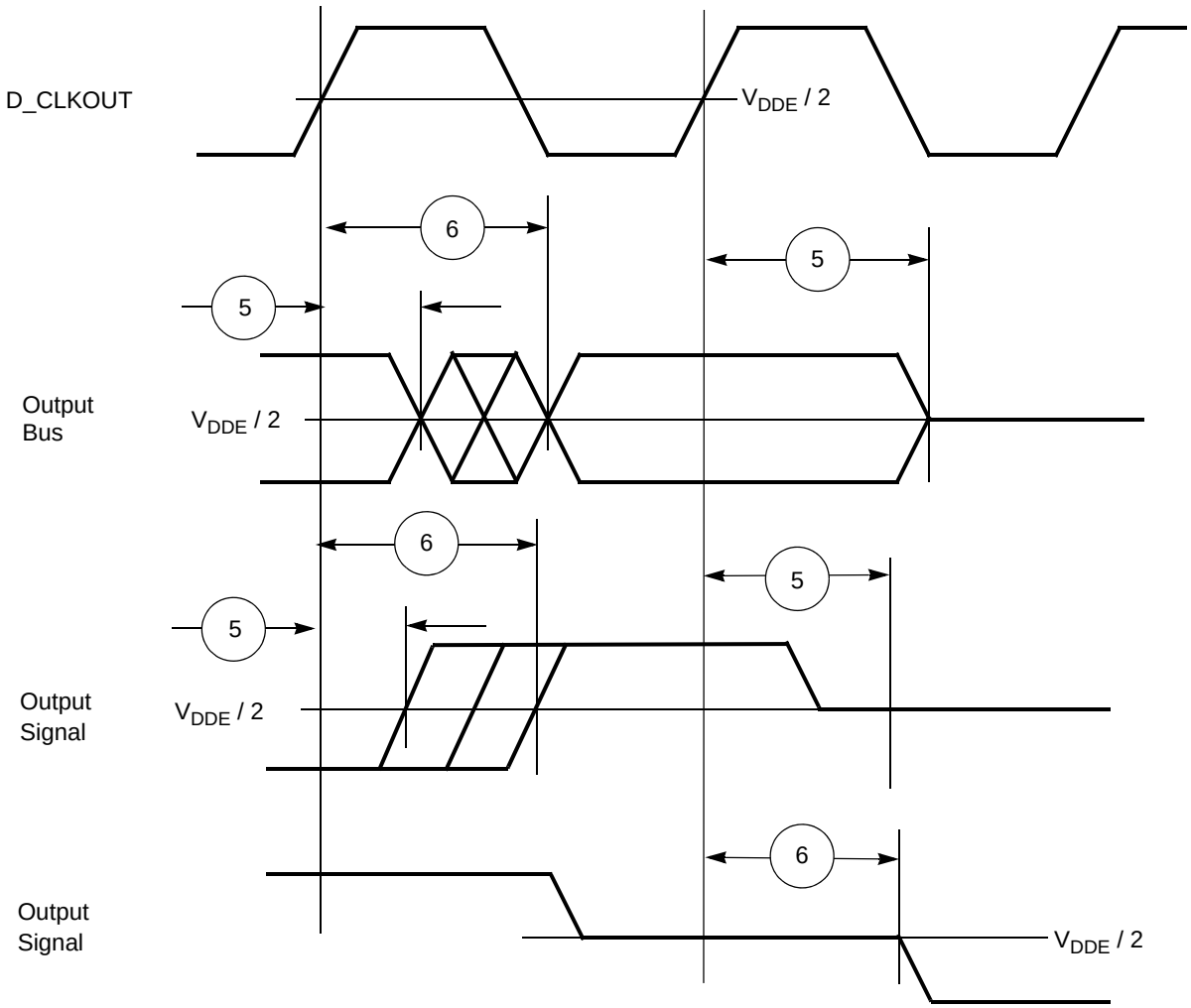



**Figure 18. Synchronous Output Timing**

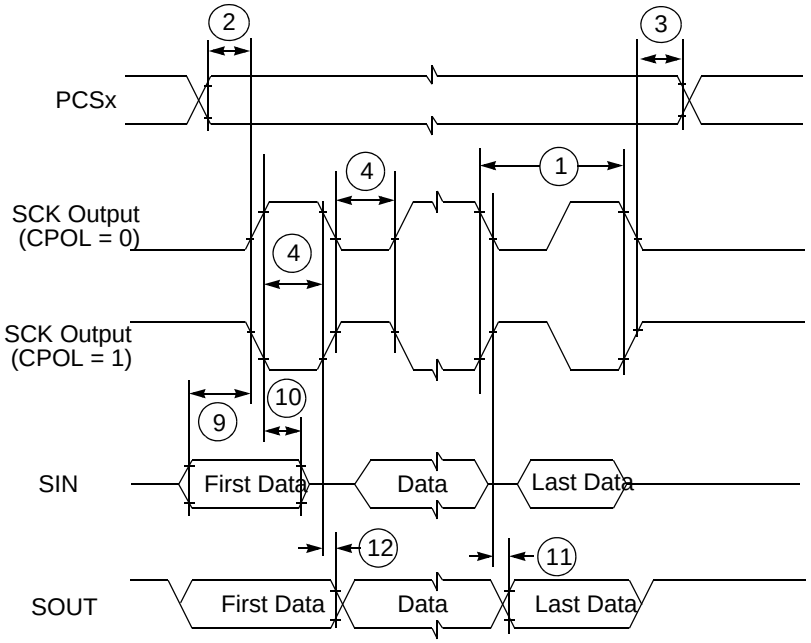



**Figure 24. DSPI Classic SPI Timing — Master, CPHA = 0**

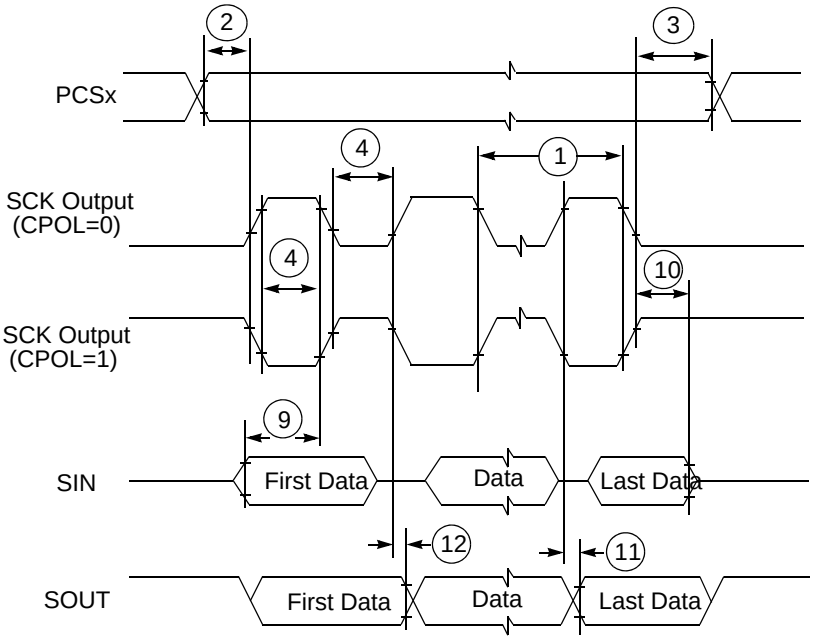



**Figure 25. DSPI Classic SPI Timing — Master, CPHA = 1**

# 5 Package Information

## 5.1 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 33 and Figure 34.

**Figure 33. 416 TEPBGA Package (1 of 2)**

Figure 36. 516 TEPBGA Package (2 of 2)

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 196 | EMIOS17_ETPUB1_ GPIO196 | P | EMIOS17 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AE15 | AB15 |
| | | A1 | ETPUB1 | eTPU B channel | O | | | | | | |
| | | A2 | FR_DBG[2] | FlexRay debug | O | | | | | | |
| | | G | GPIO196 | GPIO | I/O | | | | | | |
| 197 | EMIOS18_ETPUB2_ GPIO197 | P | EMIOS18 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AC15 | AD17 |
| | | A1 | ETPUB2 | eTPU B channel | O | | | | | | |
| | | A2 | FR_DBG[1] | FlexRay debug | O | | | | | | |
| | | G | GPIO197 | GPIO | I/O | | | | | | |
| 198 | EMIOS19_ETPUB3_ GPIO198 | P | EMIOS19 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AD15 | AB16 |
| | | A1 | ETPUB3 | eTPU B channel | O | | | | | | |
| | | A2 | FR_DBG[0] | FlexRay debug | O | | | | | | |
| | | G | GPIO198 | GPIO | I/O | | | | | | |
| 199 | EMIOS20_ETPUB4_ GPIO199 | P | EMIOS20 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AF16 | AF16 |
| | | A1 | ETPUB4 | eTPU B channel | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO199 | GPIO | I/O | | | | | | |
| 200 | EMIOS21_ETPUB5_ GPIO200 | P | EMIOS21 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AE16 | AE17 |
| | | A1 | ETPUB5 | eTPU B channel | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO200 | GPIO | I/O | | | | | | |
| 201 | EMIOS22_ETPUB6_ GPIO201 | P | EMIOS22 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AC16 | AC16 |
| | | A1 | ETPUB6 | eTPU B channel | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO201 | GPIO | I/O | | | | | | |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 104 | SOUTB_ GPIO104 | P | SOUTB | DSPI B data output | O | MH | $V_{DDEH3}$ | —/Up | —/Up | AF9 | AA10 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO104 | GPIO | I/O | | | | | | |
| 105 | PCSB0_PCSD2_ GPIO105 | P | PCSB0 | DSPI B peripheral chip select | I/O | MH | $V_{DDEH3}$ | —/Up | —/Up | AD9 | AF8 |
| | | A1 | PCSD2 | DSPI D peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO105 | GPIO | I/O | | | | | | |
| 106 | PCSB1_PCSD0_ GPIO106 | P | PCSB1 | DSPI B peripheral chip select | O | MH | $V_{DDEH3}$ | —/Up | —/Up | AC9 | AE8 |
| | | A1 | PCSD0 | DSPI D peripheral chip select | I/O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO106 | GPIO | I/O | | | | | | |
| 107 | PCSB2_SOUTC_ GPIO107 | P | PCSB2 | DSPI B peripheral chip select | O | MH | $V_{DDEH3}$ | —/Up | —/Up | AF8 | AD8 |
| | | A1 | SOUTC | DSPI C data output | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO107 | GPIO | I/O | | | | | | |
| 108 | PCSB3_SINC_ GPIO108 | P | PCSB3 | DSPI B peripheral chip select | O | MH | $V_{DDEH3}$ | —/Up | —/Up | AD10 | AC9 |
| | | A1 | SINC | DSPI C data input | I | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO108 | GPIO | I/O | | | | | | |
| 109 | PCSB4_SCKC_ GPIO109 | P | PCSB4 | DSPI B peripheral chip select | O | MH | $V_{DDEH3}$ | —/Up | —/Up | AC8 | AF7 |
| | | A1 | SCKC | DSPI C clock | I/O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO109 | GPIO | I/O | | | | | | |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 82 | MDO11_GPIO82 | –[12] | MDO11[14] | Nexus message data out | O | F | $V_{DDE2}$ | O/Low | —/Down | Y3 | Y4 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO82 | GPIO | I/O | | | | | | |
| 231 | MDO12_GPIO231 | –[12] | MDO12[14] | Nexus message data out | O | F | $V_{DDE2}$ | O/Low | —/Down | AA1 | Y5 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO231 | GPIO | I/O | | | | | | |
| 232 | MDO13_GPIO232 | –[12] | MDO13[14] | Nexus message data out | O | F | $V_{DDE2}$ | O/Low | —/Down | AA2 | AA1 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO232 | GPIO | I/O | | | | | | |
| 233 | MDO14_GPIO233 | –[12] | MDO14[14] | Nexus message data out | O | F | $V_{DDE2}$ | O/Low | —/Down | AA3 | AA2 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO233 | GPIO | I/O | | | | | | |
| 234 | MDO15_GPIO234 | –[12] | MDO15[14] | Nexus message data out | O | F | $V_{DDE2}$ | O/Low | —/Down | Y4 | AA3 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO234 | GPIO | I/O | | | | | | |
| 224 | $\overline{\text{MSEO0}}$ | –[12] | MSEO0[14] | Nexus message start/end out | O | F | $V_{DDE2}$ | O/Low | MSEO/HI | U2 | U6 |
| 225 | $\overline{\text{MSEO1}}$ | –[12] | MSEO1[14] | Nexus message start/end out | O | F | $V_{DDE2}$ | O/Low | MSEO/HI | T3 | U5 |
| 226 | RDY | –[12] | RDY | Nexus ready output | O | F | $V_{DDE2}$ | O/Low | RDY/HI | R4 | U3 |
| — | TCK | –[12] | TCK | JTAG test clock input | I | F | $V_{DDE2}$ | TCK/Down | TCK/Down | AB2 | AB2 |
| — | TDI | –[12] | TDI | JTAG test data input | I | F | $V_{DDE2}$ | TDI/Up | TDI/Up | AC2 | AC2 |
| 228 | TDO | –[12] | TDO | JTAG test data output | O | F | $V_{DDE2}$ | TDO/Up | TDO/Up | AB1 | AB1 |
| — | TMS | –[12] | TMS | JTAG test mode select input | I | F | $V_{DDE2}$ | TMS/Up | TMS/Up | AB3 | AB3 |