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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z7 |
| Core Size | 32-Bit Dual-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, SCI, SPI |
| Peripherals | DMA, POR, PWM |
| Number of I/O | - |
| Program Memory Size | 6MB (6M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 1.32V |
| Data Converters | A/D 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5676rdk3mvy1 |

# Table of Contents

# 3 Pin Assignments

## 3.1 416-ball TEPBGA Pin Assignments

Figure 3 shows the 416-ball TEPBGA pin assignments.

**CAUTION**

This ball map is preliminary and subject to change. Do not use it for board design.

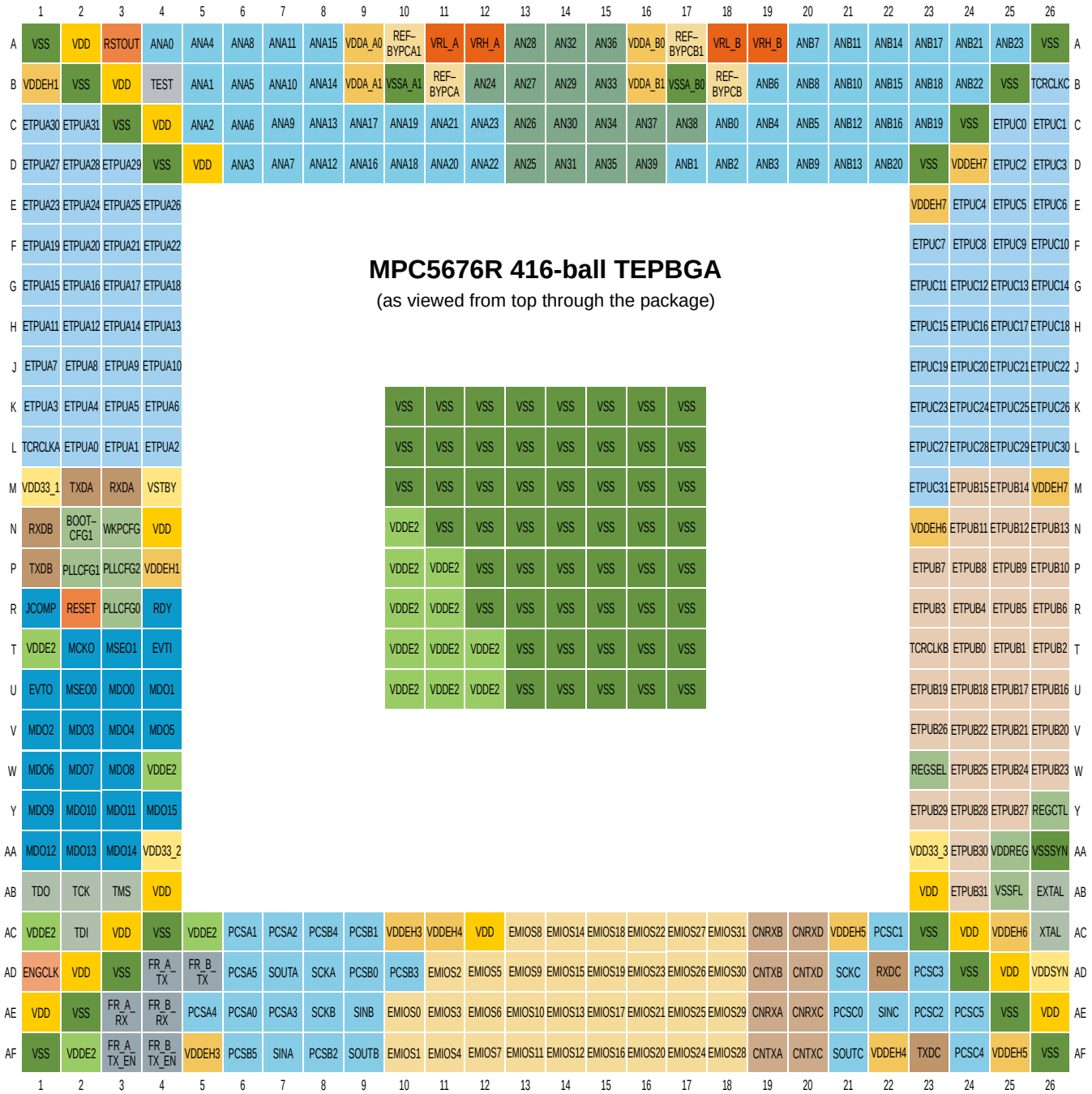


**Figure 3. MPC5676R 416-ball TEPBGA (full diagram)**

## 3.3 Pin Muxing and Reset States

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

# 4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5676R.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

## 4.1 Maximum Ratings

**Table 2. Absolute Maximum Ratings[1]**

| Spec | Characteristic | Symbol | Min | Max[2] | Unit |
|---|---|---|---|---|---|
| 1 | 1.2 V Core Supply Voltage[3] | $V_{DD}$ | –0.3 | 1.65 [4] | V |
| 2 | SRAM Standby Voltage | $V_{STBY}$ | –0.3 | 5.5 [5,6] | V |
| 3 | Clock Synthesizer Voltage | $V_{DDSYN}$ | –0.3 | 4.5 [6,7] | V |
| 4 | I/O Supply Voltage (I/O buffers and predrivers) | $V_{DD33}$ | –0.3 | 4.5 [6,7] | V |
| 5 | Analog Supply Voltage (reference to $V_{SSA}$[8]) | $V_{DDA}$[9] | –0.3 | 5.5 [5,6] | V |
| 6 | I/O Supply Voltage (fast I/O pads) | $V_{DDE}$ | –0.3 | 4.5 [6] | V |
| 7 | I/O Supply Voltage (medium I/O pads) | $V_{DDEH}$ | –0.3 | 5.5 [5,6] | V |
| 8 | Voltage Regulator Input Supply Voltage | $V_{DDREG}$ | –0.3 | 5.5[5,6] | V |
| 9 | Analog Reference High Voltage (reference to $V_{RL}$[10]) | $V_{RH}$[11] | –0.3 | 5.5 [5,6] | V |
| 10 | $V_{SS}$ to $V_{SSA}$[8] Differential Voltage | $V_{SS} – V_{SSA}$ | –0.1 | 0.1 | V |
| 11 | $V_{REF}$ Differential Voltage | $V_{RH} – V_{RL}$ | –0.3 | 5.5 [5,6] | V |
| 12 | $V_{RL}$ to $V_{SSA}$ Differential Voltage | $V_{RL} – V_{SSA}$ | –0.3 | 0.3 | V |
| 13 | $V_{DD33}$ to $V_{DDSYN}$ Differential Voltage | $V_{DD33} – V_{DDSYN}$ | –0.1 | 0.1 | V |
| 14 | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage | $V_{SSSYN} – V_{SS}$ | –0.1 | 0.1 | V |
| 15 | Maximum Digital Input Current [12] (per pin, applies to all digital pins) | $I_{MAXD}$ | –3 [13] | 3 [13] | mA |
| 16 | Maximum Analog Input Current [14] (per pin, applies to all analog pins) | $I_{MAXA}$ | –3 [9,13] | 3 [9,13] | mA |

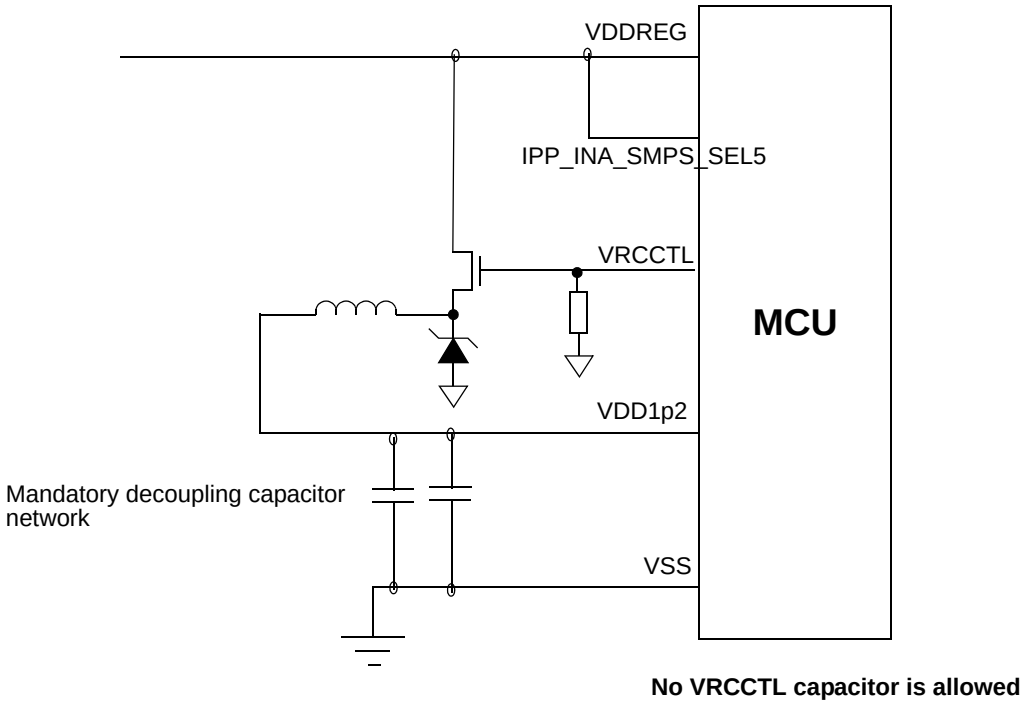


**Figure 6. VRC 1.2V buck SMPS LDO configuration with external MOS - Schottky diode**

**Table 9. VRC LDO recommended external devices**

| Part Name | Part Type | Nominal | Description |
|---|---|---|---|
| NJD2873 | NPN | | ON Semiconductor TM |
| Beta (Bf) | | | From 60 to 550 |
| Vbe | | | From 0.4 V to 1.0 V |
| Vce | | | From 0.2 V to 0.6 V depends on package / power |
| | Capacitor | 6 x 4.7 uF - 20 V | Ceramic low ESR—One for each VDD pin |
| | Capacitor | 6 x 0.1 uF - 20 V | Ceramic —One capacitor for each VDD pin |
| | Capacitor | 20 uF | Supply decoupling cap (close to bipolar collector) |
| | Capacitor | 2.2 uF | Snubber cap, required with NJD2873 (on bipolar base) |
| | Resistor | 12 Ω | Optional ESR for snubber cap |

**Table 10. VRC SMPS recommended external devices**

| Part Name | Part Type | Nominal | Description |
|---|---|---|---|
| IR7353 | HS nMOS + Schottky | | Low threshold n-MOS/Low Vf Schottky diode |
| SS8P3L | Schottky | | Low Vf Schottky diode |
| Vf | | | From 0.4V to 0.6 V |
| SI3460 or equivalent | nMOS | | Low threshold n-MOS |
| Vth | | | Less than 2 V |
| Ids | | | More than 1.5 A |
| Vds | | | More than 12 V |
| Rdson | | | Less than 100 Ohms |
| Cg | | | Less than 5 nF |
| Turn on / off delay | | | Less than 50 ns |
| Rise time | | | Less than 90 ns |
| LQH66SN2R2M03 | inductor | 2.2 uH—3.2 A | muRata TM shielded coil, preferred $f_{max}$ > 40 MHz |
| C3225X7R1E106M | capacitor | 22 uF — 25 V | TDK high capacitance ceramic SMD (on VDD close to coil) |
| C3225X7R1E225K | capacitor | 2 to 6 x 2.2 uF — 25 V | TDK ceramic SMD (on VDD close to MCU) |
| | capacitor | 6 x 0.1 uF — 20 V | Ceramic -One capacitor for each VDD pin |
| C3225X7R1E106M | capacitor | 22 uF — 25 V | Supply decoupling cap—close to n-MOS drain |
| | resistor | 20 K | Pull down for power n—MOS gate |

## 4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each $V_{DDE}/V_{DDEH}$ first and then power up $V_{DD}$. For power down, drop $V_{DD}$ to 0 V first, and then drop all $V_{DDE}/V_{DDEH}$ supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 11 and Table 12.

There are no limits on the fall times for the power supplies.

### 4.6.3 Power Sequencing and POR Dependent on $V_{DDA}$

During power up or down, $V_{DDA}$ can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between $V_{DDA}$ and $V_{DDEH}$ is more than 1 V, the following will result:

- Triggers POR (ADC monitors on $V_{DDEH1}$ segment which powers the RESET pin) if the leakage current path created, when $V_{DDA}$ is sufficiently low, causes sufficient voltage drop on $V_{DDEH1}$ node monitored crosses low-voltage detect level.
- If $V_{DDA}$ is between 0–2 V, powering all the other segments (especially $V_{DDEH1}$) will not be sufficient to get the part out of reset.
- Each $V_{DDEH}$ will have a leakage current to $V_{DDA}$ of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V). .
- Each $V_{DD}$ has the same behavior; however, the leakage will be small even though there is no current limiting resistor since $V_{DD} = 1.32$ V max.

## 4.7 DC Electrical Specifications

**Table 13. DC Electrical Specifications[1]**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Core Supply Voltage (External Regulation) | $V_{DD}$ | 1.14 | 1.32[2, 3] | V |
| 1a | Core Supply Voltage (Internal Regulation)[4] | $V_{DD}$ | 1.08 | 1.32 | V |
| 2 | I/O Supply Voltage (fast I/O pads) | $V_{DDE}$ | 3.0 | 3.6[2] | V |
| 3 | I/O Supply Voltage (medium I/O pads) | $V_{DDEH}$ | 3.0 | 5.25[2] | V |
| 4 | 3.3 V I/O Buffer Voltage | $V_{DD33}$ | 3.0 | 3.6[2] | V |
| 5 | Analog Supply Voltage | $V_{DDA}$ | 4.75 | 5.25[2] | V |
| 6a | SRAM Standby Voltage low range | $V_{STBY\_LOW}$ | 0.95[5] | 1.2 | V |
| 6b | SRAM Standby Voltage high range | $V_{STBY\_HIGH}$ | 2 | 6 | V |
| 7 | Voltage Regulator Control Input Voltage[6] | $V_{DDREG}$ | 2.7[7] | 5.5[2] | V |
| 8 | Clock Synthesizer Operating Voltage[8] | $V_{DDSYN}$ | 3.0 | 3.6[2] | V |
| 9 | Fast I/O Input High Voltage<br>Hysteresis enabled<br>Hysteresis disabled | $V_{IH\_F}$ | <br>0.65 × $V_{DDE}$<br>0.55 × $V_{DDE}$ | $V_{DDE}$ + 0.3 | V |
| 10 | Fast I/O Input Low Voltage<br>Hysteresis enabled<br>Hysteresis disabled | $V_{IL\_F}$ | $V_{SS}$ – 0.3 | <br>0.35 × $V_{DDE}$<br>0.40 × $V_{DDE}$ | V |
| 11 | Medium I/O Input High Voltage<br>Hysteresis enabled<br>Hysteresis disabled | $V_{IH\_S}$ | <br>0.65 × $V_{DDEH}$<br>0.55 × $V_{DDEH}$ | $V_{DDEH}$ + 0.3 | V |

**Table 19. eQADC Conversion Specifications (Operating) (continued)**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 16 | TUE value at 16 MHz [13, 14] (with calibration) | TUE16 | — | ±8 | Counts |
| 17 | Variable gain amplifier accuracy (gain=1)[15]<br>INL, 8 MHz ADC<br>INL, 16 MHz ADC<br>DNL, 8 MHz ADC<br>DNL, 16 MHz ADC | GAINVGA1 | <br>–4<br>–8<br>$-3^{16}$<br>$-3^{16}$ | <br>4<br>8<br>$3^{16}$<br>$3^{16}$ | Counts[17] |
| 18 | Variable gain amplifier accuracy (gain=2)[15]<br>INL, 8 MHz ADC<br>INL, 16 MHz ADC<br>DNL, 8 MHz ADC<br>DNL, 16 MHz ADC | GAINVGA2 | <br>–5<br>–8<br>–3<br>–3 | <br>5<br>8<br>3<br>3 | Counts |
| 19 | Variable gain amplifier accuracy (gain=4)[15]<br>INL, 8 MHz ADC<br>INL, 16 MHz ADC<br>DNL, 8 MHz ADC<br>DNL, 16 MHz ADC | GAINVGA4 | <br>–7<br>–8<br>–4<br>–4 | <br>7<br>8<br>4<br>4 | Counts |

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} - V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from $V_{RL}$ + 50 LSB to $V_{RH}$ – 50 LSB.

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than $V_{RH}$ and $000 for values less than $V_{RL}$. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}$=$I_{INJMAX}$,$I_{INJMIN}$.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

16 Guaranteed 10-bit mono tonicity.

17 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

**Table 25. Flash Memory AC Timing Specifications[1]**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{RES}$ | Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low | — | — | 100 | ns |
| $T_{DONE}$ | Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared | — | — | 5 | ns |
| $T_{PSRT}$ | Time between program suspend resume and the next program suspend request.[2] | 100 | — | — | µs |
| $T_{ESRT}$ | Time between erase suspend resume and the next erase suspend request.[3] | 10 | — | — | ms |

1 This parameter is guaranteed by characterization before qualification rather than 100% tested.

2 Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does notoccur is $T_{PSRT}$.

3 If Erase suspend rate is less than $T_{ESRT}$, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

**Table 26. Flash EEPROM Module Life**

| Spec | Characteristic | Symbol | Min | Typical[1] | Unit |
|---|---|---|---|---|---|
| 1 | Number of Program/Erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range ($T_J$) | P/E | 100,000 | — | cycles |
| 2 | Number of Program/Erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range ($T_J$) | P/E | 1,000 | 100,000 | cycles |
| 3 | Minimum Data Retention at 85 °C ambient temperature[2]<br>Blocks with 0–1,000 P/E cycles<br>Blocks with 1,001–10,000 P/E cycles<br>Blocks with 10,001–100,000 P/E cycles | Retention | <br>20<br>10<br>1 – 5 | — | years |

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the NXP definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

## 4.11.2 Pad AC Specifications

**Table 29. Pad AC Specifications ($V_{DDEH}$ = 5.0 V, $V_{DDE}$ = 3.3 V)[1]**

| Spec | Pad | SRC/DSC | Out Delay[2,4] L → H/H → L (ns) | Rise/Fall[3,4] (ns) | Load Drive (pF) |
|---|---|---|---|---|---|
| 1 | Medium[5] | 00 | 152/165 | 70/74 | 50 |
| 2 | | | 205/220 | 96/96 | 200 |
| 3 | | 01 | 28/34 | 12/15 | 50 |
| 4 | | | 52/59 | 28/31 | 200 |
| 5 | | 11 | 12/12 | 5.3/5.9 | 50 |
| 6 | | | 32/32 | 22/22 | 200 |
| 7 | Fast[6] | 00 | 2.5 | 1.2 | 10 |
| 8 | | 01 | | | 20 |
| 9 | | 10 | | | 30 |
| 10 | | 11 | | | 50 |
| 11 | Fast with Slew Rate | 00 | 40/40 | 16/16 | 50 |
| 12 | | | 50/50 | 21/21 | 200 |
| 13 | | 01 | 13/13 | 5/5 | 50 |
| 14 | | | 19/19 | 8/8 | 200 |
| 15 | | 10 | 8/8 | 2.4/2.4 | 50 |
| 16 | | | 12/12 | 5/5 | 200 |
| 17 | | 11 | 5/5 | 1.1/1/1 | 50 |
| 18 | | | 8/8 | 2.6 | 200 |
| 19 | Pull Up/Down (3.6 V max) | — | — | 7500 | 50 |
| 20 | Pull Up/Down (5.25 V max) | — | 6000 | 5000/5000 | 50 |

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at $V_{DD}$ = 1.02 V to 1.32 V, $V_{DDE}$ = 3.0 V to 3.6 V, $V_{DDEH}$ = 4.75 V to 5.25 V, $V_{DD33}$ and $V_{DDSYN}$ = 3.0 V to 3.6 V, $T_A = T_L$ to $T_H$.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

**Table 30. Derated Pad AC Specifications ($V_{DDEH}$ = 3.3 V)[1]**

| Spec | Pad | SRC/DSC | Out Delay[2,3] L → H/H → L (ns) | Rise/Fall[4,3] (ns) | Load Drive (pF) |
|---|---|---|---|---|---|
| 1 | Medium[5] | 00 | 200/210 | 86/86 | 50 |
| 2 | | | 270/285 | 120/120 | 200 |
| 3 | | 01 | 37/45 | 15.5/19 | 50 |
| 4 | | | 69/82 | 38/43 | 200 |
| 5 | | 11 | 18/17 | 7.6/8.5 | 50 |
| 6 | | | 46/49 | 30/34 | 200 |

**Table 32. JTAG Pin AC Electrical Characteristics[1] (continued)**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 12 | TCK Falling Edge to Output Valid out of High Impedance | $t_{BSDVZ}$ | — | 50 | ns |
| 13 | TCK Falling Edge to Output High Impedance | $t_{BSDHZ}$ | — | 50 | ns |
| 14 | Boundary Scan Input Valid to TCK Rising Edge | $t_{BSDST}$ | 50 | — | ns |
| 15 | TCK Rising Edge to Boundary Scan Input Invalid | $t_{BSDHT}$ | 50 | — | ns |

1 JTAG timing specified at $V_{DD}$ = 1.08 V to 1.32 V, $V_{DDE}$ = 3.0 V to 3.6 V, $V_{DD33}$ and $V_{DDSYN}$ = 3.0 V to 3.6 V, $T_A = T_L$ to $T_H$, and $C_L$ = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 33 for functional specifications.

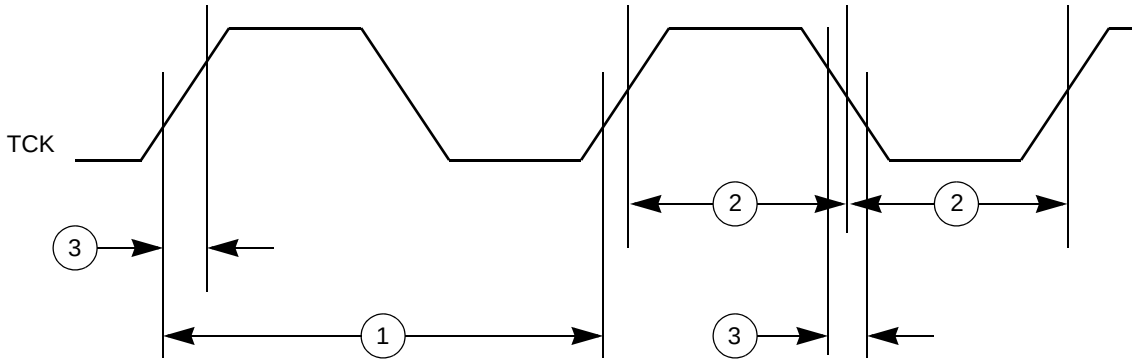


**Figure 11. JTAG Test Clock Input Timing**

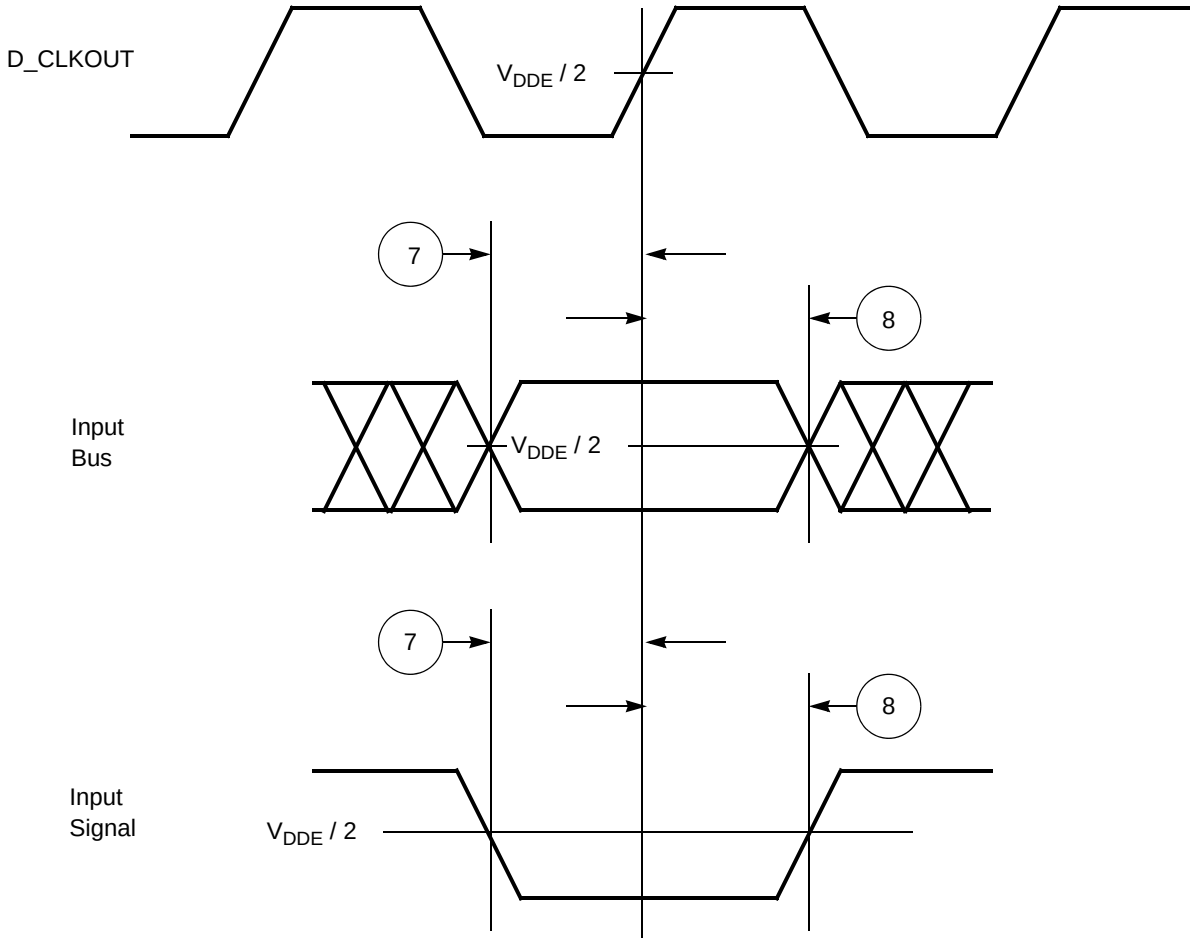


**Figure 19. Synchronous Input Timing**

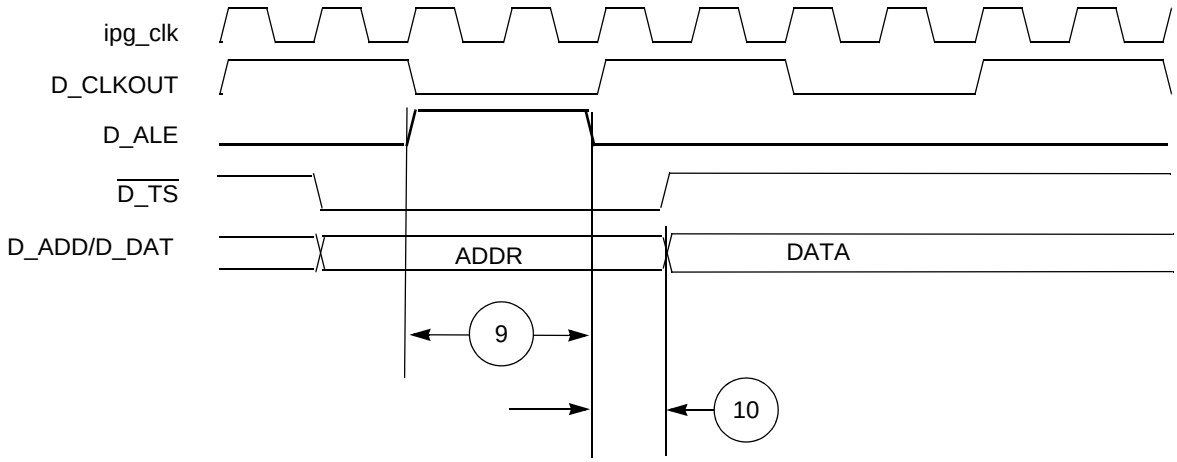


**Figure 20. ALE Signal Timing**

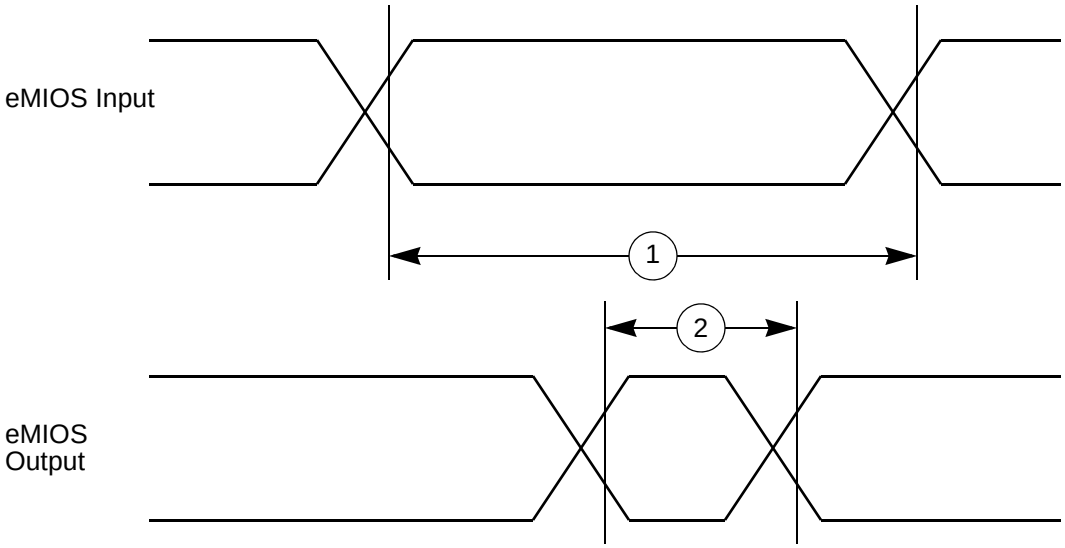


**Figure 23. eMIOS Timing**

## 4.12.9 DSPI Timing

**Table 38. DSPI Timing[1,2]**

| Spec | Characteristic | Symbol | Peripheral Bus Freq: 92 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | DSPI Cycle Time[3, 4]<br>Master (MTFE = 0)<br>Slave (MTFE = 0)<br>Master (MTFE = 1)<br>Slave (MTFE = 1) | $t_{SCK}$ | 23.8 | 1800 | ns |
| 2 | PCS to SCK Delay[5] | $t_{CSC}$ | 12 | — | ns |
| 3 | After SCK Delay[6] | $t_{ASC}$ | 12 | — | ns |
| 4 | SCK Duty Cycle | $t_{SDC}$ | 0.4 * $t_{SCK}$ | 0.6 * $t_{SCK}$ | ns |
| 5 | Slave Access Time<br>($\overline{SS}$ active to SOUT valid) | $t_A$ | — | 25 | ns |
| 6 | Slave SOUT Disable Time<br>($\overline{SS}$ inactive to SOUT High-Z or invalid) | $t_{DIS}$ | — | 25 | ns |
| 7 | PCS*x* to $\overline{PCSS}$ time | $t_{PCSC}$ | 4 | — | ns |
| 8 | $\overline{PCSS}$ to PCS*x* time | $t_{PASC}$ | 5 | — | ns |

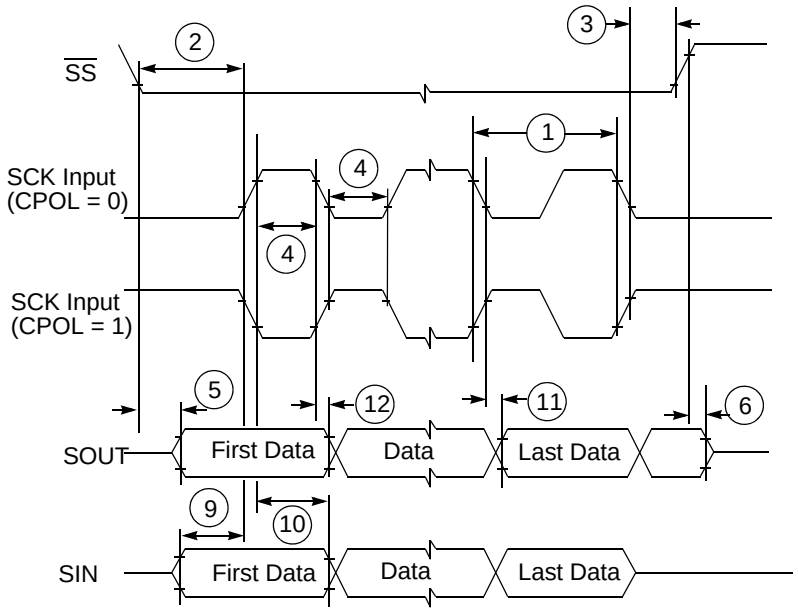


**Figure 26. DSPI Classic SPI Timing — Slave, CPHA = 0**

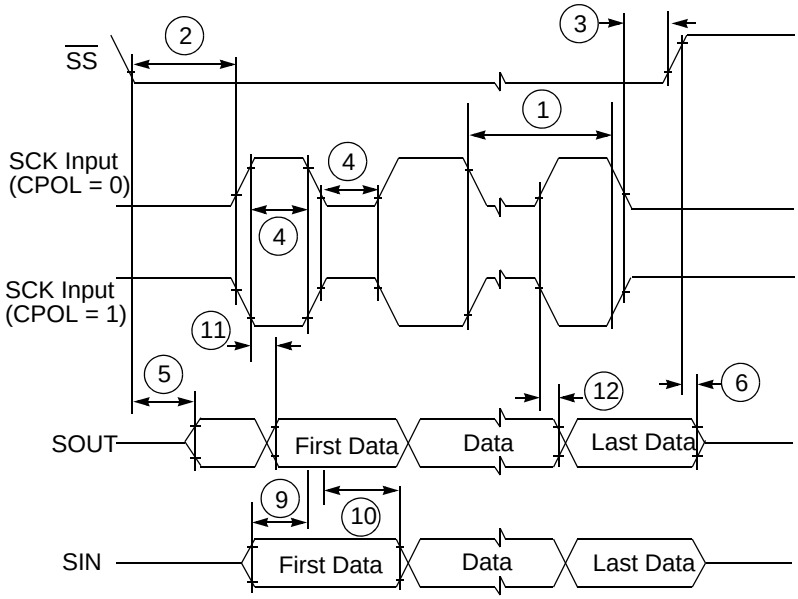


**Figure 27. DSPI Classic SPI Timing — Slave, CPHA = 1**

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location 416 | Package Location 516 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145 | ETPUA31_PCSC4_ GPIO145 | P | ETPUA31 | eTPU A channel | I/O | MH | $V_{DDEH1}$ | —/WKPCFG | —/WKPCFG | C2 | C2 |
| | | A1 | PCSC4 | DSPI C peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO145 | GPIO | I/O | | | | | | |
| **eTPU_B** | | | | | | | | | | | |
| 146 | TCRCLKB_IRQ6_ GPIO146 | P | TCRCLKB | eTPU B TCR clock | I | MH | $V_{DDEH6}$ | —/Up | —/Up | T23 | V25 |
| | | A1 | IRQ6 | External interrupt request | I | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO146 | GPIO | I/O | | | | | | |
| 147 | ETPUB0_ETPUB16_ GPIO147 | P | ETPUB0 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | T24 | V26 |
| | | A1 | ETPUB16 | eTPU B channel (output only) | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO147 | GPIO | I/O | | | | | | |
| 148 | ETPUB1_ETPUB17_ GPIO148 | P | ETPUB1 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | T25 | U22 |
| | | A1 | ETPUB17 | eTPU B channel (output only) | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO148 | GPIO | I/O | | | | | | |
| 149 | ETPUB2_ETPUB18_ GPIO149 | P | ETPUB2 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | T26 | U23 |
| | | A1 | ETPUB18 | eTPU B channel (output only) | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO149 | GPIO | I/O | | | | | | |
| 150 | ETPUB3_ETPUB19_ GPIO150 | P | ETPUB3 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | R23 | T22 |
| | | A1 | ETPUB19 | eTPU B channel (output only) | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO150 | GPIO | I/O | | | | | | |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 163 | ETPUB16_PCSA1_ GPIO163 | P | ETPUB16 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | U26 | V24 |
| | | A1 | PCSA1 | DSPI A peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO163 | GPIO | I/O | | | | | | |
| 164 | ETPUB17_PCSA2_ GPIO164 | P | ETPUB17 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | U25 | T21 |
| | | A1 | PCSA2 | DSPI A peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO164 | GPIO | I/O | | | | | | |
| 165 | ETPUB18_PCSA3_ GPIO165 | P | ETPUB18 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | U24 | W26 |
| | | A1 | PCSA3 | DSPI A peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO165 | GPIO | I/O | | | | | | |
| 166 | ETPUB19_PCSA4_ GPIO166 | P | ETPUB19 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | U23 | W25 |
| | | A1 | PCSA4 | DSPI A peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO166 | GPIO | I/O | | | | | | |
| 167 | ETPUB20_ GPIO167 | P | ETPUB20 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | V26 | W24 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO167 | GPIO | I/O | | | | | | |
| 168 | ETPUB21_ GPIO168 | P | ETPUB21 | eTPU B channel | I/O | MH | $V_{DDEH6}$ | —/WKPCFG | —/WKPCFG | V25 | V22 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO168 | GPIO | I/O | | | | | | |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location 416 | Package Location 516 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 435 | EMIOS29_PCSC1_ GPIO435 | P | EMIOS29 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AE18 | AB17 |
| | | A1 | PCSC1 | DSPI C peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO435 | GPIO | I/O | | | | | | |
| 436 | EMIOS30_PCSC2_ GPIO436 | P | EMIOS30 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AD18 | AF19 |
| | | A1 | PCSC2 | DSPI C peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO436 | GPIO | I/O | | | | | | |
| 437 | EMIOS31_PCSC5_ GPIO437 | P | EMIOS31 | eMIOS channel | I/O | MH | $V_{DDEH4}$ | —/WKPCFG | —/WKPCFG | AC18 | AA17 |
| | | A1 | PCSC5 | DSPI C peripheral chip select | O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO437 | GPIO | I/O | | | | | | |
| **eQADC** | | | | | | | | | | | |
| — | ANA0 | P | ANA0[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA0 | ANA0 | A4 | A4 |
| — | ANA1 | P | ANA1[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA1 | ANA1 | B5 | B5 |
| — | ANA2 | P | ANA2[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA2 | ANA2 | C5 | C5 |
| — | ANA3 | P | ANA3[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA3 | ANA3 | D6 | D6 |
| — | ANA4 | P | ANA4[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA4 | ANA4 | A5 | A5 |
| — | ANA5 | P | ANA5[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA5 | ANA5 | B6 | B6 |
| — | ANA6 | P | ANA6[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA6 | ANA6 | C6 | C6 |
| — | ANA7 | P | ANA7[9] | eQADC A shared analog input | I | AE/up-down | $V_{DDA\_A1}$ | ANA7 | ANA7 | D7 | C7 |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| — | AN35 | P | AN35 | eQADC analog input | I | AE | $V_{DDA\_B0}$ | AN35 | AN35 | D15 | D15 |
| — | AN36 | P | AN36 | eQADC analog input | I | AE | $V_{DDA\_B1}$ | AN36 | AN36 | A15 | A15 |
| — | AN37 | P | AN37 | eQADC analog input | I | AE | $V_{DDA\_B0}$ | AN37 | AN37 | C16 | C17 |
| — | AN38 | P | AN38 | eQADC analog input | I | AE | $V_{DDA\_B0}$ | AN38 | AN38 | C17 | D16 |
| — | AN39 | P | AN39 | eQADC analog input | I | AE | $V_{DDA\_B0}$ | AN39 | AN39 | D16 | C16 |
| — | ANB0 | P | ANB0 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB0 | ANB0 | C18 | C18 |
| — | ANB1 | P | ANB1 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB1 | ANB1 | D17 | D17 |
| — | ANB2 | P | ANB2 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB2 | ANB2 | D18 | D18 |
| — | ANB3 | P | ANB3 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB3 | ANB3 | D19 | D19 |
| — | ANB4 | P | ANB4 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB4 | ANB4 | C19 | B19 |
| — | ANB5 | P | ANB5 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB5 | ANB5 | C20 | A20 |
| — | ANB6 | P | ANB6 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB6 | ANB6 | B19 | C20 |
| — | ANB7 | P | ANB7 | eQADC B shared analog input | I | AE/up-down | $V_{DDA\_B0}$ | ANB7 | ANB7 | A20 | C19 |
| — | ANB8 | P | ANB8 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB8 | ANB8 | B20 | B20 |
| — | ANB9 | P | ANB9 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB9 | ANB9 | D20 | A21 |
| — | ANB10 | P | ANB10 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB10 | ANB10 | B21 | B21 |
| — | ANB11 | P | ANB11 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB11 | ANB11 | A21 | C21 |
| — | ANB12 | P | ANB12 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB12 | ANB12 | C21 | A22 |
| — | ANB13 | P | ANB13 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB13 | ANB13 | D21 | B22 |
| — | ANB14 | P | ANB14 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB14 | ANB14 | A22 | D20 |
| — | ANB15 | P | ANB15 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB15 | ANB15 | B22 | C22 |
| — | ANB16 | P | ANB16 | eQADC B analog input | I | AE | $V_{DDA\_B0}$ | ANB16 | ANB16 | C22 | D21 |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 240 | PCSC2_GPIO240 | P | PCSC2 | DSPI C peripheral chip select | O | MH | $V_{DDEH5}$ | —/Up | —/Up | AE23 | AE23 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO240 | GPIO | I/O | | | | | | |
| 241 | PCSC3_GPIO241 | P | PCSC3 | DSPI C peripheral chip select | O | MH | $V_{DDEH5}$ | —/Up | —/Up | AD23 | AD23 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO241 | GPIO | I/O | | | | | | |
| 242 | PCSC4_GPIO242 | P | PCSC4 | DSPI C peripheral chip select | O | MH | $V_{DDEH5}$ | —/Up | —/Up | AF24 | AF24 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO242 | GPIO | I/O | | | | | | |
| 243 | PCSC5_GPIO243 | P | PCSC5 | DSPI C peripheral chip select | O | MH | $V_{DDEH5}$ | —/Up | —/Up | AE24 | AE24 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO243 | GPIO | I/O | | | | | | |
| **EBI** | | | | | | | | | | | |
| 256 | D_CS0_ GPIO256 | P | D_CS0 | EBI chip select 0 | O | F | $V_{DDE9}$ | —/Up | —/Up | — | AD9 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO256 | GPIO | I/O | | | | | | |
| 257 | D_CS2_D_ADD_DAT31_ GPIO257 | P | D_CS2 | EBI chip select 2 | O | F | $V_{DDE8}$ | —/Up | —/Up | — | U1 |
| | | A1 | D_ADD_DAT31 | Address and data in mux mode. | I/O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO257 | GPIO | I/O | | | | | | |

**Table 39. Signal Properties and Muxing Summary (continued)**

| GPIO/PCR[1] | Signal Name[2] | P/A/G[3] | Function[4] | Function Summary | Direction | Pad Type[5] | Voltage[6] | State during RESET[7] | State after RESET[8] | Package Location | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 416 | 516 |
| 258 | D_CS3_D_TEA_ GPIO258 | P | D_CS3 | EBI chip select 3 | O | F | $V_{DDE8}$ | —/Up | —/Up | — | T6 |
| | | A1 | D_TEA | EBI transfer error acknowledge | I/O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO258 | GPIO | I/O | | | | | | |
| 259 | D_ADD12_ GPIO259 | P | D_ADD12 | EBI address bus | O | F | $V_{DDE8}$ | —/Up | —/Up | — | R1 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO259 | GPIO | I/O | | | | | | |
| 260 | D_ADD13_ GPIO260 | P | D_ADD13 | EBI address bus | O | F | $V_{DDE8}$ | —/Up | —/Up | — | R2 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO260 | GPIO | I/O | | | | | | |
| 261 | D_ADD14_ GPIO261 | P | D_ADD14 | EBI address bus | O | F | $V_{DDE8}$ | —/Up | —/Up | — | R3 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO261 | GPIO | I/O | | | | | | |
| 262 | D_ADD15_ GPIO262 | P | D_ADD15 | EBI address bus | O | F | $V_{DDE8}$ | —/Up | —/Up | — | R4 |
| | | A1 | — | — | — | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO262 | GPIO | I/O | | | | | | |
| 263 | D_ADD16_D_ADD_DAT16_ GPIO263 | P | D_ADD16 | EBI address bus | O | F | $V_{DDE8}$ | —/Up | —/Up | — | R5 |
| | | A1 | D_ADD_DAT16 | Address and data in mux mode. | I/O | | | | | | |
| | | A2 | — | — | — | | | | | | |
| | | G | GPIO263 | GPIO | I/O | | | | | | |

# Appendix B Revision History

Table 40 describes the changes made to this document between revisions.

**Table 40. Revision History**

| Revision | Date | Description |
|---|---|---|
| Rev 1 | 5 Aug 2011 | Initial customer release |
| Rev 2 | 21 Dec 2011 | Added information about specs 1a through 1d in the PMC Electrical Specifications table.<br><br>Updated the footnote reference (changed from [13] to [14]) of spec 18 of the PMC Electrical Specifications table.<br><br>Updated the Operating Current 5.0 V Supplies @ fsys = 180MHz VDDA Max value (changed from 30 to 50).<br><br>Updated footnote [1] of the VDD33 Pad Average DC Current table (changed IDDE to IDD33).<br><br>Updated the pF value of 11 SRC/DSC Fast with Slew Rate (changed from 2.6 to 200) in the Pad AC Specifications (VDDEH = 5.0 V, VDDE = 3.3 V) table.<br><br>Added a footnote for ANA0-ANA7 ([9]) functions in the “Signal Properties and Muxing Summary” table.<br><br>Added a footnote for MDO0-MDO15 ([14]) and MSEO0 functions in the “Signal Properties and Muxing Summary” table.<br><br>Updated figure numbers 25, 27, 29, and 31: Added specs 1-4.<br><br>Changed the title of the “PFCPR1 Settings” table to “BIUCR1/BIUCR3”.<br><br>Added a new row “Load” under “Termination” in the “DSPI LVDS Pad Specification” table.<br><br>Updated the “Max” and “Typical” values of “Delay, Z to Normal”, “Rise/Fall Time”, and “Data Frequency” in the “DSPI LVDS Pad Specification” table.<br><br>Changed “$V_{DDE}$” to “$V_{DDEH}$” in footnote [10] of the “DC Electrical Specifications” table.<br><br>Made the following changes in the “DSPI Timing” table:<br>• Update the minimum peripheral bus frequencies for “Data Setup Time for Inputs” and “Data Hold Time for Outputs”.<br>• Updated the maximum peripheral bus frequencies for “Data Valid (after SCK edge)”.<br>• Added “Master (LVDS)” information for “Data Valid (after SCK edge)” and “Data Hold Time for Outputs”.<br><br>Changed the minimum voltage value of the “I/O Supply Voltage (fast I/O pads)” from “1.62 V” to “3.0 V” in the “DC Electrical Specifications” table.<br><br>Changed “$V_{DDE}$” values from “1.62 V to 1.98 V” to “3.0 V to 3.6 V” in footnote [1] of the “Pad AC Specifications ($V_{DDEH}$ = 5.0 V, $V_{DDE}$ = 3.3 V)” table.<br><br>Removed voltage ranges “1.62 V–1.98 V” and “2.25 V–2.75 V” from “Fast I/O Weak Pull Up/Down Current” in the “DC Electrical Specifications” table. |