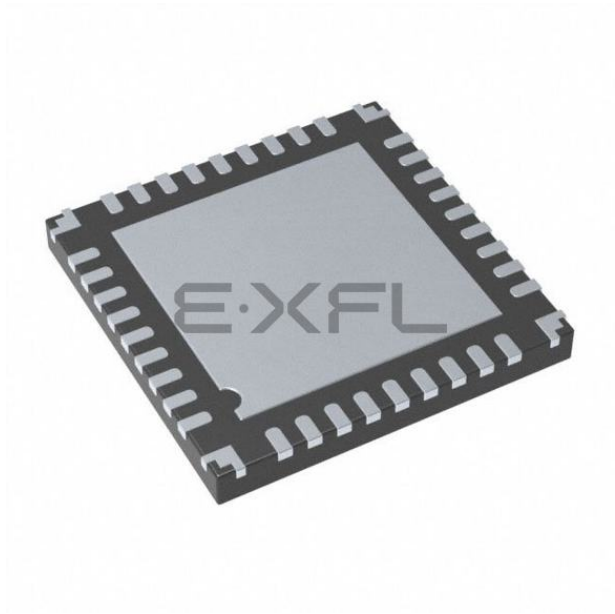

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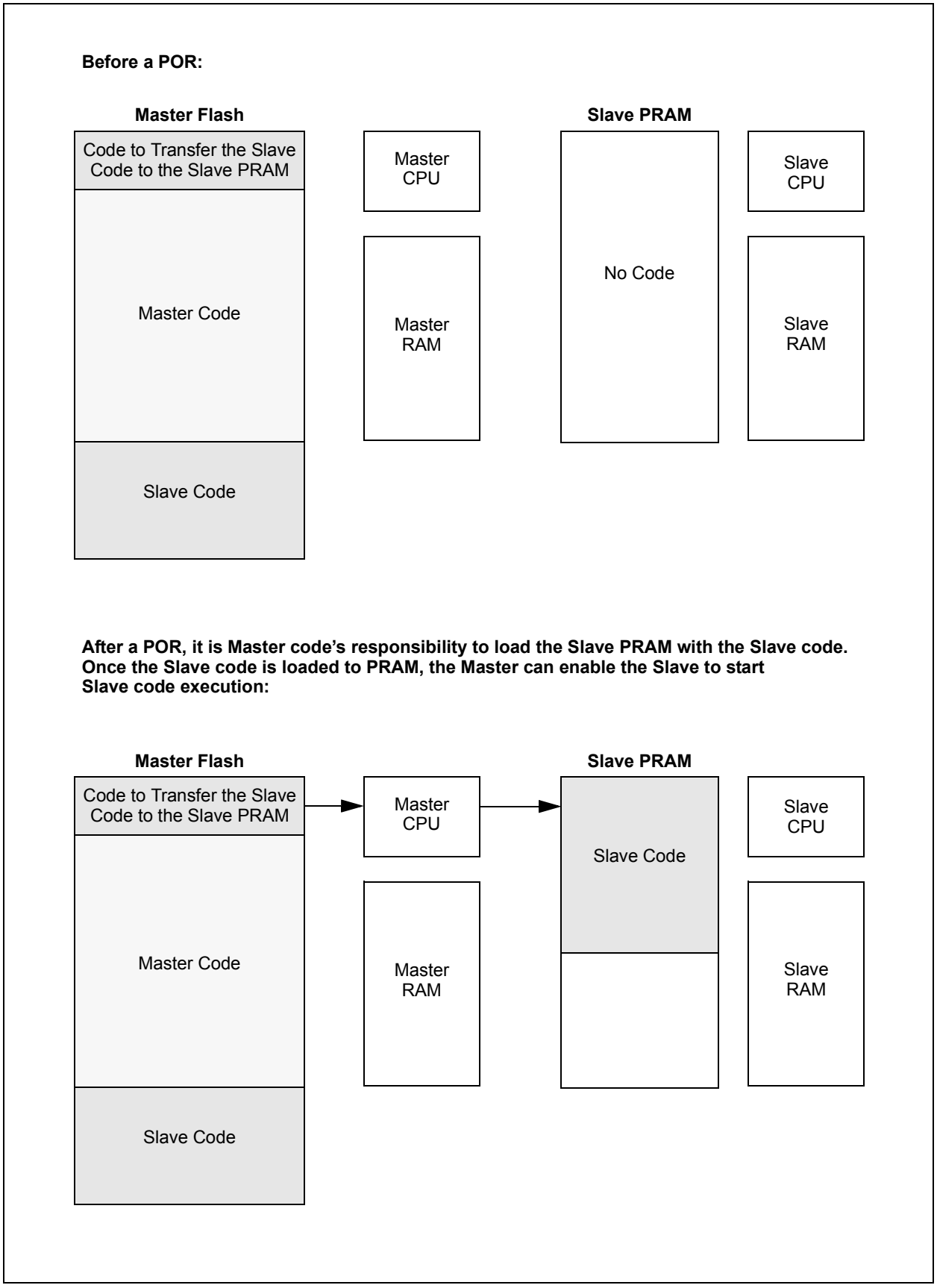
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit Dual-Core |
| Speed | 180MHz, 200MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT |
| Number of I/O | 27 |
| Program Memory Size | 152KB (152K x 8) |
| Program Memory Type | FLASH, PRAM |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 31x12b; D/A 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-UFQFN Exposed Pad |
| Supplier Device Package | 36-UQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp203-e-m5 |

**FIGURE 1-1: SLAVE CORE CODE TRANSFER BLOCK DIAGRAM**



#### 3.2.1.1 Program Memory Organization

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 3-5).

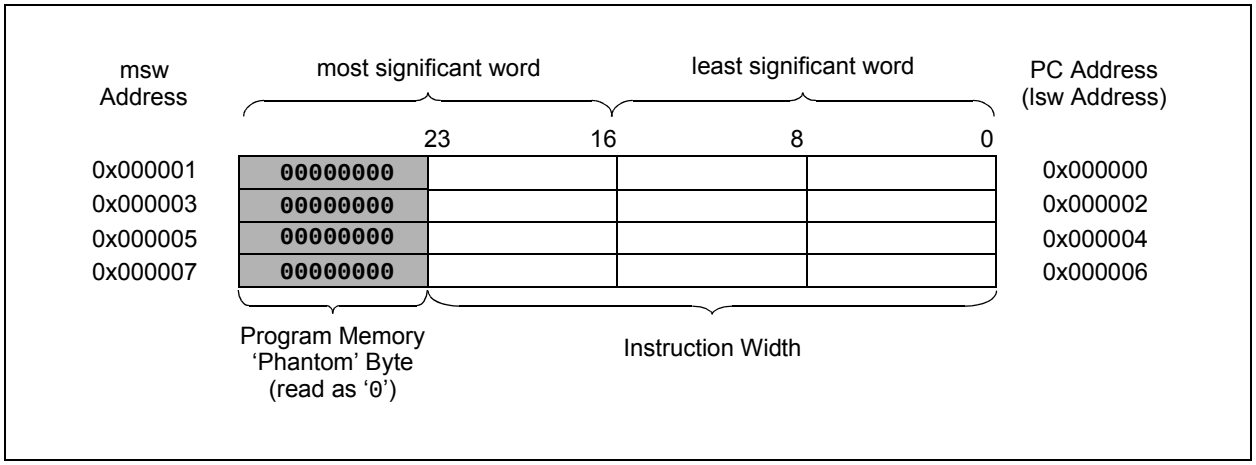
Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented, by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

#### 3.2.1.2 Interrupt and Trap Vectors

All dsPIC33CH128MP508 family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 3.5 "Master Interrupt Controller"**.

**FIGURE 3-5: PROGRAM MEMORY ORGANIZATION**




### 3.2.2 UNIQUE DEVICE IDENTIFIER (UDID)

All dsPIC33CH128MP508 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

The UDID is stored in five read-only locations, located between 0x801200 and 0x801208 in the device configuration space. Table 3-3 lists the addresses of the identifier words and shows their contents

**TABLE 3-3: UDID ADDRESSES**

| UDID | Address | Description |
|---|---|---|
| UDID1 | 0x801200 | UDID Word 1 |
| UDID2 | 0x801202 | UDID Word 2 |
| UDID3 | 0x801204 | UDID Word 3 |
| UDID4 | 0x801206 | UDID Word 4 |
| UDID5 | 0x801208 | UDID Word 5 |

### 3.2.7 MODULO ADDRESSING

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

#### 3.2.7.1 Start and End Address

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 3-4).

| **Note:** | Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear). |
|---|---|

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

#### 3.2.7.2 W Address Register Selection

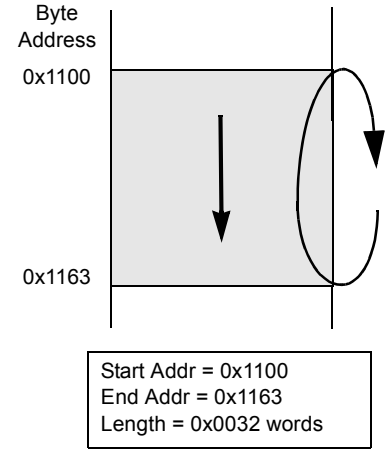
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W (XWM) register, to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 3.2.1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W (YWM) register, to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit (MODCON<14>) is set.

**FIGURE 3-10: MODULO ADDRESSING OPERATION EXAMPLE**




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

**FIGURE 3-11: BIT-REVERSED ADDRESSING EXAMPLE**

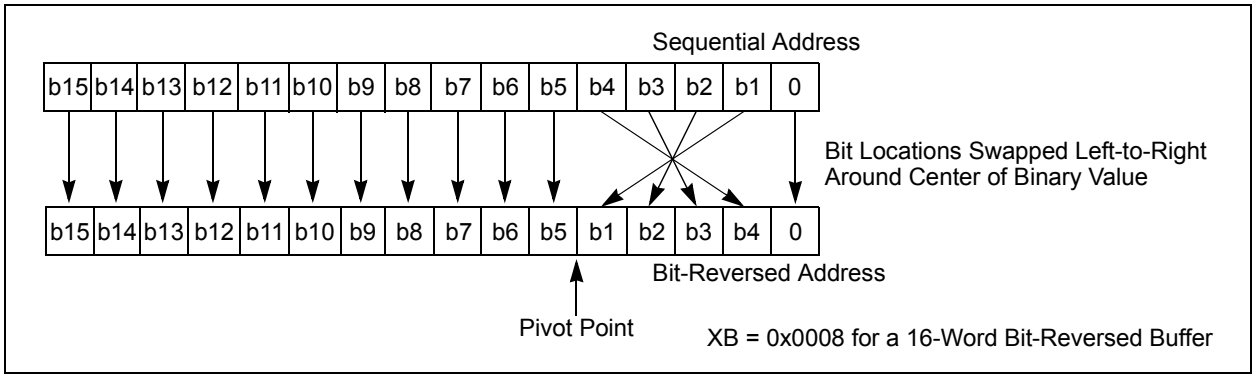



**TABLE 3-21: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)**

| Normal Address | | | | | Bit-Reversed Address | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **A3** | **A2** | **A1** | **A0** | **Decimal** | **A3** | **A2** | **A1** | **A0** | **Decimal** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 0 | 4 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 14 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 | 3 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 1 | 0 | 14 | 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 15 |

**REGISTER 3-134: C1FIFOCONLx: CAN FIFO CONTROL REGISTER x (x = 1 TO 7) LOW (CONTINUED)**

bit 2 **TFERFFIE:** Transmit/Receive FIFO Empty/Full Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Empty Interrupt Enable
1 = Interrupt is enabled for FIFO empty
0 = Interrupt is disabled for FIFO empty

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Full Interrupt Enable
1 = Interrupt is enabled for FIFO full
0 = Interrupt is disabled for FIFO full

bit 1 **TFHRFHIE:** Transmit/Receive FIFO Half Empty/Half Full Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Half Empty Interrupt Enable
1 = Interrupt is enabled for FIFO half empty
0 = Interrupt is disabled for FIFO half empty

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Half Full Interrupt Enable
1 = Interrupt is enabled for FIFO half full
0 = Interrupt is disabled for FIFO half full

bit 0 **TFNRFNIE:** Transmit/Receive FIFO Not Full/Not Empty Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Not Full Interrupt Enable
1 = Interrupt is enabled for FIFO not full
0 = Interrupt is disabled for FIFO not full

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Not Empty Interrupt Enable
1 = Interrupt is enabled for FIFO not empty
0 = Interrupt is disabled for FIFO not empty

**Note 1:** This bit can only be modified in Configuration mode (OPMOD<2:0> = 100).

**REGISTER 3-174: ADIEL: ADC INTERRUPT ENABLE REGISTER LOW**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IE<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **IE<15:0>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

**REGISTER 3-175: ADIEH: ADC INTERRUPT ENABLE REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | IE<20:16> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **IE<20:16>:** Common Interrupt Enable bits
1 = Common and individual interrupts are enabled for the corresponding channel
0 = Common and individual interrupts are disabled for the corresponding channel

**REGISTER 3-183: PTGCST: PTG CONTROL/STATUS LOW REGISTER (CONTINUED)**

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Operation Selection bit(1)

11 = Single-level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 3)

10 = Single-level detect with Step delay executed on exit of command (Mode 2)

01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 1)

00 = Continuous edge detect with Step delay executed on exit of command (Mode 0)

**Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.

**2:** This bit is only used with the PTGCTRL Step command software trigger option.

**3:** The PTGSSEN bit may only be written when in Debug mode.

**TABLE 4-9: SLAVE SFR BLOCK 900h**

| Register | Address | All Resets | Register | Address | All Resets | Register | Address | All Resets |
|---|---|---|---|---|---|---|---|---|
| **CCP** | | | CCP2STATL | 980 | -----0--00xx0000 | CCP3RAL | 9B0 | 0000000000000000 |
| CCP1CON1L | 950 | 0-00000000000000 | CCP2STATH | 982 | ----------00000 | CCP3RBL | 9B4 | 0000000000000000 |
| CCP1CON1H | 952 | 00--000000000000 | CCP2TMRL | 984 | 0000000000000000 | CCP3BUFL | 9B8 | 0000000000000000 |
| CCP1CON2L | 954 | 00-0----00000000 | CCP2TMRH | 986 | 0000000000000000 | CCP3BUFH | 9BA | 0000000000000000 |
| CCP1CON2H | 956 | 0------100-00000 | CCP2PRL | 988 | 1111111111111111 | CCP4CON1L | 9BC | 0-00000000000000 |
| CCP1CON3H | 95A | 0000------0-00-- | CCP2PRH | 98A | 1111111111111111 | CCP4CON1H | 9BE | 00--000000000000 |
| CCP1STATL | 95C | -----0--00xx0000 | CCP2RAL | 98C | 0000000000000000 | CCP4CON2L | 9C0 | 00-0----00000000 |
| CCP1STATH | 95E | ----------00000 | CCP2RBL | 990 | 0000000000000000 | CCP4CON2H | 9C2 | 0------100-00000 |
| CCP1TMRL | 960 | 0000000000000000 | CCP2BUFL | 994 | 0000000000000000 | CCP4CON3H | 9C6 | 0000------0-00-- |
| CCP1TMRH | 962 | 0000000000000000 | CCP2BUFH | 996 | 0000000000000000 | CCP4STATL | 9C8 | -----0--00xx0000 |
| CCP1PRL | 964 | 1111111111111111 | CCP3CON1L | 998 | 0-00000000000000 | CCP4STATH | 9CA | ----------00000 |
| CCP1PRH | 966 | 1111111111111111 | CCP3CON1H | 99A | 00--000000000000 | CCP4TMRL | 9CC | 0000000000000000 |
| CCP1RAL | 968 | 0000000000000000 | CCP3CON2L | 99C | 00-0----00000000 | CCP4TMRH | 9CE | 0000000000000000 |
| CCP1RBL | 96C | 0000000000000000 | CCP3CON2H | 99E | 0------100-00000 | CCP4PRL | 9D0 | 1111111111111111 |
| CCP1BUFL | 970 | 0000000000000000 | CCP3CON3H | 9A2 | 0000------0-00-- | CCP4PRH | 9D2 | 1111111111111111 |
| CCP1BUFH | 972 | 0000000000000000 | CCP3STATL | 9A4 | -----0--00xx0000 | CCP4RAL | 9D4 | 0000000000000000 |
| CCP2CON1L | 974 | 0-00000000000000 | CCP3STATH | 9A6 | ----------00000 | CCP4RBL | 9D8 | 0000000000000000 |
| CCP2CON1H | 976 | 00--000000000000 | CCP3TMRL | 9A8 | 0000000000000000 | CCP4BUFL | 9DC | 0000000000000000 |
| CCP2CON2L | 978 | 00-0----00000000 | CCP3TMRH | 9AA | 0000000000000000 | CCP4BUFH | 9DE | 0000000000000000 |
| CCP2CON2H | 97A | 0------100-00000 | CCP3PRL | 9AC | 1111111111111111 | | | |
| CCP2CON3H | 97E | 0000------0-00-- | CCP3PRH | 9AE | 1111111111111111 | | | |

**Legend:** x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

**TABLE 4-10: SLAVE SFR BLOCK A00h**

| Register | Address | All Resets | Register | Address | All Resets | Register | Address | All Resets |
|---|---|---|---|---|---|---|---|---|
| **DMA** | | | DMACH0 | AC4 | ---0-00000000000 | DMACH1 | ACE | ---0-00000000000 |
| DMACON | ABC | 0-0----------0 | DMAINT0 | AC6 | 0000000000000--0 | DMAINT1 | AD0 | 0000000000000--0 |
| DMABUF | ABE | 0000000000000000 | DMASRC0 | AC8 | 0000000000000000 | DMASRC1 | AD2 | 0000000000000000 |
| DMAL | AC0 | 0001000000000000 | DMADST0 | ACA | 0000000000000000 | DMADST1 | AD4 | 0000000000000000 |
| DMAH | AC2 | 0001000000000000 | DMACNT0 | ACC | 0000000000000001 | DMACNT1 | AD6 | 0000000000000001 |

**Legend:** x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

#### 4.2.4.2 Extended X Data Space

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible, regardless of the contents of the Data Space Read Page register. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space in combination with DSRPAG = 0x00. Consequently, DSRPAG is initialized to 0x001 at Reset.

| | |
|---|---|
| **Note 1:** | DSRPAG should not be used to access Page 0. An EDS access with DSRPAG set to 0x000 will generate an address error trap. |
| **2:** | Clearing the DSRPAG in software has no effect. |

The remaining PSV pages are only accessible using the DSRPAG register in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

#### 4.2.4.3 Software Stack

The W15 register serves as a dedicated Software Stack Pointer (SSP), and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the Stack Pointer (for example, creating stack frames).

| | |
|---|---|
| **Note:** | To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware. |

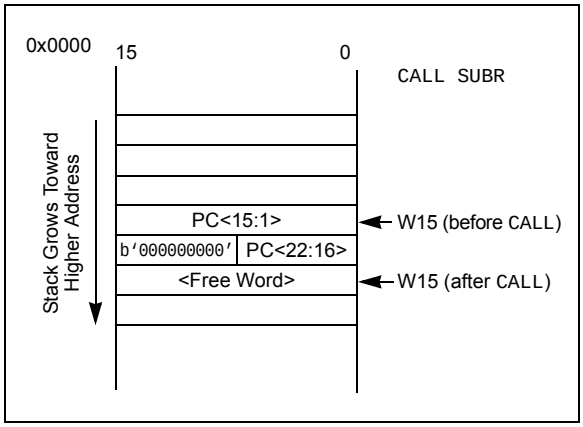
W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33CH128MP508S1 devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-8 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-8. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

| | |
|---|---|
| **Note 1:** | To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to W14 when used as a Stack Frame Pointer (SFA = 1). |
| **2:** | As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment |

**FIGURE 4-8: CALL STACK FRAME**



#### 4.6.5.5 Virtual Connections

The dsPIC33CH128MP508S1 family devices support six virtual S1RPn pins (S1RP170-S1RP175), which are identical in functionality to all other S1RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to S1RP170 and the PWM control input can be configured for S1RP170 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

#### 4.6.5.6 Slave PPS Inputs to Master Core PPS

The dsPIC33CH128MP508S1 Slave core subsystem PPS has connections to the Master core subsystem virtual PPS (S1RPV5-S1RPV0) output blocks. These inputs are mapped as S1RP175, S1RP174, S1RP173, S1RP172, S1RP171 and S1RP170.

The S1RPn inputs, S1RP1-S1RP13, are connected to internal signals from both the Master and Slave core subsystems. Additionally, the Master core virtual PPS output blocks (RPV5-RPV0) are connected to the Slave core PPS circuitry.

There are virtual pins in PPS to share between Master and Slave:

- RP181 is for Master input (RPV5)
- RP180 is for Master input (RPV4)
- RP179 is for Master input (RPV3)
- RP178 is for Master input (RPV2)
- RP177 is for Master input (RPV1)
- RP176 is for Master input (RPV0)
- S1RP175 is for Slave input (S1RPV5)
- S1RP174 is for Slave input (S1RPV4)
- S1RP173 is for Slave input (S1RPV3)
- S1RP172 is for Slave input (S1RPV2)
- S1RP171 is for Slave input (S1RPV1)
- S1RP170 is for Slave input (S1RPV0)

The idea of the S1RPVn (Remappable Pin Virtual) is to interconnect between Master and Slave without an I/O pin. For example, the Master UART receiver can be connected to the Slave UART transmit using S1RPVn and data communication can happen from Slave to Master without using any physical pin.

## 6.4 Master Special Function Registers

These Special Function Registers provide run-time control and status of the Master core's oscillator system.

### 6.4.1 MASTER OSCILLATOR CONTROL REGISTERS

**REGISTER 6-1: OSCCON: OSCILLATOR CONTROL REGISTER (MASTER)(1)**

| U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
|---|---|---|---|---|---|---|---|
| — | COSC2 | COSC1 | COSC0 | — | NOSC2(2) | NOSC1(2) | NOSC0(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CLKLOCK | — | LOCK | — | CF(3) | — | — | OSWEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
- 111 = Fast RC Oscillator (FRC) with Divide-by-n (FRCDIVN)
- 110 = Backup FRC (BFRC)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved – default to FRC
- 011 = Primary Oscillator (XT, HS, EC) with PLL (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
- 111 = Fast RC Oscillator (FRC) with Divide-by-n (FRCDIVN)
- 110 = Backup FRC (BFRC)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved – default to FRC
- 011 = Primary Oscillator (XT, HS, EC) with PLL (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **Unimplemented:** Read as '0'

**Note 1:** Writes to this register require an unlock sequence.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

**REGISTER 7-3: PMD2: MASTER PERIPHERAL MODULE DISABLE 2 CONTROL REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CCP8MD | CCP7MD | CCP6MD | CCP5MD | CCP4MD | CCP3MD | CCP2MD | CCP1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CCP8MD:** SCCP8 Module Disable bit
1 = SCCP8 module is disabled
0 = SCCP8 module is enabled

bit 6 **CCP7MD:** SCCP7 Module Disable bit
1 = SCCP7 module is disabled
0 = SCCP7 module is enabled

bit 5 **CCP6MD:** SCCP6 Module Disable bit
1 = SCCP6 module is disabled
0 = SCCP6 module is enabled

bit 4 **CCP5MD:** SCCP5 Module Disable bit
1 = SCCP5 module is disabled
0 = SCCP5 module is enabled

bit 3 **CCP4MD:** SCCP4 Module Disable bit
1 = SCCP4 module is disabled
0 = SCCP4 module is enabled

bit 2 **CCP3MD:** SCCP3 Module Disable bit
1 = SCCP3 module is disabled
0 = SCCP3 module is enabled

bit 1 **CCP2MD:** SCCP2 Module Disable bit
1 = SCCP2 module is disabled
0 = SCCP2 module is enabled

bit 0 **CCP1MD:** SCCP1 Module Disable bit
1 = SCCP1 module is disabled
0 = SCCP1 module is enabled

**REGISTER 10-3: CCPxCON2L: CCPx CONTROL 2 LOW REGISTERS**

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PWMRSEN | ASDGM | — | SSDG | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
- 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
- 0 = ASEVT bit must be cleared in software to resume PWM activity on output pins

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
- 1 = Waits until the next Time Base Reset or rollover for shutdown to occur
- 0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
- 1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
- 0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
- 1 = ASDGx Source n is enabled (see Table 10-8 and Table 10-9 for auto-shutdown/gating sources)
- 0 = ASDGx Source n is disabled

## 16.4 SENT Control/Status Registers

**REGISTER 16-1: SENTxCON1: SENTx CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SNTEN | — | SNTSIDL | — | RCVEN | TXM(1) | TXPOL(1) | CRCEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PPP | SPCEN(2) | — | PS | — | NIBCNT2 | NIBCNT1 | NIBCNT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **SNTEN:** SENTx Enable bit
1 = SENTx is enabled
0 = SENTx is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SNTSIDL:** SENTx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **RCVEN:** SENTx Receive Enable bit
1 = SENTx operates as a receiver
0 = SENTx operates as a transmitter (sensor)

bit 10 **TXM:** SENTx Transmit Mode bit(1)
1 = SENTx transmits data frame only when triggered using the SYNCTXEN status bit
0 = SENTx transmits data frames continuously while SNTEN = 1

bit 9 **TXPOL:** SENTx Transmit Polarity bit(1)
1 = SENTx data output pin is low in the Idle state
0 = SENTx data output pin is high in the Idle state

bit 8 **CRCEN:** CRC Enable bit
Module in Receive Mode (RCVEN = 1):
1 = SENTx performs CRC verification on received data using the preferred J2716 method
0 = SENTx does not perform CRC verification on received data
Module in Transmit Mode (RCVEN = 1):
1 = SENTx automatically calculates CRC using the preferred J2716 method
0 = SENTx does not calculate CRC

bit 7 **PPP:** Pause Pulse Present bit
1 = SENTx is configured to transmit/receive SENT messages with pause pulse
0 = SENTx is configured to transmit/receive SENT messages without pause pulse

bit 6 **SPCEN:** Short PWM Code Enable bit(2)
1 = SPC control from external source is enabled
0 = SPC control from external source is disabled

bit 5 **Unimplemented:** Read as '0'

**Note 1:** This bit has no function in Receive mode (RCVEN = 1).
**2:** This bit has no function in Transmit mode (RCVEN = 0).

## 19.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note 1:** This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729) in the *"dsPIC33/PIC24 Family Reference Manual",* which is available from the Microchip web site (www.microchip.com).

**2:** The CRC module is available only on the Master.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

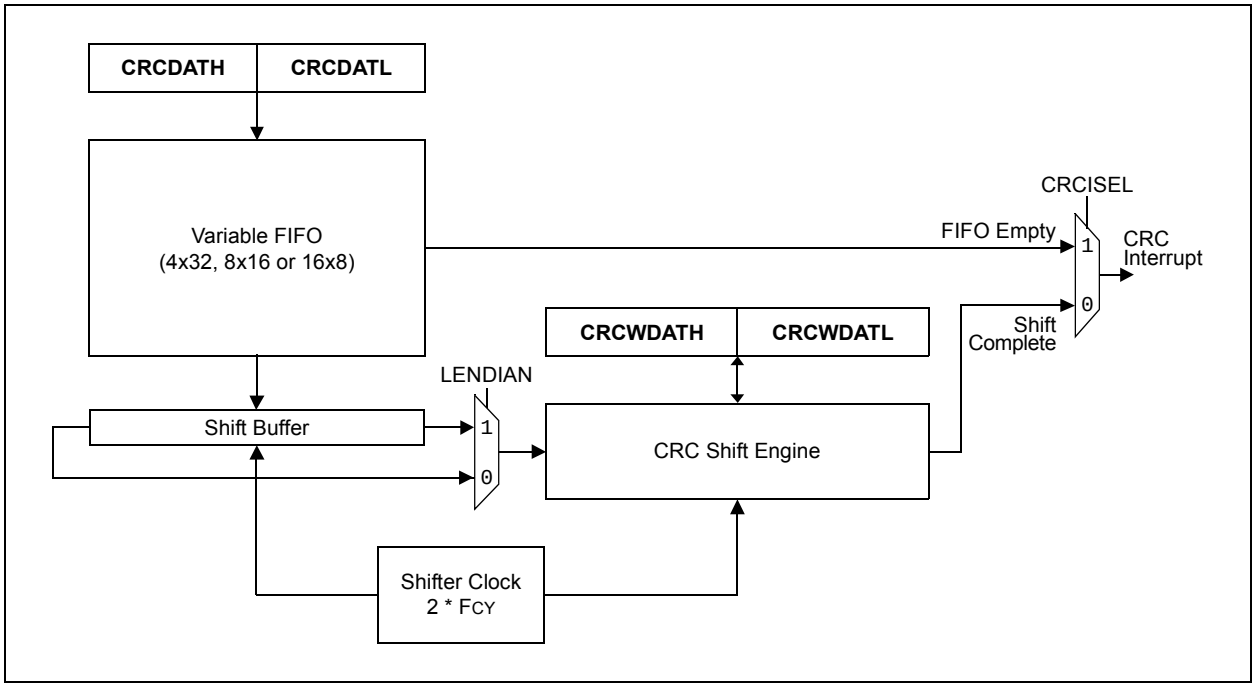
- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

A simple version of the CRC shift engine is displayed in Figure 19-1. Table 19-1 displays a simplified block diagram of the CRC generator.

**TABLE 19-1: CRC MODULE OVERVIEW**

| | Number of CRC Modules | Identical (Modules) |
|---|---|---|
| Master Core | 1 | Yes |
| Slave Core | None | NA |

**FIGURE 19-1: CRC MODULE BLOCK DIAGRAM**



**REGISTER 21-4: FOSCSEL CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/PO-1 | U-1 | U-1 | U-1 | U-1 | R/PO-1 | R/PO-1 | R/PO-1 |
|---|---|---|---|---|---|---|---|
| IESO | — | — | — | — | FNOSC2 | FNOSC1 | FNOSC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6-3 **Unimplemented:** Read as ‘1’

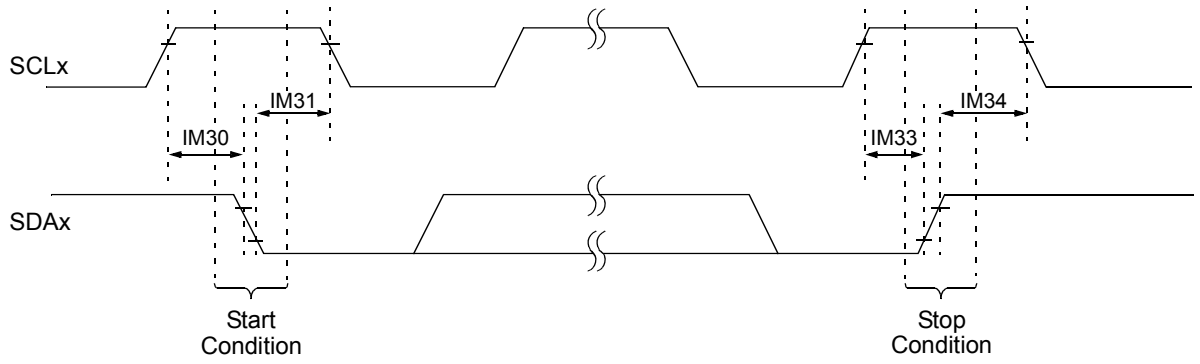
bit 2-0 **FNOSC<2:0>:** Initial Oscillator Source Selection bits
111 = Internal Fast RC (FRC) Oscillator with Postscaler
110 = Backup Fast RC (BFRC)
101 = LPRC Oscillator
100 = Reserved
011 = Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)
010 = Primary (XT, HS, EC) Oscillator
001 = Internal Fast RC Oscillator with PLL (FRCPLL)
000 = Fast RC (FRC) Oscillator

**TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(1) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 40 | DIV2.U | DIV2.U | Wm,Wn | Unsigned 16/16-bit Integer Divide (W1:W0 preserved) | 1 | 6 | N,Z,C,OV |
| | | DIV2.UD | Wm,Wn | Unsigned 32/16-bit Integer Divide (W1:W0 preserved) | 1 | 6 | N,Z,C,OV |
| 41 | DO | DO | #lit15,Expr | Do Code to PC + Expr, lit15 + 1 Times | 2 | 2 | None |
| | | DO | Wn,Expr | Do code to PC + Expr, (Wn) + 1 Times | 2 | 2 | None |
| 42 | ED | ED | Wm*Wm,Acc,Wx,Wy,Wxd | Euclidean Distance (no accumulate) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 43 | EDAC | EDAC | Wm*Wm,Acc,Wx,Wy,Wxd | Euclidean Distance | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 44 | EXCH | EXCH | Wns,Wnd | Swap Wns with Wnd | 1 | 1 | None |
| 46 | FBCL | FBCL | Ws,Wnd | Find Bit Change from Left (MSb) Side | 1 | 1 | C |
| 47 | FF1L | FF1L | Ws,Wnd | Find First One from Left (MSb) Side | 1 | 1 | C |
| 48 | FF1R | FF1R | Ws,Wnd | Find First One from Right (LSb) Side | 1 | 1 | C |
| 49 | FLIM | FLIM | Wb, Ws | Force Data (Upper and Lower) Range Limit without Limit Excess Result | 1 | 1 | N,Z,OV |
| | | FLIM.V | Wb, Ws, Wd | Force Data (Upper and Lower) Range Limit with Limit Excess Result | 1 | 1 | N,Z,OV |
| 50 | GOTO | GOTO | Expr | Go to Address | 2 | 4/2(2) | None |
| | | GOTO | Wn | Go to Indirect | 1 | 4/2(2) | None |
| | | GOTO.L | Wn | Go to Indirect (long address) | 1 | 4/2(2) | None |
| 51 | INC | INC | f | f = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC | f,WREG | WREG = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC | Ws,Wd | Wd = Ws + 1 | 1 | 1 | C,DC,N,OV,Z |
| 52 | INC2 | INC2 | f | f = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 | f,WREG | WREG = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 | Ws,Wd | Wd = Ws + 2 | 1 | 1 | C,DC,N,OV,Z |
| 53 | IOR | IOR | f | f = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR | f,WREG | WREG = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR | #lit10,Wn | Wd = lit10 .IOR. Wd | 1 | 1 | N,Z |
| | | IOR | Wb,Ws,Wd | Wd = Wb .IOR. Ws | 1 | 1 | N,Z |
| | | IOR | Wb,#lit5,Wd | Wd = Wb .IOR. lit5 | 1 | 1 | N,Z |
| 54 | LAC | LAC | Wso,#Slit4,Acc | Load Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | LAC.D | Wso, #Slit4, Acc | Load Accumulator Double | 1 | 2 | OA,SA,OB,SB |
| 55 | LDSLV | LDSLV | Wso,Wdo,lit2 | Move a Single Instruction Word from Master to Slave PRAM | 1 | 1 | None |
| 56 | LNK | LNK | #lit14 | Link Frame Pointer | 1 | 1 | SFA |
| 57 | LSR | LSR | f | f = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR | f,WREG | WREG = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR | Ws,Wd | Wd = Logical Right Shift Ws | 1 | 1 | C,N,OV,Z |
| | | LSR | Wb,Wns,Wnd | Wnd = Logical Right Shift Wb by Wns | 1 | 1 | N,Z |
| | | LSR | Wb,#lit5,Wnd | Wnd = Logical Right Shift Wb by lit5 | 1 | 1 | N,Z |
| 58 | MAC | MAC | Wm*Wn,Acc,Wx,Wxd,Wy,Wyd, AWB | Multiply and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MAC | Wm*Wm,Acc,Wx,Wxd,Wy,Wyd | Square and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 59 | MAX | MAX | Acc | Force Data Maximum Range Limit | 1 | 1 | N,OV,Z |
| | | MAX.V | Acc, Wnd | Force Data Maximum Range Limit with Result | 1 | 1 | N,OV,Z |

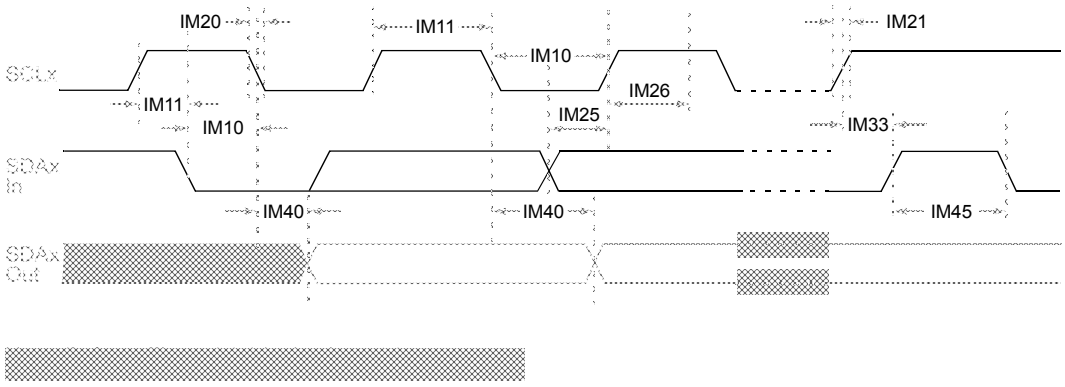
**Note 1:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
**2:** Cycle times for Slave core are different for Master core, as shown in 2.
**3:** For dsPIC33CH128MP508 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times

**FIGURE 24-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**



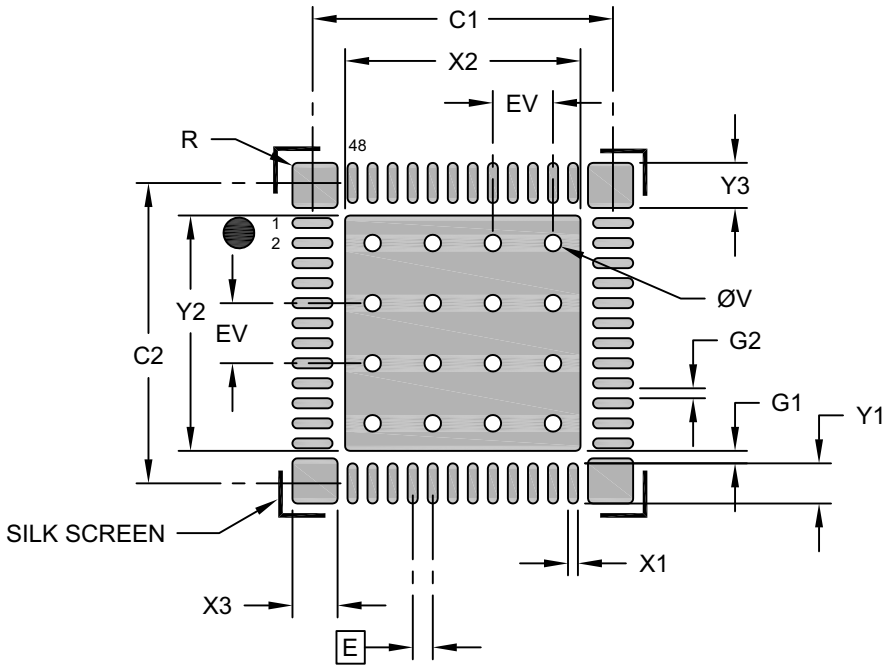

**Note:** Refer to Figure 24-1 for load conditions.

**FIGURE 24-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**



### 48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Center Pad Width | X2 | | | 4.70 |
| Center Pad Length | Y2 | | | 4.70 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X48) | X1 | | | 0.20 |
| Contact Pad Length (X48) | Y1 | | | 0.80 |
| Corner Anchor Pad Width (X4) | X3 | | | 0.90 |
| Corner Anchor Pad Length (X4) | Y3 | | | 0.90 |
| Pad Corner Radius (X 20) | R | | | 0.10 |
| Contact Pad to Center Pad (X48) | G1 | 0.25 | | |
| Contact Pad to Contact Pad | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

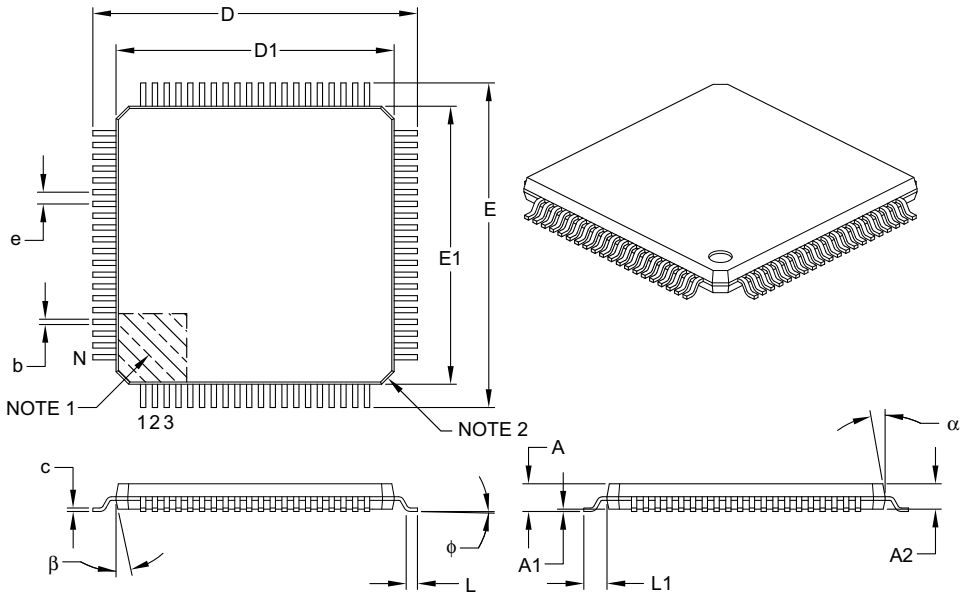
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2442A-M4

### 80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 80 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 14.00 BSC | |
| Overall Length | D | | 14.00 BSC | |
| Molded Package Width | E1 | | 12.00 BSC | |
| Molded Package Length | D1 | | 12.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B