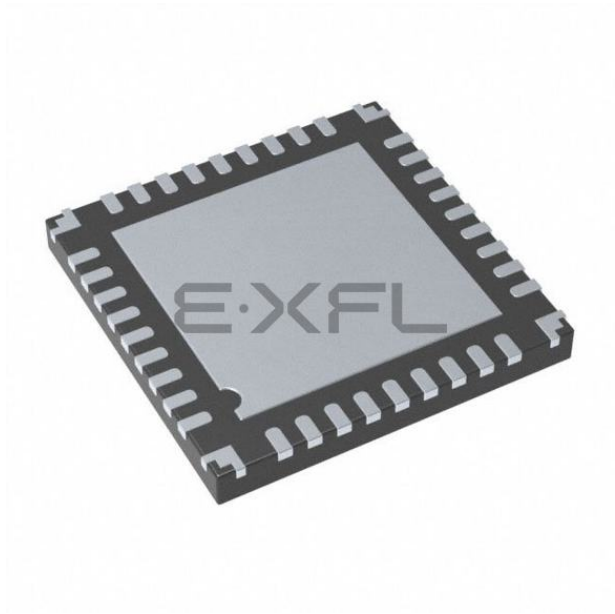

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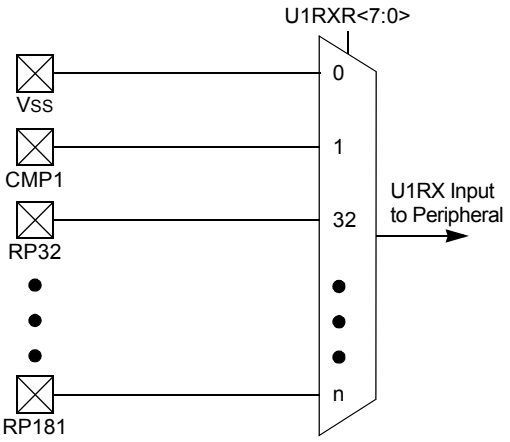
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	27
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp203t-i-m5

FIGURE 3-20: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1'). Physical connection to a pin can be made through RP32 through RP71. There are internal signals and virtual pins that can be connected to an input. Table 3-30 shows the details of the input assignment.

Example 3-2 provides a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

EXAMPLE 3-2: CONFIGURING UART1 INPUT AND OUTPUT FUNCTIONS

```
//
*****************************************
// Unlock Registers
//*****************************************
__builtin_write_RPCON(0x0000);
//*****************************************
// Configure Input Functions (See Table 3-31)
// Assign U1Rx To Pin RP35
//***************************
_U1RXR = 35;
// Assign U1CTS To Pin RP36
//***************************
_U1CTSR = 36;
//*****************************************
// Configure Output Functions (See Table 3-33)
//*****************************************
// Assign U1Tx To Pin RP37
//***************************
_RP37 = 1;
//***************************
// Assign U1RTS To Pin RP38
//***************************
_RP38 = 2;
//*****************************************
// Lock Registers
//*****************************************
__builtin_write_RPCON(0x0800);
```

TABLE 3-30: MASTER REMAPPABLE PIN INPUTS (CONTINUED)

RPINRx<15:8> or RPINRx<7:0 >	Function	Available on Ports
60	RP60	Port Pin RC12
61	RP61	Port Pin RC13
62	RP62	Port Pin RC14
63	RP63	Port Pin RC15
64	RP64	Port Pin RD0
65	RP65	Port Pin RD1
66	RP66	Port Pin RD2
67	RP67	Port Pin RD3
68	RP68	Port Pin RD4
69	RP69	Port Pin RD5
70	RP70	Port Pin RD6
71	RP71	Port Pin RD7
72-169	RP72-RP169	Reserved
170	RP170	Slave Virtual S1RPV0
171	RP171	Slave Virtual S1RPV1
172	RP172	Slave Virtual S1RPV2
173	RP173	Slave Virtual S1RPV3
174	RP174	Slave Virtual S1RPV4
175	RP175	Slave Virtual S1RPV5
176	RP176	Master Virtual RPV0
177	RP177	Master Virtual RPV1
178	RP178	Master Virtual RPV2
179	RP179	Master Virtual RPV3
180	RP180	Master Virtual RPV4
181	RP181	Master Virtual RPV5

REGISTER 3-183: PTGCST: PTG CONTROL/STATUS LOW REGISTER (CONTINUED)

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Operation Selection bit(1)

11 = Single-level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 3)

10 = Single-level detect with Step delay executed on exit of command (Mode 2)

01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 1)

00 = Continuous edge detect with Step delay executed on exit of command (Mode 0)

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL Step command software trigger option.

3: The PTGSSEN bit may only be written when in Debug mode.

TABLE 3-45: PTG COMMAND OPTIONS

bit 3-0	Step Command	OPTION<3:0>	Command Description
	PTGWHI(1) or PTGWLO(1)	0000	PTGI0 (see Table 3-46 for input assignments).
		• • •	• • •
		1111	PTGI15 (see Table 3-46 for input assignments).
	PTGIRQ(1)	0000	Generate PTG Interrupt 0.
		• • •	• • •
		0111	Generate PTG Interrupt 7.
		1000	Reserved; do not use.
		• • •	• • •
		1111	Reserved; do not use.
	PTGTRIG	0000	PTGO0 (see Table 3-47 for output assignments).
		0001	PTGO1 (see Table 3-47 for output assignments).
		• • •	• • •
		1110	PTGO30 (see Table 3-47 for output assignments).
		1111	PTGO31 (see Table 3-47 for output assignments).

Note 1: All reserved commands or options will execute, but they do not have any affect (i.e., execute as a NOP instruction).

4.1.5 PROGRAMMER'S MODEL

The programmer's model for the dsPIC33CH128MP508S1 family is shown in Figure 4-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 4-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33CH128MP508S1 devices contain control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Figure 4-3.

TABLE 4-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate 1 Working Register Array
W0 through W14(1)	Alternate 2 Working Register Array
W0 through W14(1)	Alternate 3 Working Register Array
W0 through W14(1)	Alternate 4 Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators (Additional 4 Alternate Accumulators)
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Counter Register
DOSTARTH(2), DOSTARTL(2)	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-8: SLAVE SFR BLOCK 800h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Interrupts			IPC2	844	-100-100-100-100	IPC34	884	-100-100-100-100
IFS0	800	0000000000-00000	IPC3	846	-100-100-100-100	IPC35	886	---------100-100
IFS1	802	0000000000000000	IPC4	848	-100-100-100-100	IPC35	886	---------100-100
IFS2	804	00000-00-00000--	IPC5	84A	-100-100-100-100	IPC36	888	-----100--------
IFS3	806	000--------00000	IPC6	84C	-100-100-100-100	IPC42	894	-100-100-100-100
IFS4	808	--000----0000-00	IPC8	850	-100-100--------	IPC43	896	-100-100-100-100
IFS5	80A	000000000000000-	IPC9	852	-----100-100-100	IPC44	898	-100-100-100-100
IFS6	80C	0000000000000000	IPC10	854	-100-----100-100	IPC45	89A	------------100
IFS7	80E	0000000000000---	IPC12	858	-100-100-100-100	IPC47	89E	-----100-100----
IFS8	810	--0000000000000-	IPC15	85E	-100-100-100----	INTCON1	8C0	000000000000000-
IFS9	812	--0---00-00--0--	IPC16	860	-100-----100-100	INTCON2	8C2	000----0----0000
IFS10	814	00000000--------	IPC17	862	-----100-100-100	INTCON3	8C4	-------0---0---0
IFS11	816	-00--------00000	IPC18	864	-100------------	INTCON4	8C6	--------------00
IEC0	820	0000000000-00000	IPC19	866	---------100-100	INTTREG	8C8	000-000000000000
IEC1	822	0000000000000000	IPC20	868	-100-100-100----	**Flash**		
IEC2	824	00000-00-00000--	IPC21	86A	-100-100-100-100	NVMCON	8D0	0000--00----0000
IEC3	826	000--------00000	IPC22	86C	-100-100-100-100	NVMADR	8D2	0000000000000000
IEC4	828	--000----0000-00	IPC23	86E	-100-100-100-100	NVMADRU	8D4	--------00000000
IEC5	82A	000000000000000-	IPC24	870	-100-100-100-100	NVMKEY	8D6	--------00000000
IEC6	82C	0000000000000000	IPC25	872	-100-100-100-100	NVMSRCADRL	8D8	0000000000000000
IEC7	82E	0000000000000---	IPC26	874	-100-100-100-100	NVMSRCADRH	8DA	--------00000000
IEC8	830	--0000000000000-	IPC27	876	-100-100-100-100	PGA1CON	8E0	00000000---0-010
IEC8	830	--0000000000000-	IPC28	878	-100------------	PGA1CAL	8E2	--------00000000
IEC9	832	--0---00-00--0--	IPC29	87A	-100-100-100-100	PGA2CON	8E4	00000000---0-010
IEC10	834	00000000------00	IPC30	87C	-100-100-100-100	PGA2CAL	8E6	--------00000000
IEC11	836	-00--------00000	IPC31	87E	-100-100-100-100	PGA3CON	8E8	00000000---0-010
IPC0	840	-100-100-100-100	IPC32	880	-100-100-100----	PGA3CAL	8EA	--------00000000
IPC1	842	-100-100-----100	IPC33	882	-100-100-100-100			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

EXAMPLE 4-2: SLAVE PRAM LOAD AND VERIFY ROUTINE

```
#include <libpic30.h>
//__program_slave(core#, verify, &slave_image)
if (__program_slave(1, 0, &slave) == 0)
{
   /* now verify */
   if (__program_slave(1, 1, &slave) ==
   ESLV_VERIFY_FAIL)
   {
        asm("reset");   // try again
   }
}
```

The `__program_slave(core#, verify, &slave_image)` routine only supports Slave images created with a compatible Microchip language tools format. Slave PRAM images not following this format will require a custom routine that follows all requirements for the PRAM Master to Slave image loading process described in this chapter.

4.3.4 PRAM DUAL PARTITION CONSIDERATIONS

For dsPIC33CH128MP508S1 family devices operating in Dual Partition PRAM Program Memory modes, both partitions would be loaded using the Master to Slave image loading process. The Master can load the active partition of the PRAM only when SLVEN = 0 (Slave is not running). The Master can load the PRAM Inactive Partition any time. To support LiveUpdate, the Master would load the PRAM Inactive Partition while the Slave is running and then the Slave would execute the BOOTSWP instruction to swap partitions.

4.3.4.1 PRAM Partition Swapping

At device Reset, the default PRAM partition is Partition 1. The BOOTSWP instruction provides the means of swapping the Active and Inactive Partitions (soft swap) without the need for a device Reset. The BOOTSWP must always be followed by a GOTO instruction. The BOOTSWP instruction swaps the Active and Inactive Partitions, and the PC vectors to the location specified by the GOTO instruction in the newly Active Partition.

It is important to note that interrupts should temporarily be disabled while performing the soft swap sequence, and that after the partition swap, all peripherals and interrupts which were enabled remain enabled. Additionally, the RAM and stack will maintain their state after the switch. As a result, it is recommended that applications using soft swaps jump to a routine that will reinitialize the device in order to ensure the firmware runs as expected. The Configuration registers will have no effect during a soft swap.

For robustness of operation, in order to execute the BOOTSWP instruction, it is necessary to execute the NVM unlocking sequence as follows:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Execute the BOOTSWP instruction.

If the unlocking sequence is not performed, the BOOTSWP instruction will be executed as a forced NOP and a GOTO instruction, following the BOOTSWP instruction, will be executed, causing the PC to jump to that location in the current operating partition.

The SFTSWP and P2ACTIV bits in the NVMCON register are used to determine a successful swap of the Active and Inactive Partitions, as well as which partition is active. After the BOOTSWP and GOTO instructions, the SFTSWP bit should be polled to verify the partition swap has occurred and then cleared for the next panel swap event.

4.3.4.2 Dual Partition Modes

While operating in Dual Partition mode, the dsPIC33CH128MP508S1 family devices have the option for both partitions to have their own defined security segments, as shown in Figure .

Alternatively, the device can operate in Protected Dual Partition mode, where Partition 1 becomes permanently write-protected. Protected Dual Partition mode allows for a “Factory Default” mode, which provides a fail-safe backup image to be stored in Partition 1.

TABLE 4-29: SLAVE PPS INPUT CONTROL REGISTERS

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPCONL	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—
RPINR0	INT1R7	INT1R6	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	—	—	—	—	—	—	—	—
RPINR1	INT3R7	INT3R6	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0	INT2R7	INT2R6	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
RPINR2	T1CKR7	T1CKR6	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0	—	—	—	—	—	—	—	—
RPINR3	ICM1R7	ICM1R6	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0	TCKI1R7	TCKI1R6	TCKI1R5	TCKI1R4	TCKI1R3	TCKI1R2	TCKI1R1	TCKI1R0
RPINR4	ICM2R7	ICM2R6	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0	TCKI2R7	TCKI2R6	TCKI2R5	TCKI2R4	TCKI2R3	TCKI2R2	TCKI2R1	TCKI2R0
RPINR5	ICM3R7	ICM3R6	ICM3R5	ICM3R4	ICM3R3	ICM3R2	ICM3R1	ICM3R0	TCKI3R7	TCKI3R6	TCKI3R5	TCKI3R4	TCKI3R3	TCKI3R2	TCKI3R1	TCKI3R0
RPINR6	ICM4R7	ICM4R6	ICM4R5	ICM4R4	ICM4R3	ICM4R2	ICM4R1	ICM4R0	TCKI4R7	TCKI4R6	TCKI4R5	TCKI4R4	TCKI4R3	TCKI4R2	TCKI4R1	TCKI4R0
RPINR11	OCFBR7	OCFBR6	OCFBR5	OCFBR4	OCFBR3	OCFBR2	OCFBR1	OCFBR0	OCFAR7	OCFAR6	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0
RPINR12	PCI9R7	PCI9R6	PCI9R5	PCI9R4	PCI9R3	PCI9R2	PCI9R1	PCI9R0	PCI8R7	PCI8R6	PCI8R5	PCI8R4	PCI8R3	PCI8R2	PCI8R1	PCI8R0
RPINR13	PCI11R7	PCI11R6	PCI11R5	PCI11R4	PCI11R3	PCI11R2	PCI11R1	PCI11R0	PCI10R7	PCI10R6	PCI10R5	PCI10R4	PCI10R3	PCI10R2	PCI10R1	PCI10R0
RPINR14	QEIB1R7	QEIB1R6	QEIB1R5	QEIB1R4	QEIB1R3	QEIB1R2	QEIB1R1	QEIB1R0	QEIA1R7	QEIA1R6	QEIA1R5	QEIA1R4	QEIA1R3	QEIA1R2	QEIA1R1	QEIA1R0
RPINR15	QEIHOM1R7	QEIHOM1R6	QEIHOM1R5	QEIHOM1R4	QEIHOM1R3	QEIHOM1R2	QEIHOM1R1	QEIHOM1R0	QEINDX1R7	QEINDX1R6	QEINDX1R5	QEINDX1R4	QEINDX1R3	QEINDX1R2	QEINDX1R1	QEINDX1R0
RPINR18	U1DSRR7	U1DSRR6	U1DSRR5	U1DSRR4	U1DSRR3	U1DSRR2	U1DSRR1	U1DSRR0	U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
RPINR20	SCK1R7	SCK1R6	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0	SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
RPINR21	REFOIR7	REFOIR6	REFOIR5	REFOIR4	REFOIR3	REFOIR2	REFOIR1	REFOIR0	SS1R7	SS1R6	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
RPINR23	U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0	—	—	—	—	—	—	—	—
RPINR37	PCI17R7	PCI17R6	PCI17R5	PCI17R4	PCI17R3	PCI17R2	PCI17R1	PCI17R0	—	—	—	—	—	—	—	—
RPINR38	—	—	—	—	—	—	—	—	PCI18R7	PCI18R6	PCI18R5	PCI18R4	PCI18R3	PCI18R2	PCI18R1	PCI18R0
RPINR42	PCI13R7	PCI13R6	PCI13R5	PCI13R4	PCI13R3	PCI13R2	PCI13R1	PCI13R0	PCI12R7	PCI12R6	PWM12R5	PWM12R4	PWM12R3	PWM12R2	PWM12R1	PWM12R0
RPINR43	PCI15R7	PCI15R6	PCI15R5	PCI15R4	PCI15R3	PCI15R2	PCI15R1	PCI15R0	PCI14R7	PCI14R6	PCI14R5	PCI14R4	PCI14R3	PCI14R2	PCI14R1	PCI14R0
RPINR44	—	—	—	—	—	—	—	—	PCI16R7	PCI16R6	PCI16R5	PCI16R4	PCI16R3	PCI16R2	PCI16R1	PCI16R0
RPINR45	CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0	—	—	—	—	—	—	—	—
RPINR46	CLCINCR7	CLCINCR6	CLCINCR5	CLCINCR4	CLCINCR3	CLCINCR2	CLCINCR1	CLCINCR0	CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
RPINR47	ADCTRGR7	ADCTRGR6	ADCTRGR5	ADCTRGR4	ADCTRGR3	ADCTRGR2	ADCTRGR1	ADCTRGR0	CLCINDR7	CLCINDR6	CLCINDR5	CLCINDR4	CLCINDR3	CLCINDR2	CLCINDR1	CLCINDR0

REGISTER 4-47: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIHOM1R7	QEIHOM1R6	QEIHOM1R5	QEIHOM1R4	QEIHOM1R3	QEIHOM1R2	QEIHOM1R1	QEIHOM1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEINDX1R7	QEINDX1R6	QEINDX1R5	QEINDX1R4	QEINDX1R3	QEINDX1R2	QEINDX1R1	QEINDX1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **QEIHOM1R<7:0>:** Assign QEI Home 1 Input (S1QEIHOM1) to the Corresponding S1RPn Pin bits See Table 4-27.

bit 7-0 **QEINDX1R<7:0>:** Assign QEI Index 1 Input (S1QEINDX1) to the Corresponding S1RPn Pin bits See Table 4-27.

REGISTER 4-48: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1DSRR7	U1DSRR6	U1DSRR5	U1DSRR4	U1DSRR3	U1DSRR2	U1DSRR1	U1DSRR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **U1DSRR<7:0>:** Assign UART1 Data-Set-Ready ($\overline{\text{S1U1DSR}}$) to the Corresponding S1RPn Pin bits See Table 4-27.

bit 7-0 **U1RXR<7:0>:** Assign UART1 Receive (S1U1RX) to the Corresponding S1RPn Pin bits See Table 4-27.

5.2 Slave MSI Control Registers

The following registers are associated with the Slave MSI module and are located in the Slave SFR space.

- Register 5-9: SI1CON
- Register 5-10: SI1STAT
- Register 5-11: SI1MBX
- Register 5-12: SI1MBXnD
- Register 5-13: SI1FIFOCS
- Register 5-14: SWMRFDATA
- Register 5-15: SRMWFDATA

REGISTER 5-9: SI1CON: MSI1 SLAVE CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	RFITSEL1	RFITSEL0	STMIRQ	MTSIACK
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
MRSTIE	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-10 **RFITSEL<1:0>:** Read FIFO Interrupt Threshold Select bits
11 = Triggers data valid interrupt when FIFO is full after Slave write
10 = Triggers data valid interrupt when FIFO is 75% full after Slave write
01 = Triggers data valid interrupt when FIFO is 50% full after Slave write
00 = Triggers data valid interrupt when 1st FIFO entry is written by Slave

bit 9 **STMIRQ:** Slave to Master Interrupt Request bit
1 = Interrupts the Master
0 = Does not interrupt the Master

bit 8 **MTSIACK:** Slave to Acknowledge Master Interrupt bit
1 = If MTSIRQ = 1, Slave Acknowledges Master interrupt request, else protocol error
0 = If MTSIRQ = 0, Slave has not yet Acknowledged Master interrupt request, else no Master to Slave interrupt request is pending

bit 7 **MRSTIE:** Master Reset Event Interrupt Enable bit
1 = Slave Master Reset event interrupt occurs when Master enters Reset state
0 = Slave Master Reset event interrupt does not occur when Master enters Reset state

bit 6-0 **Unimplemented:** Read as ‘0’

Equation 6-3 provides the relationship between the APLL Input Frequency (AF_{PLLI}) and the AVCO Output Frequency (AF_{VCO}).

EQUATION 6-3: MASTER/SLAVE CORE AF_{VCO} CALCULATION

$$AF_{VCO} = AF_{PLLI} \times \left(\frac{M}{N1}\right) = AF_{PLLI} \times \left(\frac{APLLFBDIV<7:0>}{APLLPRE<3:0>}\right)$$

Equation 6-4 provides the relationship between the APLL Input Frequency (AF_{PLLI}) and APLL Output Frequency (AF_{PLLO}).

EQUATION 6-4: MASTER/SLAVE CORE AF_{PLLO} CALCULATION

$$AF_{PLLO} = AF_{PLLI} \times \left(\frac{M}{N1 \times N2 \times N3}\right) = AF_{PLLI} \times \left(\frac{APLLFBDIV<7:0>}{APLLPRE<3:0> \times APOST1DIV<2:0> \times APOST2DIV<2:0>}\right)$$

Where:

M = $APLLFBDIV<7:0>$
$N1$ = $APLLPRE<3:0>$
$N2$ = $APOST1DIV<2:0>$
$N3$ = $APOST2DIV<2:0>$

EXAMPLE 6-3: CODE EXAMPLE FOR USING MASTER OR SLAVE AUXILIARY PLL WITH THE INTERNAL FRC OSCILLATOR

```
//code example for AFVCO = 1 GHz and AFPLLO = 500 MHz using 8 MHz internal FRC
// Configure the source clock for the APLL
ACLKCON1bits.FRCSEL = 1;              // Select internal FRC as the clock source
// Configure the APLL prescaler, APLL feedback divider, and both APLL postscalers.
ACLKCON1bits.APLLPRE = 1;             // N1 = 1
APLLFBD1bits.APLLFBDIV = 125;         // M = 125
APLLDIV1bits.APOST1DIV = 2;           // N2 = 2
APLLDIV1bits.APOST2DIV = 1;           // N3 = 1
// Enable APLL
ACLKCON1bits.APLLEN = 1;
```

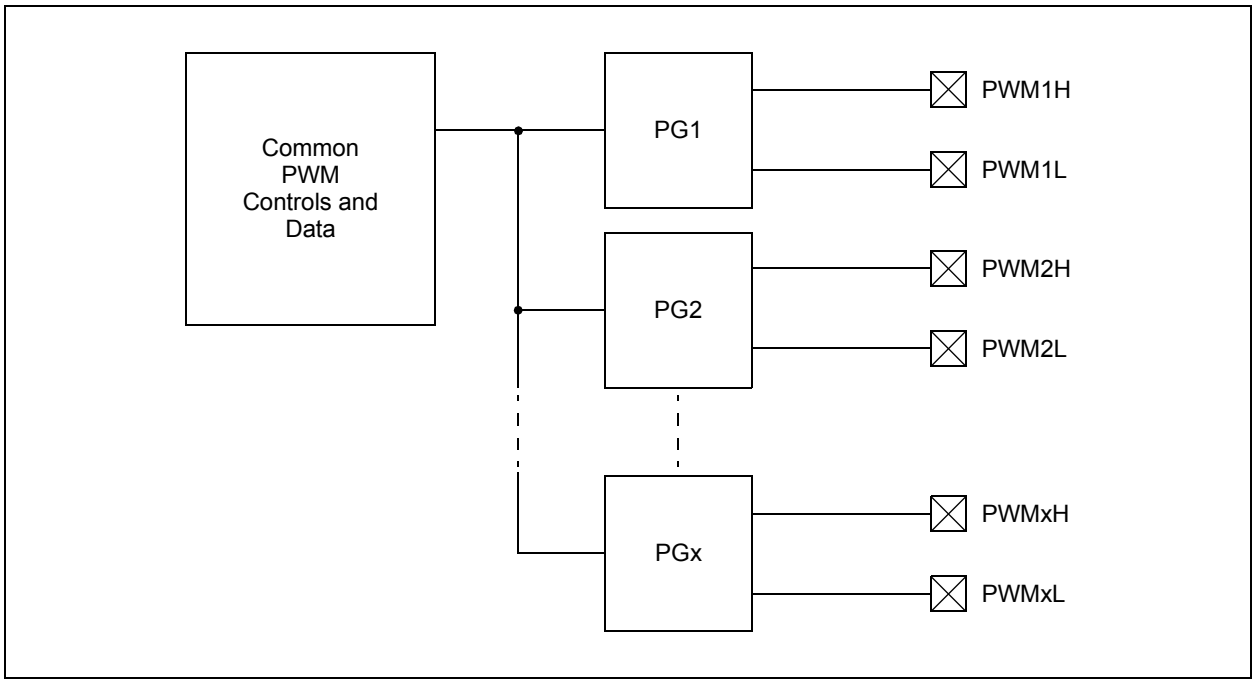
Note: Even with the APLLEN bit set, another peripheral must generate a clock request before the APLL will start.

NOTES:

9.2 Architecture Overview

The PWM module consists of a common set of controls and features, and multiple instantiations of PWM Generators (PGs). Each PWM Generator can be independently configured or multiple PWM Generators can be used to achieve complex multiphase systems. PWM Generators can also be used to implement sophisticated triggering, protection and logic functions. A high-level block diagram is shown in Figure 9-1.

FIGURE 9-1: PWM HIGH-LEVEL BLOCK DIAGRAM



REGISTER 9-7: CMBTRIGL: COMBINATIONAL TRIGGER REGISTER LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTA8EN	CTA7EN	CTA6EN	CTA5EN	CTA4EN	CTA3EN	CTA2EN	CTA1EN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CTA8EN:** Enable Trigger Output from PWM Generator #8 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 6 **CTA7EN:** Enable Trigger Output from PWM Generator #7 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 5 **CTA6EN:** Enable Trigger Output from PWM Generator #6 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 4 **CTA5EN:** Enable Trigger Output from PWM Generator #5 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 3 **CTA4EN:** Enable Trigger Output from PWM Generator #4 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 2 **CTA3EN:** Enable Trigger Output from PWM Generator #3 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 1 **CTA2EN:** Enable Trigger Output from PWM Generator #2 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

bit 0 **CTA1EN:** Enable Trigger Output from PWM Generator #1 as Source for Combinational Trigger A bit
1 = Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal
0 = Disabled

REGISTER 13-4: UxSTAH: UARTx STATUS REGISTER HIGH

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	UTXISEL2	UTXISEL1	UTXISEL0	—	URXISEL2(1)	URXISEL1(1)	URXISEL0(1)
bit 15							bit 8

HS/R/W-0	R/W-0	R/S-1	R-0	R-1	R-1	R/S-1	R-0
TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
bit 7							bit 0

Legend:	HS = Hardware Settable bit	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **UTXISEL<2:0>:** UART Transmit Interrupt Select bits
111 = Sets transmit interrupt when there is one empty slot left in the buffer
...
010 = Sets transmit interrupt when there are six empty slots or more in the buffer
001 = Sets transmit interrupt when there are seven empty slots or more in the buffer
000 = Sets transmit interrupt when there are eight empty slots in the buffer; TX buffer is empty

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **URXISEL<2:0>:** UART Receive Interrupt Select bits(1)
111 = Triggers receive interrupt when there are eight words in the buffer; RX buffer is full
...
001 = Triggers receive interrupt when there are two words or more in the buffer
000 = Triggers receive interrupt when there is one word or more in the buffer

bit 7 **TXWRE:** TX Write Transmit Error Status bit
LIN and Parity Modes:
1 = A new byte was written when the buffer was full or when P2<8:0> = 0 (must be cleared by software)
0 = No error
Address Detect Mode:
1 = A new byte was written when the buffer was full or to P1<8:0> when P1x was full (must be cleared by software)
0 = No error
Other Modes:
1 = A new byte was written when the buffer was full (must be cleared by software)
0 = No error

bit 6 **STPMD:** Stop Bit Detection Mode bit
1 = Triggers RXIF at the end of the last Stop bit
0 = Triggers RXIF in the middle of the first (or second, depending on the STSEL<1:0> setting) Stop bit

bit 5 **UTXBE:** UART TX Buffer Empty Status bit
1 = Transmit buffer is empty; writing '1' when UTXEN = 0 will reset the TX FIFO Pointers and counters
0 = Transmit buffer is not empty

bit 4 **UTXBF:** UART TX Buffer Full Status bit
1 = Transmit buffer is full
0 = Transmit buffer is not full

bit 3 **RIDLE:** Receive Idle bit
1 = UART RX line is in the Idle state
0 = UART RX line is receiving something

Note 1: The receive watermark interrupt is not set if PERIF or FERIF is set and the corresponding IE bit is set.

NOTES:

TABLE 21-2: MASTER CONFIGURATION REGISTERS MAP

Register Name	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSEC	—	AIVTDIS	—	—	—	CSS2	CSS1	CSS0	CWRP	GSS1	GSS0	GWRP	—	BSEN	BSS1	BSS0	BWRP
FBSLIM	—	—	—	—	BSLIM<12:0>												
FSIGN	—	r(2)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
FOSCSEL	—	—	—	—	—	—	—	—	—	IESO	—	—	—	—	FNOSC2	FNOSC1	FNOSC0
FOSC	—	—	—	—	XTBST	XTCFG1	XTCFG0	—	r(1)	FCKSM1	FCKSM0	—	—	—	OSCIOFNC	POSCMD1	POSCMD0
FWDT	—	FWDTEN	SWDTPS4	SWDTPS3	SWDTPS2	SWDTPS1	SWDTPS0	WDTWIN1	WDTWIN0	WINDIS	RCLKSEL1	RCLKSEL0	RWDTPS4	RWDTPS3	RWDTPS2	RWDTPS1	RWDTPS0
FPOR	—	—	—	—	—	—	—	—	—	—	—	r(1)	r(1)	—	—	—	—
FICD	—	—	—	—	—	—	—	—	—	r(1)	—	JTAGEN	—	—	—	ICS1	ICS0
FDMTIVTL	—	DMTIVT<15:0>															
FDMTIVTH	—	DMTIVT<31:16>															
FDMTCNTL	—	DMTCNT<15:0>															
FDMTCNTH	—	DMTCNT<31:16>															
FDMT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMTDIS
FDEVOPT	—	—	—	SPI2PIN	—	—	SMBEN	r(1)	r(1)	r(1)	—	—	ALTI2C2	ALTI2C1	r(1)	—	—
FALTREG	—	—	CTXT4<2:0>			—	CTXT3<2:0>			—	CTXT2<2:0>			—	CTXT1<2:0>		
FMBXM	—	MBXM<15:0>															
FMBXHS1	—	MBXHSD3	MBXHSD2	MBXHSD1	MBXHSD0	MBXHSC3	MBXHSC2	MBXHSC1	MBXHSC0	MBXHSB3	MBXHSB2	MBXHSB1	MBXHSB0	MBXHSA3	MBXHSA2	MBXHSA1	MBXHSA0
FMBXHS2	—	MBXHSH3	MBXHSH2	MBXHSH1	MBXHSH0	MBXHSG3	MBXHSG2	MBXHSG1	MBXHSG0	MBXHSF3	MBXHSF2	MBXHSF1	MBXHSF0	MBXHSE3	MBXHSE2	MBXHSE1	MBXHSE0
FMBXHSEN	—	—	—	—	—	—	—	—	—	HS<H:A>EN							
FCFGPRA0	—	—	—	—	—	—	—	—	—	—	—	—	CPRA<4:0>				
FCFGPRB0	—	CPRB<15:0>															
FCFGPRC0	—	CPRC<15:0>															
FCFGPRD0	—	CPRD<15:0>															
FCFGPRE0	—	CPRE<15:0>															

Legend: — = unimplemented bit, read as '1'; r = reserved bit.

Note 1: Bit is reserved, maintain as '1'.

2: Bit is reserved, maintain as '0'.

23.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

23.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

23.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

23.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

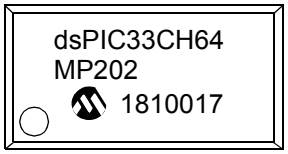
- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

25.0 PACKAGING INFORMATION

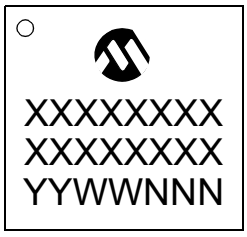
25.1 Package Marking Information

28-Lead SSOP (5.30 mm)

Example

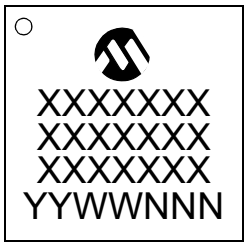


28-Lead UQFN (6x6 mm)



Example

36-Lead UQFN (5x5 mm)



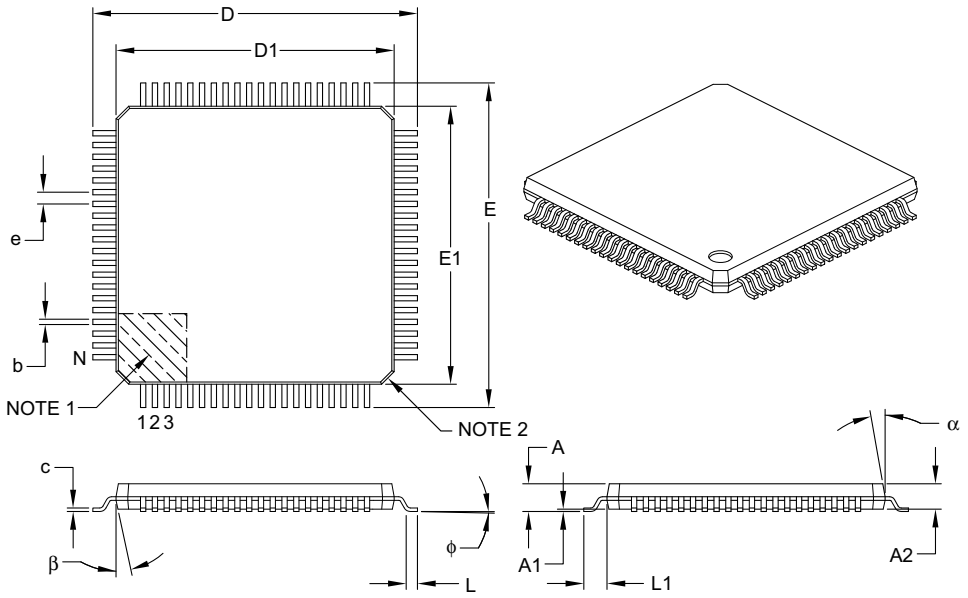
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B