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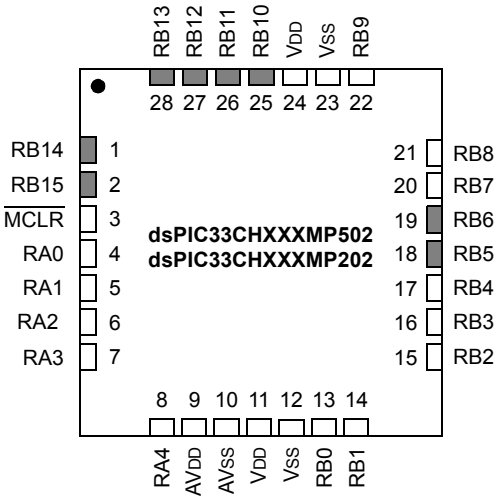
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp205-e-pt

Pin Diagrams (Continued)

28-Pin UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

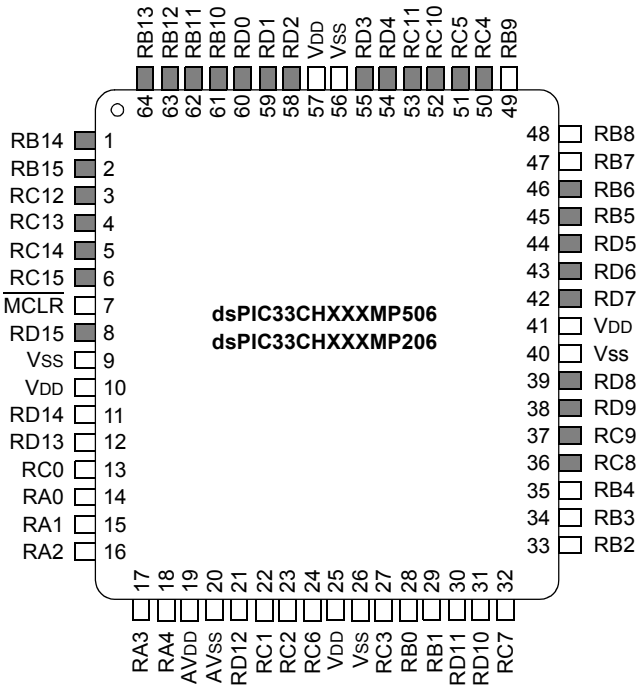
TABLE 5: 28-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	MCLR	—
4	AN0/CMP1A/RA0	S1RA0
5	AN1/RA1	S1AN15/S1RA1
6	AN2/RA2	S1AN16/S1RA2
7	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
8	AN4/IBIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
9	AVDD	AVDD
10	AVSS	AVSS
11	VDD	VDD
12	VSS	VSS
13	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
14	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
15	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
16	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
17	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
18	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
19	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
20	TDO/AN9/**RP39**/RB7	S1MCLR1/S1AN6/**S1RP39**/S1PWM5H/S1RB7
21	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
22	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
23	VSS	VSS
24	VDD	VDD
25	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
26	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
27	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM2H/S1RB12
28	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1PWM2L/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

64-Pin TQFP/QFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

TABLE 3-16: MASTER SFR BLOCK D00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O Ports			RPINR19	D2A	1111111111111111	RPOR4	D88	--000000--000000
RPCON	D00	----0----------	RPINR20	D2C	1111111111111111	RPOR5	D8A	--000000--000000
RPINR0	D04	11111111--------	RPINR21	D2E	1111111111111111	RPOR6	D8C	--000000--000000
RPINR1	D06	1111111111111111	RPINR22	D30	1111111111111111	RPOR7	D8E	--000000--000000
RPINR2	D08	11111111--------	RPINR23	D32	1111111111111111	RPOR8	D90	--000000--000000
RPINR3	D0A	1111111111111111	RPINR26	D38	--------11111111	RPOR9	D92	--000000--000000
RPINR4	D0C	1111111111111111	RPINR30	D40	11111111--------	RPOR10	D94	--000000--000000
RPINR5	D0E	1111111111111111	RPINR37	D4E	11111111--------	RPOR11	D96	--000000--000000
RPINR6	D10	1111111111111111	RPINR38	D50	--------11111111	RPOR12	D98	--000000--000000
RPINR7	D12	1111111111111111	RPINR42	D58	1111111111111111	RPOR13	D9A	--000000--000000
RPINR8	D14	1111111111111111	RPINR43	D5A	1111111111111111	RPOR14	D9C	--000000--000000
RPINR9	D16	1111111111111111	RPINR44	D5C	1111111111111111	RPOR15	D9E	--000000--000000
RPINR10	D18	1111111111111111	RPINR45	D5E	1111111111111111	RPOR16	DA0	--000000--000000
RPINR11	D1A	1111111111111111	RPINR46	D60	1111111111111111	RPOR17	DA2	--000000--000000
RPINR12	D1C	1111111111111111	RPINR47	D62	1111111111111111	RPOR18	DA4	--000000--000000
RPINR13	D1E	1111111111111111	RPOR0	D80	--000000--000000	RPOR19	DA6	--000000--000000
RPINR14	D20	1111111111111111	RPOR1	D82	--000000--000000	RPOR20	DA8	--000000--000000
RPINR15	D22	1111111111111111	RPOR2	D84	--000000--000000	RPOR21	DAA	--000000--000000
RPINR18	D28	1111111111111111	RPOR3	D86	--000000--000000	RPOR22	DAC	--000000--000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

REGISTER 3-4: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(1,3,4)

1111 = Reserved
1110 = User memory bulk erase operation
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0101 = Reserved
0100 = Reserved
0011 = Memory page erase operation
0010 = Memory row program operation
0001 = Memory double-word operation(5)
0000 = Reserved

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (IIDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.

3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

3.5 Master Interrupt Controller

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33CH128MP508 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33CH128MP508 family CPU.

The interrupt controller has the following features:

- Six Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Alternate Interrupt Vector Table (AIVT) for Debug Support

3.5.1 INTERRUPT VECTOR TABLE

The dsPIC33CH128MP508 family Interrupt Vector Table (IVT), shown in Figure 3-17, resides in program memory, starting at location, 000004h. The IVT contains six non-maskable trap vectors and up to 246 sources of interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

3.5.1.1 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 3-18, is available only when the Boot Segment (BS) is defined and the AIVT has been enabled. To enable the Alternate Interrupt Vector Table, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2<8> = 1). When the AIVT is enabled, all interrupt and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment, defined by BSLIM<12:0>. The second half of the page is no longer usable space. The Boot Segment must be at least two pages to enable the AIVT.

Note: Although the Boot Segment must be enabled in order to enable the AIVT, application code does not need to be present inside of the Boot Segment. The AIVT (and IVT) will inherit the Boot Segment code protection.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time.

3.5.2 RESET SEQUENCE

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33CH128MP508 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 3-182: ADFLxCON: ADC DIGITAL FILTER x CONTROL REGISTER (x = 0, 1, 2, 3) (CONTINUED)

bit 4-0 **FLCHSEL<4:0>:** Oversampling Filter Input Channel Selection bits

11111 = Reserved
...
10101 = Reserved
10100 = Band gap, 1.2V (AN20)
10011 = Temperature sensor (AN19)
10010 = SPGA3 (AN18)
10001 = SPGA2 (AN17)
10000 = SPGA1 (AN16)
01111 = AN15
...
00000 = AN0

REGISTER 3-189: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 3-190: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits
This register holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

Note 1: These bits are read-only when the module is executing Step commands.

TABLE 4-14: SLAVE SFR BLOCK E00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O Ports (Continued)			CNEN0B	E2C	0000000000000000	CNPUD	E5E	0000000000000000
ANSELA	E00	----------1111-	CNSTATB	E2E	0000000000000000	CNPDD	E60	0000000000000000
TRISA	E02	----------11111	CNEN1B	E30	0000000000000000	CNCOND	E62	0---0----------
PORTA	E04	----------xxxxx	CNFB	E32	0000000000000000	CNEN0D	E64	0000000000000000
LATA	E06	----------xxxxx	ANSELC	E38	--------11--1111	CNSTATD	E66	0000000000000000
ODCA	E08	----------00000	TRISC	E3A	1111111111111111	CNEN1D	E68	0000000000000000
CNPUA	E0A	----------00000	PORTC	E3C	xxxxxxxxxxxxxxxx	CNFD	E6A	0000000000000000
CNPDA	E0C	----------00000	LATC	E3E	xxxxxxxxxxxxxxxx	ANSELE	E70	---------1------
CNEN0A	E10	----------00000	ODCC	E40	0000000000000000	TRISE	E72	1111111111111111
CNSTATA	E12	----------00000	CNPUC	E42	0000000000000000	PORTE	E74	xxxxxxxxxxxxxxxx
CNEN1A	E14	----------00000	CNPDC	E44	0000000000000000	LATE	E76	xxxxxxxxxxxxxxxx
CNFA	E16	----------00000	CNCONC	E46	0---0----------	ODCE	E78	0000000000000000
ANSELB	E1C	-------11--11111	CNEN0C	E48	0000000000000000	CNPUE	E7A	0000000000000000
TRISB	E1E	1111111111111111	CNSTATC	E4A	0000000000000000	CNPDE	E7C	0000000000000000
PORTB	E20	xxxxxxxxxxxxxxxx	CNEN1C	E4C	0000000000000000	CNCONE	E7E	0---0----------
LATB	E22	xxxxxxxxxxxxxxxx	CNFC	E4E	0000000000000000	CNEN0E	E80	0000000000000000
ODCB	E24	0000000000000000	ANSELD	E54	-11111----------	CNSTATE	E82	0000000000000000
CNPUB	E26	0000000000000000	TRISD	E56	1111111111111111	CNEN1E	E84	0000000000000000
CNPDB	E28	0000000000000000	PORTD	E58	xxxxxxxxxxxxxxxx	CNFE	E86	0000000000000000
CNEN0A	E10	----------00000	LATD	E5A	xxxxxxxxxxxxxxxx			
CNCONB	E2A	0---0----------	ODCD	E5C	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.

TABLE 4-15: SLAVE SFR BLOCK F00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Reset			PMD1	FA4	----000-00000-00	REFOTRIML	FBC	0000000000000000
RCON	F80	00--x-0000000011	PMD2	FA6	--------00000000	REFOTRIMH	FBE	----------------
Oscillator			PMD4	FAA	------------0---	PCTRAPL	FBF	0000000000000000
OSCCON	F84	-000-xxx0-0-0--0	PMD6	FAE	--000000--------	PCTRAPL	FC0	0000000000000000
CLKDIV	F86	00110000--000001	PMD7	FB0	-------x----0---	PCTRAPH	FC2	--------00000000
PLLFBD	F88	----000010010110	PMD8	FB2	---00--0--xx000-			
PLLDIV	F8A	------00-011-001	**WDT**					
APLLFBD1	F90	----000010010110	WDTCONL	FB4	0--0000000000000			
APLLDIV1	F92	------00-011-001	WDTCONH	FB6	0000000000000000			
PMD			REFOCONL	FB8	0-000-00----0000			
PMDCON	FA0	----0----------	REFOCONH	FBA	-000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Reset and address values are in hexadecimal.

REGISTER 4-72: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP57R<5:0>:** Peripheral Output Function is Assigned to S1RP57 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP56R<5:0>:** Peripheral Output Function is Assigned to S1RP56 Output Pin bits (see Table 4-31 for peripheral function numbers)

REGISTER 4-73: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP59R5	RP59R4	RP59R3	RP59R2	RP59R1	RP59R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP58R5	RP58R4	RP58R3	RP58R2	RP58R1	RP58R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP59R<5:0>:** Peripheral Output Function is Assigned to S1RP59 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP58R<5:0>:** Peripheral Output Function is Assigned to S1RP58 Output Pin bits (see Table 4-31 for peripheral function numbers)

TABLE 4-33: PORTA REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELA	—	—	—	—	—	—	—	—	—	—	—	ANSELA<3:1>				—
TRISA	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>				
PORTA	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>				
LATA	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>				
ODCA	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>				
CNPUA	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>				
CNPDA	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>				
CNCONA	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0A	—	—	—	—	—	—	—	—	—	—	—	CNEN0A<4:0>				
CNSTATA	—	—	—	—	—	—	—	—	—	—	—	CNSTATA<4:0>				
CNEN1A	—	—	—	—	—	—	—	—	—	—	—	CNEN1A<4:0>				
CNFA	—	—	—	—	—	—	—	—	—	—	—	CNFA<4:0>				

TABLE 4-34: PORTB REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELB	—	—	—	—	—	—	—	ANSELB<8:7>		—	—	ANSELB<4:0>				
TRISB	TRISB<15:0>															
PORTB	RB<15:0>															
LATB	LATB<15:0>															
ODCB	ODCB<15:0>															
CNPUB	CNPUB<15:0>															
CNPDB	CNPDB<15:0>															
CNCONB	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0B	CNEN0B<15:0>															
CNSTATB	CNSTATB<15:0>															
CNEN1B	CNEN1B<15:0>															
CNFB	CNFB<15:0>															

REGISTER 4-111: ADFLxCON: ADC DIGITAL FILTER x CONTROL REGISTER (x = 0, 1, 2, 3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	HSC/R-0
FLEN	MODE1	MODE0	OVRSAM2	OVRSAM1	OVRSAM0	IE	RDY
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FLCHSEL4	FLCHSEL3	FLCHSEL2	FLCHSEL1	FLCHSEL0
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLEN:** Filter Enable bit
1 = Filter is enabled
0 = Filter is disabled and the RDY bit is cleared

bit 14-13 **MODE<1:0>:** Filter Mode bits
11 = Averaging mode
10 = Reserved
01 = Reserved
00 = Oversampling mode

bit 12-10 **OVRSAM<2:0>:** Filter Averaging/Oversampling Ratio bits
If MODE<1:0> = 00:
111 = 128x (16-bit result in the ADFLxDAT register is in 12.4 format)
110 = 32x (15-bit result in the ADFLxDAT register is in 12.3 format)
101 = 8x (14-bit result in the ADFLxDAT register is in 12.2 format)
100 = 2x (13-bit result in the ADFLxDAT register is in 12.1 format)
011 = 256x (16-bit result in the ADFLxDAT register is in 12.4 format)
010 = 64x (15-bit result in the ADFLxDAT register is in 12.3 format)
001 = 16x (14-bit result in the ADFLxDAT register is in 12.2 format)
000 = 4x (13-bit result in the ADFLxDAT register is in 12.1 format)
If MODE<1:0> = 11 (12-bit result in the ADFLxDAT register in all instances):
111 = 256x
110 = 128x
101 = 64x
100 = 32x
011 = 16x
110 = 8x
001 = 4x
000 = 2x

bit 9 **IE:** Filter Common ADC Interrupt Enable bit
1 = Common ADC interrupt will be generated when the filter result will be ready
0 = Common ADC interrupt will not be generated for the filter

bit 8 **RDY:** Oversampling Filter Data Ready Flag bit
This bit is cleared by hardware when the result is read from the ADFLxDAT register.
1 = Data in the ADFLxDAT register is ready
0 = The ADFLxDAT register has been read and new data in the ADFLxDAT register is not ready

bit 7-5 **Unimplemented:** Read as '0'

EXAMPLE 6-1: CODE EXAMPLE FOR USING MASTER PRIMARY PLL WITH 8 MHz INTERNAL FRC

```
//code example for 50 MIPS system clock using 8MHz FRC
// Select FRC on POR
#pragma  config FNOSC = FRC       // Oscillator Source Selection (Internal Fast RC (FRC))
#pragma  config IESO = OFF
// Enable Clock Switching
#pragma  config FCKSM = CSECMD
int      main()
{
// Configure PLL prescaler, both PLL postscalers, and PLL feedback divider
CLKDIVbits.PLLPRE = 1;            // N1=1
PLLFBDbits.PLLFBDIV = 125;        // M = 125
PLLDIVbits.POST1DIV = 5;          // N2=5
PLLDIVbits.POST2DIV = 1;          // N3=1
// Initiate Clock Switch to FRC with PLL (NOSC=0b001)
__builtin_write_OSCCONH(0x01);
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while    (OSCCONbits.OSWEN!= 0);
}
```

Note: *FPLLO = FPLLI * M/(N1 * N2 * N3); FPLLI = 8; M = 125; N1 = 1; N2 = 5; N3 = 1;* so *FPLLO = 8 * 125/(1 * 5 * 1) = 200 MHz* or *50 MIPS.*

EXAMPLE 6-2: CODE EXAMPLE FOR USING SLAVE PRIMARY PLL WITH 8 MHz INTERNAL FRC

```
//code example for 60 MIPS system clock using 8MHz FRC
// Select Internal FRC at POR
// Select FRC on POR
#pragma config  S1FNOSC = FRC      // Oscillator Source Selection (Internal Fast RC (FRC))
#pragma config  S1IESO = OFF       // Two-speed Oscillator Start-up Enable bit (Start up with
user-selected oscillator source)
// Enable Clock Switching
#pragma config  S1FCKSM = CSECMD
int     main()
{
// Configure PLL prescaler, both PLL postscalers, and PLL feedback divider
CLKDIVbits.PLLPRE = 1;            // N1=1
PLLFBDbits.PLLFBDIV = 150;        // M = 150
PLLDIVbits.POST1DIV = 5;          // N2=5
PLLDIVbits.POST2DIV = 1;          // N3=1
// Initiate Clock Switch to FRC with PLL (NOSC=0b001)
__builtin_write_OSCCONH(0x01);
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while   (OSCCONbits.OSWEN!= 0);
}
```

Note: *FPLLO = FPLLI * M/(N1 * N2 * N3); FPLLI = 8; M = 150; N1 = 1; N2 = 5; N3 = 1;* so *FPLLO = 8 * 150/(1 * 5 * 1) = 240 MHz* or *60 MIPS.*

REGISTER 9-27: PGxTRIGA: PWM GENERATOR x TRIGGER A REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PGxTRIGA<15:0>:** PWM Generator x Trigger A Register bits

REGISTER 9-28: PGxTRIGB: PWM GENERATOR x TRIGGER B REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PGxTRIGB<15:0>:** PWM Generator x Trigger B Register bits

REGISTER 9-29: PGxTRIGC: PWM GENERATOR x TRIGGER C REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGxTRIGC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PGxTRIGC<15:0>:** PWM Generator x Trigger C Register bits

REGISTER 13-14: UxRXCHK: UARTx RECEIVE CHECKSUM REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXCHK<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCHK<7:0>:** Receive Checksum bits (calculated from RX words)

LIN Modes:
C0EN = 1: Sum of all received data + addition carries, including PID.
C0EN = 0: Sum of all received data + addition carries, excluding PID.

LIN Slave:
Cleared when Break is detected.

LIN Master/Slave:
Cleared when Break is detected.

Other Modes:
C0EN = 1: Sum of every byte received + addition carries.
C0EN = 0: Value remains unchanged.

REGISTER 16-2: SENTxSTAT: SENTx STATUS REGISTER (CONTINUED)

bit 0 **SYNCTXEN:** SENTx Synchronization Period Status/Transmit Enable bit(1)

Module in Receive Mode (RCVEN = 1):

1 = A valid synchronization period was detected; the module is receiving nibble data

0 = No synchronization period has been detected; the module is not receiving nibble data

Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):

The bit always reads as '1' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads '0' when the module is disabled.

Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):

1 = The module is transmitting a SENTx data frame

0 = The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission

Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

19.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729) in the *"dsPIC33/PIC24 Family Reference Manual",* which is available from the Microchip web site (www.microchip.com).

2: The CRC module is available only on the Master.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

A simple version of the CRC shift engine is displayed in Figure 19-1. Table 19-1 displays a simplified block diagram of the CRC generator.

TABLE 19-1: CRC MODULE OVERVIEW

	Number of CRC Modules	Identical (Modules)
Master Core	1	Yes
Slave Core	None	NA

FIGURE 19-1: CRC MODULE BLOCK DIAGRAM

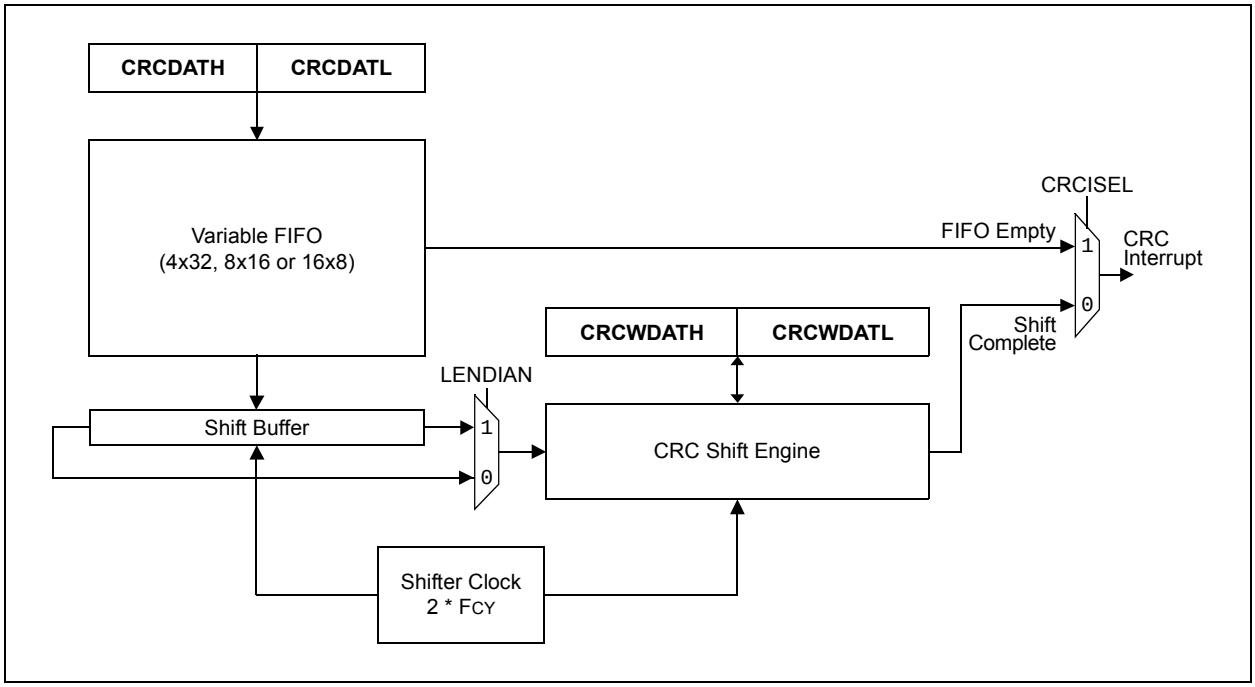


TABLE 24-44: ANALOG-TO-DIGITAL CONVERSION TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(2) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
AD50	TAD	ADC Clock Period	14.28	—	—	ns	
AD51	FTP	Throughput Rate	—	—	3.5	Msps	Dedicated Cores 0 and 1
			—	—	3.5	Msps	Shared core

Note 1: These parameters are characterized but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

TABLE 24-45: HIGH-SPEED ANALOG COMPARATOR MODULE SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(2) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM09	FIN	Input Frequency	400	500	550	MHz	
CM10	VIOFF	Input Offset Voltage	-20	—	+20	mV	
CM11	VICM	Input Common-Mode Voltage Range(1)	AVSS	—	AVDD	V	
CM13	CMRR	Common-Mode Rejection Ratio	60	—	—	dB	
CM14	TRESP	Large Signal Response	—	15	—	ns	V+ input step of 100 mV while V- input is held at AVDD/2
CM15	VHYST	Input Hysteresis	15	30	45	mV	Depends on HYSSEL<1:0>

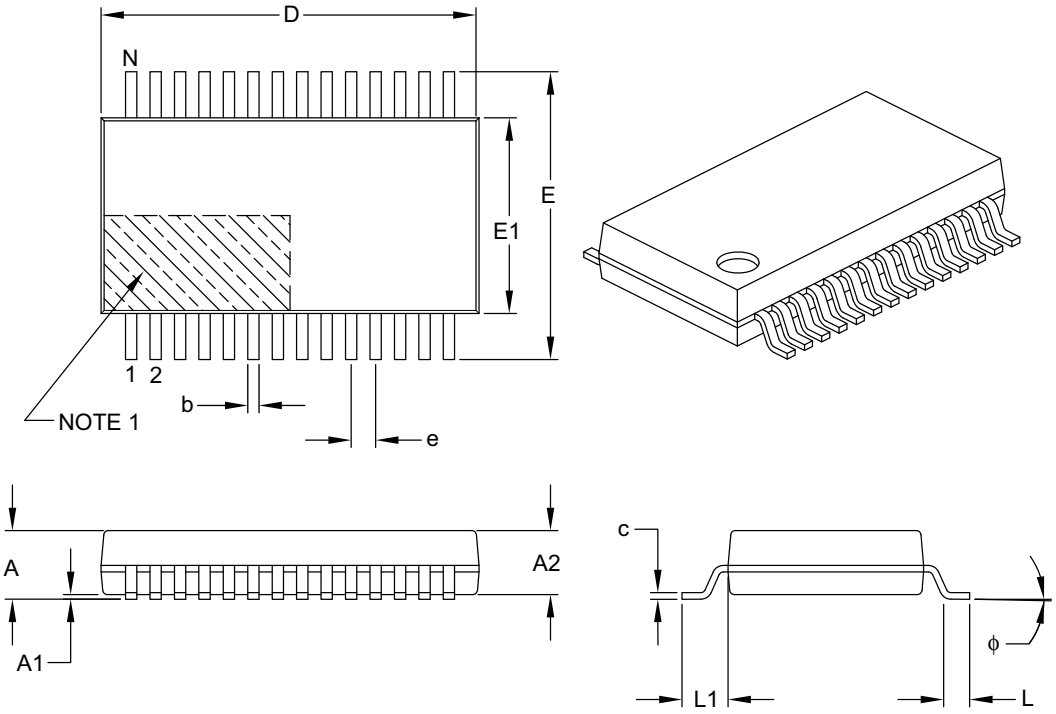
Note 1: These parameters are for design guidance only and are not tested in manufacturing.

2: The comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

25.2 Package Details

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

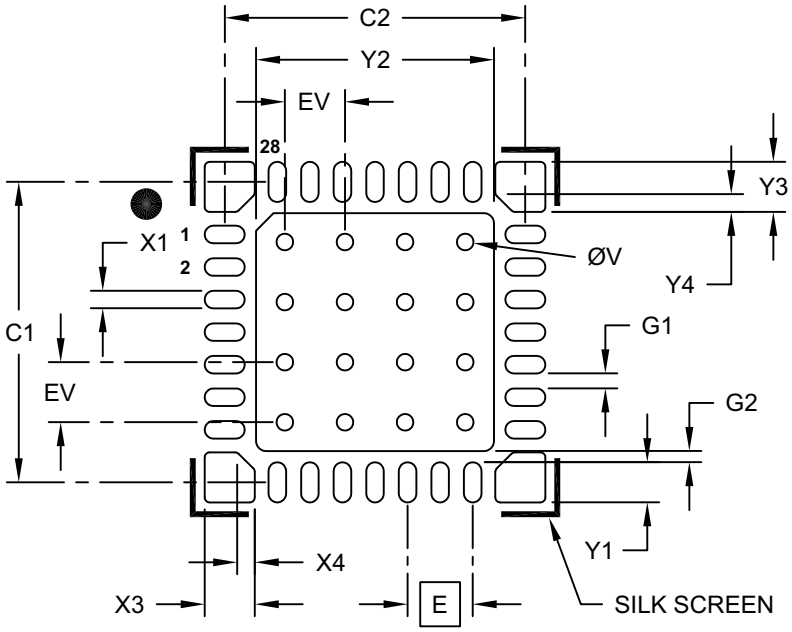
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			4.75
Optional Center Pad Length	Y2			4.75
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.80
Corner Anchor (X4)	X3			1.00
Corner Anchor (X4)	Y3			1.00
Corner Anchor Chamfer (X4)	X4			0.35
Corner Anchor Chamfer (X4)	Y4			0.35
Contact Pad to Pad (X28)	G1	0.20		
Contact Pad to Center Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

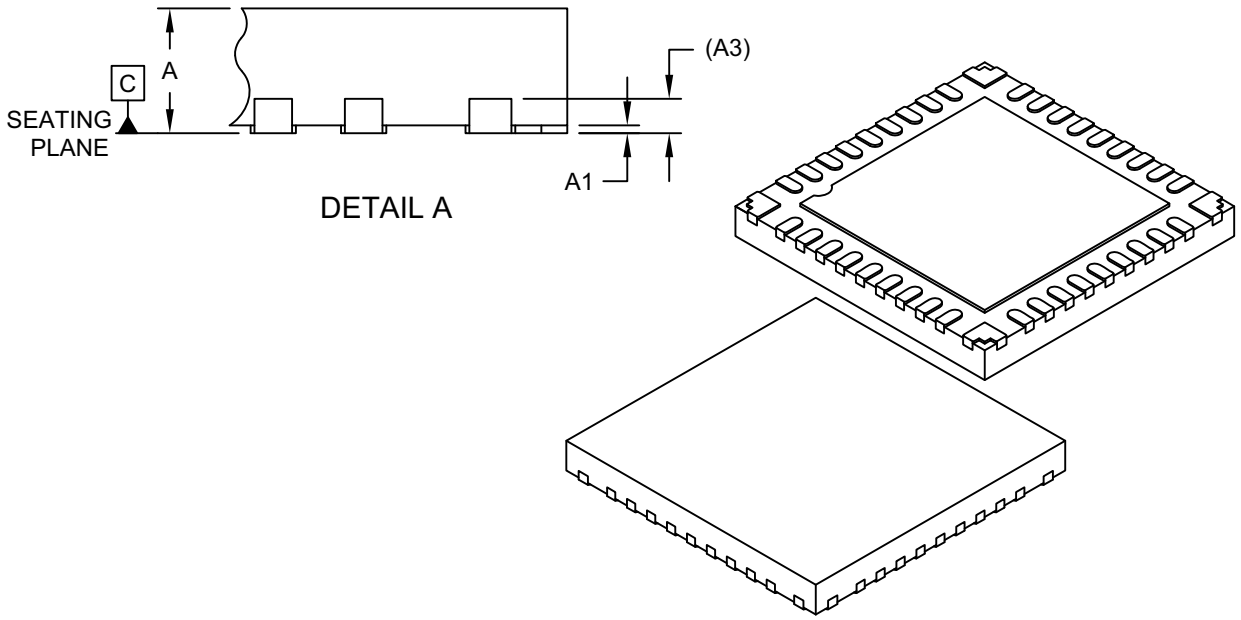
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2385B

36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-436A–M5 Sheet 2 of 2