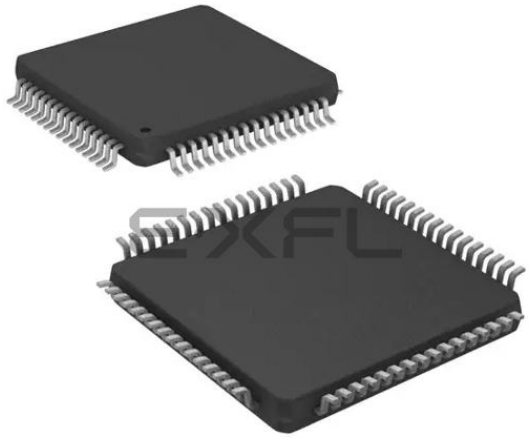
Microchip Technology - DSPIC33CH128MP206-E/PT Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp206-e-pt

3.2.9 INTERFACING PROGRAM AND DATA MEMORY SPACES

The dsPIC33CH128MP508 family architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33CH128MP508 family devices provides two methods by which Program Space can be accessed during operation:

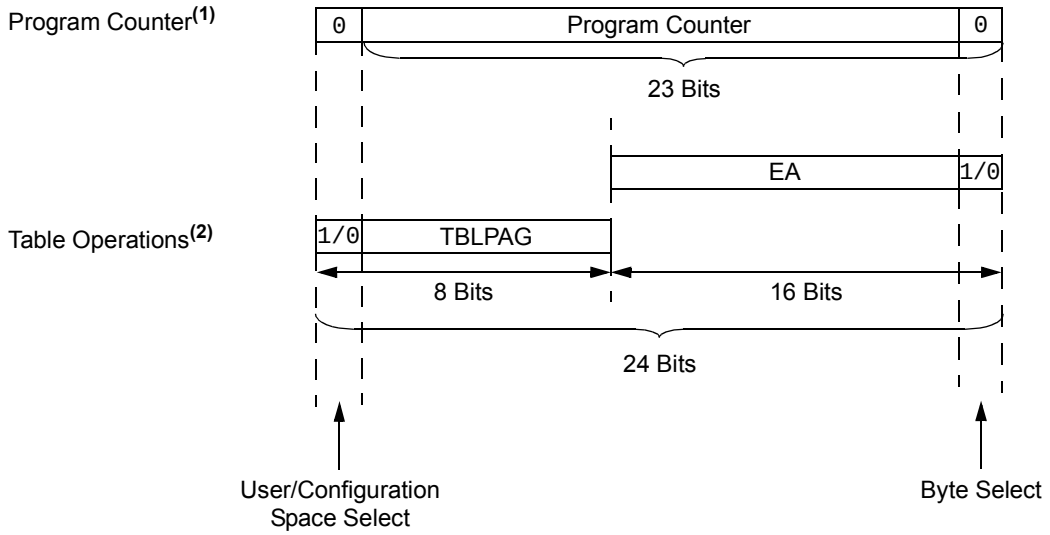
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 3-22: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xxx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 3-12: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

3.4.2 RESET CONTROL REGISTER

REGISTER 3-15: RCON: RESET CONTROL REGISTER(1)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W Register Reset has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

TABLE 3-26: MASTER INTERRUPT PRIORITY REGISTERS (CONTINUED)

Register	Address	Bit 15	Bit14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPC35	886h	—	—	—	—	—	—	—	—	—	S1SRSTIP2	S1SRSTIP1	S1SRSTIP0	—	MSIFLTIP2	MSIFLTIP1	MSIFLTIP0
IPC36	888h	—	—	—	—	—	S1BRKIP2	S1BRKIP1	S1BRKIP0	—	—	—	—	—	—	—	—
IPC37	88Ah	—	—	—	—	—	CCT7IP2	CCT7IP1	CCT7IP0	—	CCP7IP2	CCP7IP1	CCP7IP0	—	—	—	—
IPC38	88Ch	—	—	—	—	—	—	—	—	—	CCT8IP2	CCT8IP1	CCT8IP0	—	CCP8IP2	CCP8IP1	CCP8IP0
IPC39	88Eh	—	—	—	—	—	—	—	—	—	S1CLKFIP2	S1CLKFIP1	S1CLKFIP0	—	—	—	—
IPC40	890h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC41	892h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC42	894h	—	PEVTCIP2	PEVTCIP1	PEVTCIP0	—	PEVTBIP2	PEVTBIP1	PEVTBIP0	—	PEVTAIP2	PEVTAIP1	PEVTAIP0	—	ADFIFOIP2	ADFIFOIP1	ADFIFOIP0
IPC43	896h	—	CLC3PIP2	CLC3PIP1	CLC3PIP0	—	PEVTFIP2	PEVTFIP1	PEVTFIP0	—	PEVTEIP2	PEVTEIP1	PEVTEIP0	—	PEVTDIP2	PEVTDIP1	PEVTDIP0
IPC44	898h	—	CLC3NIP2	CLC3NIP1	CLC3NIP0	—	CLC2NIP2	CLC2NIP1	CLC2NIP0	—	CLC1NIP2	CLC1NIP1	CLC1NIP0	—	CLC4PIP2	CLC4PIP1	CLC4PIP0
IPC45	89Ah	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC4NIP2	CLC4NIP1	CLC4NIP0
IPC46	89Ch	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC47	89Eh	—	—	—	—	—	U2EVTIP2	U2EVTIP1	U2EVTIP0	—	U1EVTIP2	U1EVTIP1	U1EVTIP0	—	—	—	—

Legend: — = Unimplemented.

REGISTER 3-18: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMA Controller Trap Status bit
1 = DMAC error trap has occurred
0 = DMAC error trap has not occurred

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

TABLE 3-30: MASTER REMAPPABLE PIN INPUTS

RPINRx<15:8> or RPINRx<7:0 >	Function	Available on Ports
0	Vss	Internal
1	Master Comparator 1	Internal
2	Slave Comparator 1	Internal
3	Slave Comparator 2	Internal
4	Slave Comparator 3	Internal
5	Slave REFCLKO	Internal
6	Master PTG Trigger 26	Internal
7	Master PTG Trigger 27	Internal
8	Slave PWM Event Output C	Internal
9	Slave PWM Event Output D	Internal
10	Slave PWM Event Output E	Internal
11	Master PWM Event Output C	Internal
12	Master PWM Event Output D	Internal
13	Master PWM Event Output E	Internal
14-31	RP14-RP31	Reserved
32	RP32	Port Pin RB0
33	RP33	Port Pin RB1
34	RP34	Port Pin RB2
35	RP35	Port Pin RB3
36	RP36	Port Pin RB4
37	RP37	Port Pin RB5
38	RP38	Port Pin RB6
39	RP39	Port Pin RB7
40	RP40	Port Pin RB8
41	RP41	Port Pin RB9
42	RP42	Port Pin RB10
43	RP43	Port Pin RB11
44	RP44	Port Pin RB12
45	RP45	Port Pin RB13
46	RP46	Port Pin RB14
47	RP47	Port Pin RB15
48	RP48	Port Pin RC0
49	RP49	Port Pin RC1
50	RP50	Port Pin RC2
51	RP51	Port Pin RC3
52	RP52	Port Pin RC4
53	RP53	Port Pin RC5
54	RP54	Port Pin RC6
55	RP55	Port Pin RC7
56	RP56	Port Pin RC8
57	RP57	Port Pin RC9
58	RP58	Port Pin RC10
59	RP59	Port Pin RC11

REGISTER 3-139: C1FIFOUAHx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) HIGH(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<31:24>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<31:16>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-140: C1FIFOUALx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) LOW(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<15:0>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

FIGURE 3-25: SHARED CORE BLOCK DIAGRAM

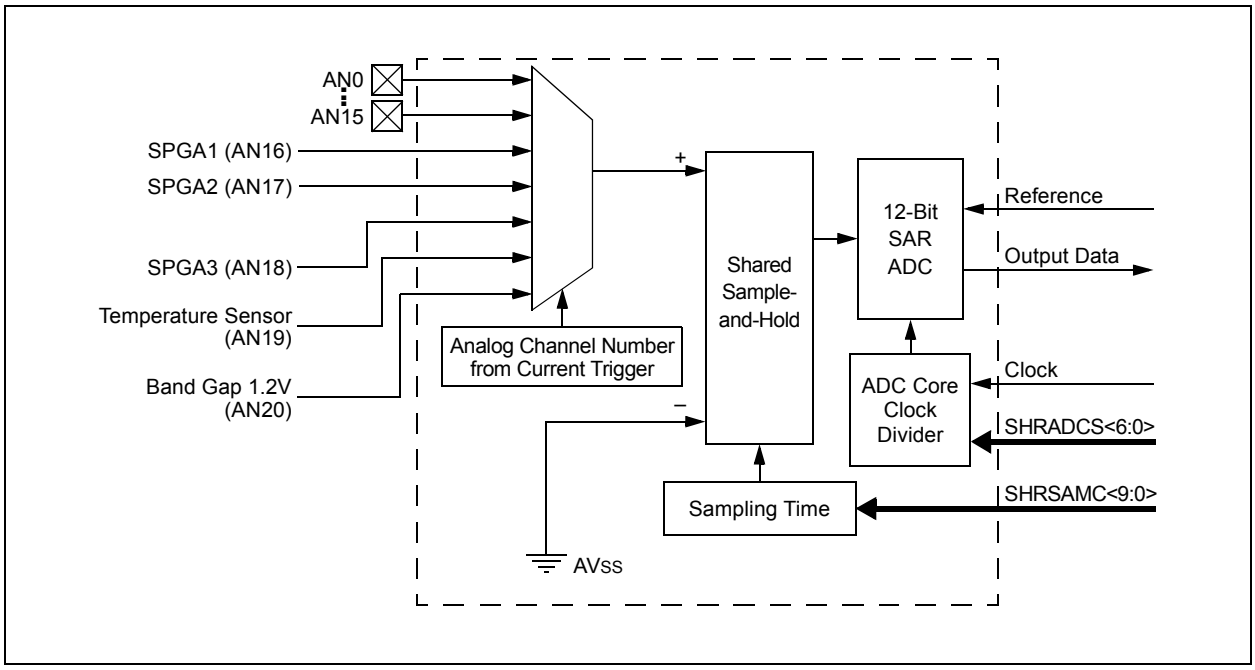
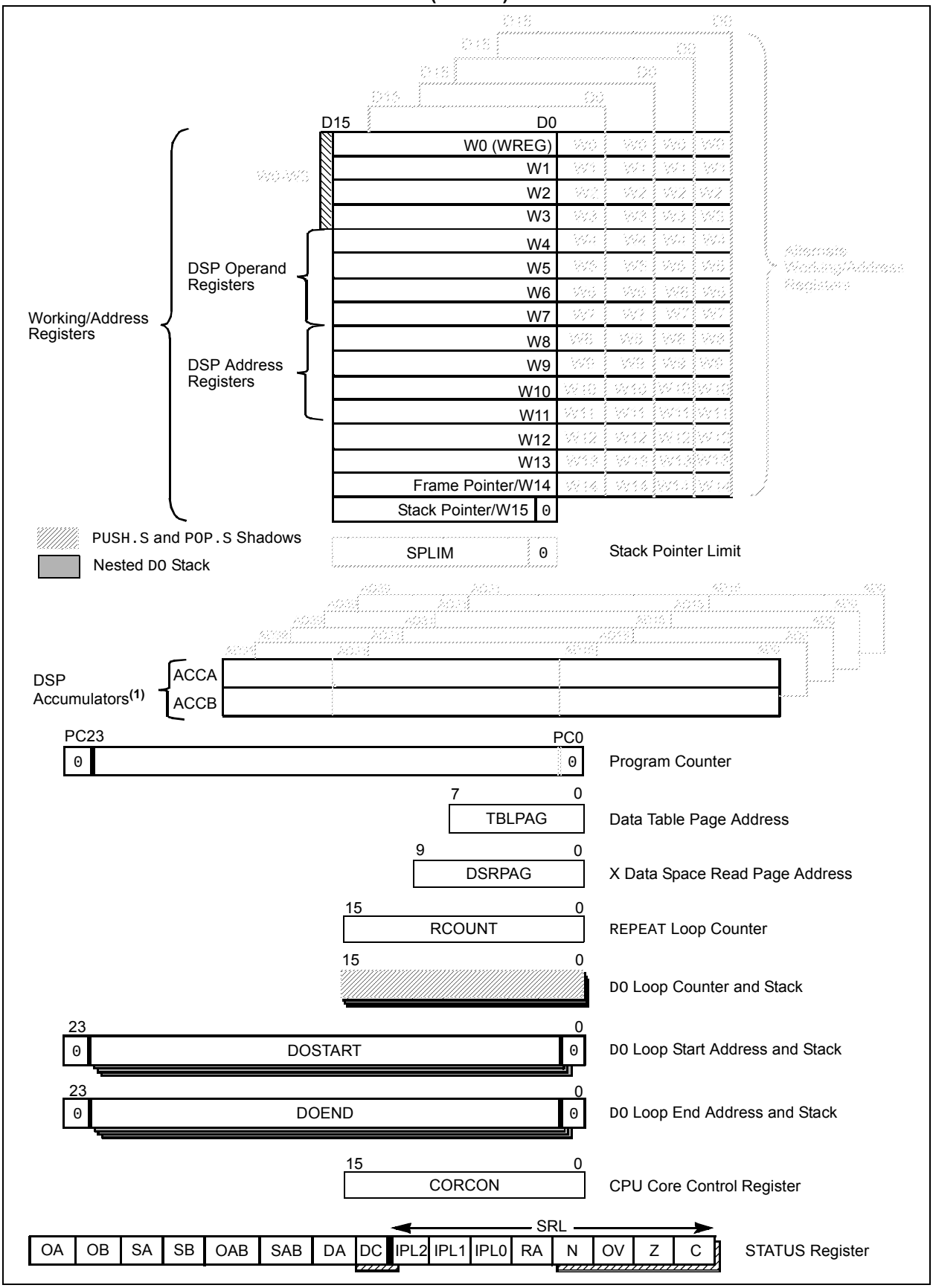


FIGURE 4-2: PROGRAMMER'S MODEL (SLAVE)



4.3.2 RTSP OPERATION

RTSP allows the user application to program one double instruction word, or one row, at a time.

The double instruction word write blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of one double instruction word and 64 double instruction words, respectively.

Note:	Because the PRAM is volatile, RTSP writes that change the Slave PRAM user code will be lost when the device is powered down. For persistent changes to Slave PRAM user code, the Slave image in the Master Flash should be updated.

The basic sequence for RTSP programming is to first load two 24-bit instructions into the NVM write latches found in configuration memory space. Refer to Figure 4-3 for write latch addresses. Then, the WR bit in the NVMCON register is set to initiate the write process. The processor stalls (waits) until the programming operation is finished. The WR bit is automatically cleared when the operation is finished. All program operations may optionally use the NVM interrupt to signal the successful completion of the operation.

Double instruction word writes are performed by manually loading both write latches, using TBLWTL and TBLWTH instructions, and then initiating the NVM write while the NVMOP<3:0> bits (NVMCON<3:0>) are set to '0x1'. The program space destination address is defined by the NVMADR/U registers.

EXAMPLE 4-1: PRAM WRITE/READ

```
//Sample code for PRAM write
// Writing 0x777777 to location 0x3000
    NVMCON = 0x4001;
    TBLPAG = 0xFA;                    // write latch upper address
    NVMADR = 0x3000;                  // set target write address of general segment
    NVMADRU = 0x0000;
    __builtin_tblwtl(0, 0x7777);      // load write latches
    __builtin_tblwth (0,0x77);

    __builtin_tblwtl(2, 0x7777);      // load write latches
    __builtin_tblwth (2,0x77);

    asm volatile ("disi #5");
    __builtin_write_NVM();

    while(_WR == 1 ) ;
// Sample code for reading address location 0x3000
//readDataL /readDataLH need to be defined as variables.
    TBLPAG = 0x0000;
    readDataL = __builtin_tblrdl(0x3000);
    readDataH = __builtin_tblrdh(0x0000);
```

TABLE 4-37: PORTE REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSLE	—	—	—	—	—	—	—	—	—	ANSELE6	—	—	—	—	—	—
TRISE	TRISE<15:0>															
PORTE	RE<15:0>															
LATE	LATE<15:0>															
ODCE	ODCE<15:0>															
CNPUE	CNPUE<15:0>															
CNPDE	CNPDE<15:0>															
CNCONE	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0E	CNEN0E<15:0>															
CNSTATE	CNSTATE<15:0>															
CNEN1E	CNEN1E<15:0>															
CNFE	CNFE<15:0>															

REGISTER 6-6: ACLKCON1: AUXILIARY CLOCK CONTROL REGISTER (MASTER)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
APLLEN(1)	APLLCK	—	—	—	—	—	FRCSEL
bit 15							bit 8

U-0	U-0	r-0	r-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	—	APLLPRE3	APLLPRE2	APLLPRE1	APLLPRE0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **APLLEN:** Auxiliary PLL Enable/Bypass select bit(1)
1 = AFPLLO is connected to the APLL post-divider output (bypass disabled)
0 = AFPLLO is connected to the APLL input clock (bypass enabled)

bit 14 **APLLCK:** APLL Phase-Locked State Status bit
1 = Auxiliary PLL is in lock
0 = Auxiliary PLL is not in lock

bit 13-9 **Unimplemented:** Read as '0'

bit 8 **FRCSEL:** FRC Clock Source Select bit
1 = FRC is the clock source for APLL
0 = Primary Oscillator is the clock source for APLL

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **Reserved:** Maintain as '0'

bit 3-0 **APLLPRE<3:0>:** Auxiliary PLL Phase Detector Input Divider bits
1111 = Reserved
...
1001 = Reserved
1000 = Input divided by 8
0111 = Input divided by 7
0110 = Input divided by 6
0101 = Input divided by 5
0100 = Input divided by 4
0011 = Input divided by 3
0010 = Input divided by 2
0001 = Input divided by 1 (power-on default selection)
0000 = Reserved

Note 1: Even with the APLLEN bit set, another peripheral must generate a clock request before the APLL will start.

TABLE 7-2: MASTER PMD REGISTERS

Register	Bit 15	Bit14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMDCONL	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—
PMD1	—	—	—	—	T1MD	QEIMD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	ADC1MD
PMD2	—	—	—	—	—	—	—	—	CCP8MD	CCP7MD	CCP6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
PMD3	—	—	—	—	—	—	—	—	CRCMD	—	—	—	—	—	I2C2MD	—
PMD4	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—
PMD6	—	—	DMA5MD	DMA4MD	DMA3MD	DMA2MD	DMA1MD	DMA0MD	—	—	—	—	—	—	—	—
PMD7	—	—	—	—	—	—	—	CMP1MD	—	—	—	—	PTGMD	—	—	—
PMD8	—	—	—	SENT2MD	SENT1MD	—	—	—	—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	BIASMD	—

TABLE 7-3: SLAVE PMD REGISTERS

Register	Bit 15	Bit14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMDCON	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—
PMD1	—	—	—	—	T1MD	QEIMD	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADC1MD
PMD2	—	—	—	—	—	—	—	—	—	—	—	—	CCP4MD	CCP3MD	CCP2MD	CCP1MD
PMD4	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—
PMD6	—	—	—	—	—	—	DMA1MD	DMA0MD	—	—	—	—	—	—	—	—
PMD7	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	PGA1MD	—
PMD8	—	PGA3MD	—	—	—	PGA2MD	—	—	—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	—

REGISTER 9-2: FSCL: FREQUENCY SCALE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSCL<15:0>:** Frequency Scale Register bits
The value in this register is added to the frequency scaling accumulator at each pwm_clk. When the accumulated value exceeds the value of FSMINPER, a clock pulse is produced.

REGISTER 9-3: FSMINPER: FREQUENCY SCALING MINIMUM PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSMINPER<15:0>:** Frequency Scaling Minimum Period Register bits
This register holds the minimum clock period (maximum clock frequency) that can be produced by the frequency scaling circuit.

REGISTER 14-7: SPIxIMSKH: SPIx INTERRUPT MASK REGISTER HIGH

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXWIEN	—	RXMSK5(1)	RXMSK4(1,4)	RXMSK3(1,3)	RXMSK2(1,2)	RXMSK1(1)	RXMSK0(1)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXWIEN	—	TXMSK5(1)	TXMSK4(1,4)	TXMSK3(1,3)	TXMSK2(1,2)	TXMSK1(1)	TXMSK0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RXWIEN:** Receive Watermark Interrupt Enable bit
1 = Triggers receive buffer element watermark interrupt when RXMSK<5:0> ≤ RXELM<5:0>
0 = Disables receive buffer element watermark interrupt

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RXMSK<5:0>:** RX Buffer Mask bits(1,2,3,4)
RX mask bits; used in conjunction with the RXWIEN bit.

bit 7 **TXWIEN:** Transmit Watermark Interrupt Enable bit
1 = Triggers transmit buffer element watermark interrupt when TXMSK<5:0> = TXELM<5:0>
0 = Disables transmit buffer element watermark interrupt

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TXMSK<5:0>:** TX Buffer Mask bits(1,2,3,4)
TX mask bits; used in conjunction with the TXWIEN bit.

Note 1: Mask values higher than FIFODEPTH are not valid. The module will not trigger a match for any value in this case.
2: RXMSK2 and TXMSK2 bits are only present when FIFODEPTH = 8 or higher.
3: RXMSK3 and TXMSK3 bits are only present when FIFODEPTH = 16 or higher.
4: RXMSK4 and TXMSK4 bits are only present when FIFODEPTH = 32.

REGISTER 21-25: FS1OSCSEL CONFIGURATION REGISTER (SLAVE)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

R/PO-1	U-1	U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1
S1IESO	—	—	—	—	S1FNOSC2	S1FNOSC1	S1FNOSC0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **S1IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6-3 **Unimplemented:** Read as ‘1’

bit 2-0 **S1FNOSC<2:0>:** Oscillator Selection bits
111 = Fast RC Oscillator (FRC) divided by N
110 = Backup FRC (BFRC)
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator with PLL Module (MSPLL, HSPLL, ECPLL)
010 = Primary Oscillator (MS, HS, EC)
001 = Fast RC Oscillator (FRC) with PLL Module (FRCPLL)
000 = Fast RC Oscillator (FRC)

TABLE 24-26: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS10	FIN	External CLKI Frequency (External Clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC
		Oscillator Crystal Frequency	3.5	—	10	MHz	XT
			10	—	32	MHz	HS
OS20	TOSC	TOSC = 1/FOSC	15.6	—	DC	ns	
OS25	TCY	Instruction Cycle Time(2)	10	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x TOSC	—	0.55 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3,4)	—	5.4	—	ns	
OS41	TckF	CLKO Fall Time(3,4)	—	6.4	—	ns	
OS42	GM	External Oscillator Transconductance(3)	2.7	—	4	mA/V	XTCFG<1:0> = 00, XTBST = 0
			4	—	7	mA/V	XTCFG<1:0> = 00, XTBST = 1
			4.5	—	7	mA/V	XTCFG<1:0> = 01, XTBST = 0
			6	—	11.9	mA/V	XTCFG<1:0> = 01, XTBST = 1
			5.9	—	9.7	mA/V	XTCFG<1:0> = 10, XTBST = 0
			6.9	—	15.9	mA/V	XTCFG<1:0> = 10, XTBST = 1
			6.7	—	12	mA/V	XTCFG<1:0> = 11, XTBST = 0
			7.5	—	19	mA/V	XTCFG<1:0> = 11, XTBST = 1

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an External Clock applied to the OSCI pin. When an External Clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin.

4: This parameter is characterized but not tested in manufacturing.

TABLE 24-32: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period	—	200	—	µs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSCI period
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	1.5	—	µs	
SY20	TMCLR	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	µs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	µs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	40	µs	Clock fail to BFRC switch
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	—	—	15	µs	From POR event
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	50	µs	From Reset event

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

TABLE 24-40: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(4)**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 x (VDD/5.5V)	300	ns	
			1 MHz mode(2)	—	120	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	120	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	50	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY (BRG + 1)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY (BRG + 1)	—	µs	
			400 kHz mode	TCY (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY (BRG + 1)	—	µs	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3450	ns	
			400 kHz mode	—	900	ns	
			1 MHz mode(2)	—	450	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 3)**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

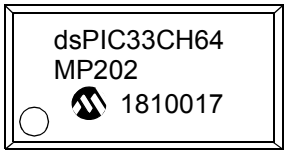
4: These parameters are characterized but not tested in manufacturing.

25.0 PACKAGING INFORMATION

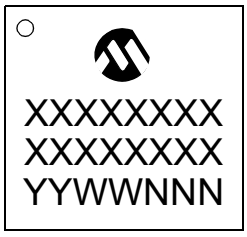
25.1 Package Marking Information

28-Lead SSOP (5.30 mm)

Example

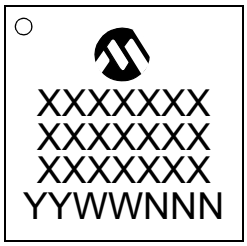


28-Lead UQFN (6x6 mm)



Example

36-Lead UQFN (5x5 mm)



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.