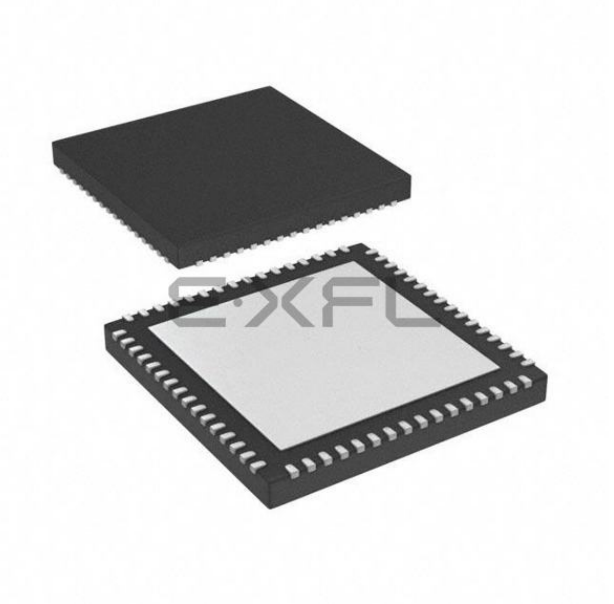

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp206-i-mr

TABLE 3: dsPIC33CHXXXMP20X FAMILY WITH NO CAN FD

Product	Core	Pins	Flash[(1)]	Data RAM	ADC Modules	ADC Channels	Timers	SCCP	CAN FD	SENT	UART	SPI/I^{2}S	I^{2}C	QEI	CLC	PTG	CRC	PWM (High Resolution)	Analog Comparators	PGA	Current Bias Source	REFO
dsPIC33CH64MP202	Master	28	64K	16K	1	12	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP202	Master	28	128K	16K	1	12	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP203	Master	36	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP203	Master	36	128K	16K	1	15	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP205	Master	48	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP205	Master	48	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP206	Master	64	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP206	Master	64	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP208	Master	80	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP208	Master	80	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1

Note 1: For the Slave core, the implemented program memory of 24K is PRAM.

TABLE 8: 64-PIN TQFP/QFN (CONTINUED)

Pin #	Master Core	Slave Core
51	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
52	**RP58**/RC10	**S1RP58**/S1PWM1H/S1RC10
53	**RP59**/RC11	**S1RP59**/S1PWM1L/S1RC11
54	**RP68**/RD4	**S1RP68**/S1PWM3H/S1RD4
55	**RP67**/RD3	**S1RP67**/S1PWM3L/S1RD3
56	V_{SS}	V_{SS}
57	V_{DD}	V_{DD}
58	**RP66**/RD2	**S1RP66**/S1PWM8L/S1RD2
59	**RP65**/RD1	**S1RP65**/S1PWM4H/S1RD1
60	**RP64**/RD0	**S1RP64**/S1PWM4L/S1RD0
61	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1RB10
62	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1RB11
63	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1RB12
64	**RP45**/PWM2L/RB13	**S1RP45**/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

TABLE 9: 80-PIN TQFP (CONTINUED)

Pin #	Master Core	Slave Core
51	VDD	VDD
52	**RP71**/RD7	**S1RP71**/S1PWM8H/S1RD7
53	**RP70**/RD6	**S1RP70**/S1PWM6H/S1RD6
54	**RP69**/RD5	**S1RP69**/S1PWM6L/S1RD5
55	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
56	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
57	RE10	S1RE10
58	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
59	RE11	S1RE11
60	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
61	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
62	ASCL2/RE12	S1RE12
63	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
64	ASDA2/RE13	S1RE13
65	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
66	**RP58**/RC10	**S1RP58**/S1PWM1H/S1RC10
67	**RP59**/RC11	**S1RP59**/S1PWM1L/S1RC11
68	**RP68**/RD4	**S1RP68**/S1PWM3H/S1RD4
69	**RP67**/RD3	**S1RP67**/S1PWM3L/S1RD3
70	VSS	VSS
71	VDD	VDD
72	**RP66**/RD2	**S1RP66**/S1PWM8L/S1RD2
73	**RP65**/RD1	**S1RP65**/S1PWM4H/S1RD1
74	**RP64**/RD0	**S1RP64**/S1PWM4L/S1RD0
75	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1RB10
76	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1RB11
77	RE14	S1RE14
78	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1RB12
79	RE15	S1RE15
80	**RP45**/PWM2L/RB13	**S1RP45**/S1RB13

Legend: RPn and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

3.2 Master Memory Organization

Note:	This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33E/PIC24E Program Memory"** (DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33CH128MP508 family architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

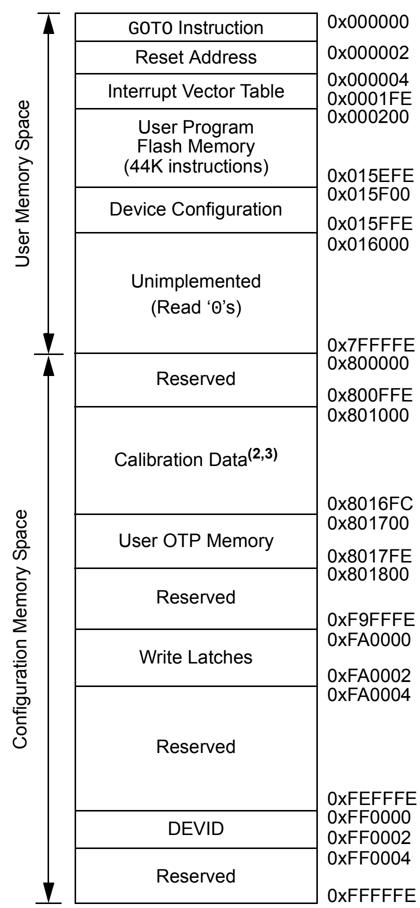
3.2.1 PROGRAM ADDRESS SPACE

The program address memory space of the dsPIC33CH128MP508 family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 3.2.9 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to permit access to calibration data and Device ID sections of the configuration memory space.

The program memory maps for the Master dsPIC33CHXXXMPX08 device are shown in Figure 3-3 and Figure 3-4.

FIGURE 3-3: PROGRAM MEMORY MAP FOR MASTER dsPIC33CH128MPXXX DEVICES(1)



Note 1: Memory areas are not shown to scale.
2: Calibration data area must be maintained during programming.
3: Calibration data area includes UDID locations.

3.2.1.1 Program Memory Organization

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 3-5).

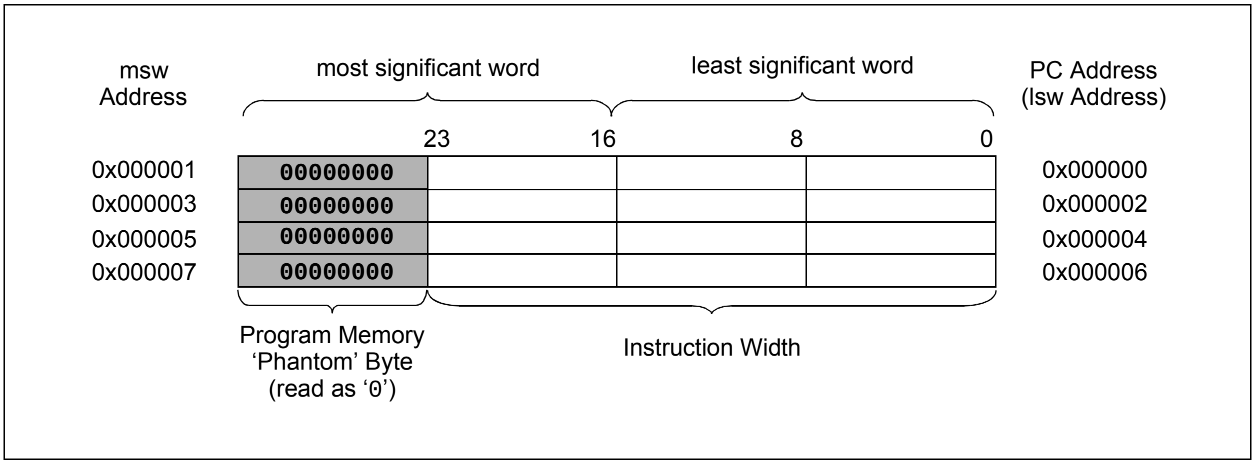
Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented, by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

3.2.1.2 Interrupt and Trap Vectors

All dsPIC33CH128MP508 family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 3.5 “Master Interrupt Controller”**.

FIGURE 3-5: PROGRAM MEMORY ORGANIZATION



3.2.2 UNIQUE DEVICE IDENTIFIER (UDID)

All dsPIC33CH128MP508 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

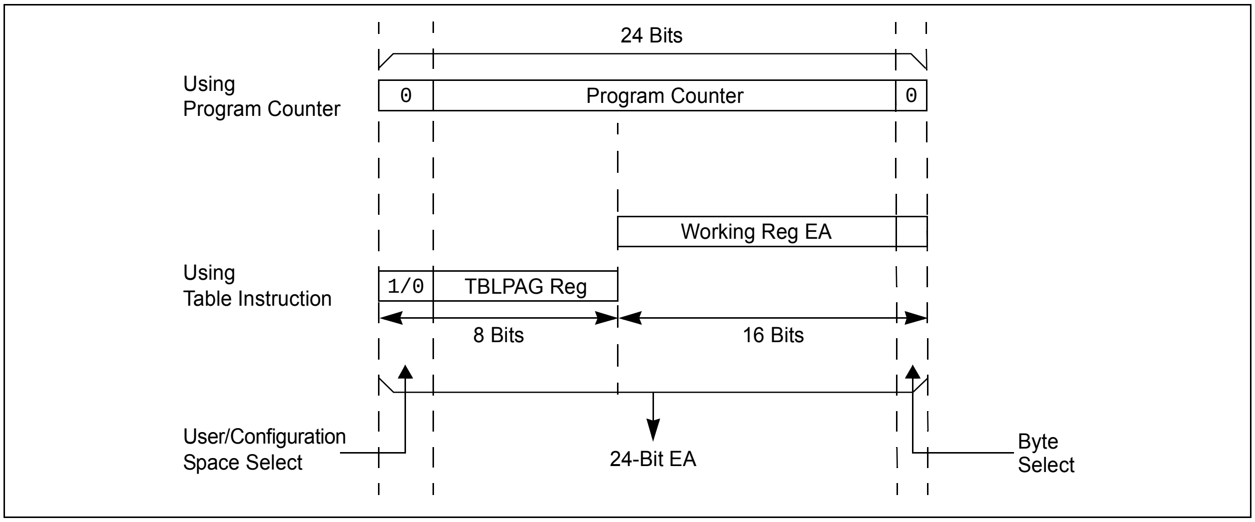
The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

The UDID is stored in five read-only locations, located between 0x801200 and 0x801208 in the device configuration space. Table 3-3 lists the addresses of the identifier words and shows their contents

TABLE 3-3: UDID ADDRESSES

UDID	Address	Description
UDID1	0x801200	UDID Word 1
UDID2	0x801202	UDID Word 2
UDID3	0x801204	UDID Word 3
UDID4	0x801206	UDID Word 4
UDID5	0x801208	UDID Word 5

FIGURE 3-14: ADDRESSING FOR TABLE REGISTERS



REGISTER 3-13: ECCSTATL: ECC SYSTEM STATUS DISPLAY REGISTER LOW

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SECOUT<7:0>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SECIN<7:0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SECOUT<7:0>:** Calculated Single Error Correction Parity Value bits

bit 7-0 **SECIN<7:0>:** Read Single Error Correction Parity Value bits
Bits are the actual parity value of a Flash read operation.

REGISTER 3-14: ECCSTATH: ECC SYSTEM STATUS DISPLAY REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
—	—	—	—	—	—	DEDOUT	DEDIN
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SECSYND<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **DEDOUT:** Calculated Dual Bit Error Detection Parity bit

bit 8 **DEDIN:** Read Dual Bit Error Detection Parity bit

bit 7-0 **SECSYND<7:0>:** Calculated ECC Syndrome Value bits
Indicates the bit location that contains the error.

TABLE 3-23: MASTER INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
T1 – Timer1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
CNA – Change Notice Interrupt A	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
CNB – Change Notice Interrupt B	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
Reserved	13	5	0x00001E	—	—	—
CCP1 – Input Capture/Output Compare 1	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
CCT1 – CCP1 Timer	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
DMA1 – DMA Channel 1	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1RX – SPI1 Receiver	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1TX – SPI1 Transmitter	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
ECCSBE – ECC Single Bit Error	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
NVM – NVM Write Complete	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
INT1 – External Interrupt 1	23	15	0x000032	IFS0<15>	IEC0<15>	IPC3<14:12>
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
DMA2 – DMA Channel 2	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CNC – Change Notice Interrupt C	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT2 – External Interrupt 2	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
DMA3 – DMA Channel 3	29	21	0x00003E	IFS1<5>	IEC1<5>	IPC5<6:4>
DMA4 – DMA Channel 4	30	22	0x000040	IFS1<6>	IEC1<6>	IPC5<10:8>
CCP2 – Input Capture/Output Compare 2	31	23	0x000042	IFS1<7>	IEC1<7>	IPC5<14:12>
CCT2 – CCP2 Timer	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
CAN1 – CAN1 Combined Error	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
INT3 – External Interrupt 3	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
U2RX – UART2 Receiver	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
U2TX – UART2 Transmitter	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
SPI2RX – SPI2 Receiver	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
SPI2TX – SPI2 Transmitter	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
C1RX – CAN1 RX Data Ready	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
Reserved	40-41	32-33	0x000054-0x000056	—	—	—
DMA5 – DMA Channel 5	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
CCP3 – Input Capture/Output Compare 3	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
CCT3 – CCP3 Timer	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
SI2C2 – I2C2 Slave Event	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
MI2C2 – I2C2 Master Event	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47	39	0x000062	—	—	—
CCP4 – Input Capture/Output Compare 4	48	40	0x000064	IFS2<8>	IEC2<8>	IPC10<2:0>
CCT4 – CCP4 Timer	49	41	0x000066	IFS2<9>	IEC2<9>	IPC10<6:4>
Reserved	50	42	0x000068	—	—	—
CCP5 – Input Capture/Output Compare 5	51	43	0x00006A	IFS2<11>	IEC2<11>	IPC10<14:12>
CCT5 – CCP5 Timer	52	44	0x00006C	IFS2<12>	IEC2<12>	IPC11<2:0>
DMT – Deadman Timer	53	45	0x00006E	IFS2<13>	IEC2<13>	IPC11<6:4>
CCP6 – Input Capture/Output Compare 6	54	46	0x000070	IFS2<14>	IEC2<14>	IPC11<10:8>
CCT6 – CCP6 Timer	55	47	0x000072	IFS2<15>	IEC2<15>	IPC11<14:12>

REGISTER 3-28: CNPUx: CHANGE NOTIFICATION PULL-UP ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNPUx<15:0>:** Change Notification Pull-up Enable for PORTx bits
1 = The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection
0 = The pull-up for PORTx[n] is disabled

REGISTER 3-29: CNPDx: CHANGE NOTIFICATION PULL-DOWN ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNPDx<15:0>:** Change Notification Pull-Down Enable for PORTx bits
1 = The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled)
0 = The pull-down for PORTx[n] is disabled

4.1.5 PROGRAMMER'S MODEL

The programmer's model for the dsPIC33CH128MP508S1 family is shown in Figure 4-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 4-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33CH128MP508S1 devices contain control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Figure 4-3.

TABLE 4-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate 1 Working Register Array
W0 through W14(1)	Alternate 2 Working Register Array
W0 through W14(1)	Alternate 3 Working Register Array
W0 through W14(1)	Alternate 4 Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators (Additional 4 Alternate Accumulators)
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Counter Register
DOSTARTH(2), DOSTARTL(2)	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-31: OUTPUT SELECTION FOR REMAPPABLE PINS (S1RPn)

Function	RPnR<5:0>	Output Name
Default PORT	000000	S1RPn tied to Default Pin
S1U1TX	000001	S1RPn tied to UART1 Transmit
$\overline{\text{S1U1RTS}}$	000010	S1RPn tied to UART1 Request-to-Send
S1SDO1	000101	S1RPn tied to SPI1 Data Output
S1SCK1OUT	000110	S1RPn tied to SPI1 Clock Output
$\overline{\text{S1SS1OUT}}$	000111	S1RPn tied to SPI1 Slave Select
S1REFCLKO	001110	S1RPn tied to Reference Clock Output
S1OCM1	001111	S1RPn tied to SCCP1 Output
S1OCM2	010000	S1RPn tied to SCCP2 Output
S1OCM3	010001	S1RPn tied to SCCP3 Output
S1OCM4	010010	S1RPn tied to SCCP4 Output
S1CMP1	010111	S1RPn tied to Comparator 1 Output
S1CMP2	011000	S1RPn tied to Comparator 2 Output
S1CMP3	011001	S1RPn tied to Comparator 3 Output
S1PWMH4	100010	S1RPn tied to PWM4H Output
S1PWML4	100011	S1RPn tied to PWM4L Output
S1PWMEA	100100	S1RPn tied to PWM Event A Output
S1PWMEB	100101	S1RPn tied to PWM Event B Output
S1QEICMP1	100110	S1RPn tied to QEI Comparator Output
S1CLC1OUT	101000	S1RPn tied to CLC1 Output
S1CLC2OUT	101001	S1RPn tied to CLC2 Output
S1PWMEC	101100	S1RPn tied to PWM Event C Output
S1PWMED	101101	S1RPn tied to PWM Event D Output
MPTGTRG1	101110	Master PTG24 Output
MPTGTRG2	101111	Master PTG25 Output
S1CLC3OUT	110010	S1RPn tied to CLC3 Output

REGISTER 4-82: RPOR22: PERIPHERAL PIN SELECT OUTPUT REGISTER 22

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP175R5(1)	RP175R4(1)	RP175R3(1)	RP175R2(1)	RP175R1(1)	RP175R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP174R5(1)	RP174R4(1)	RP174R3(1)	RP174R2(1)	RP174R1(1)	RP174R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

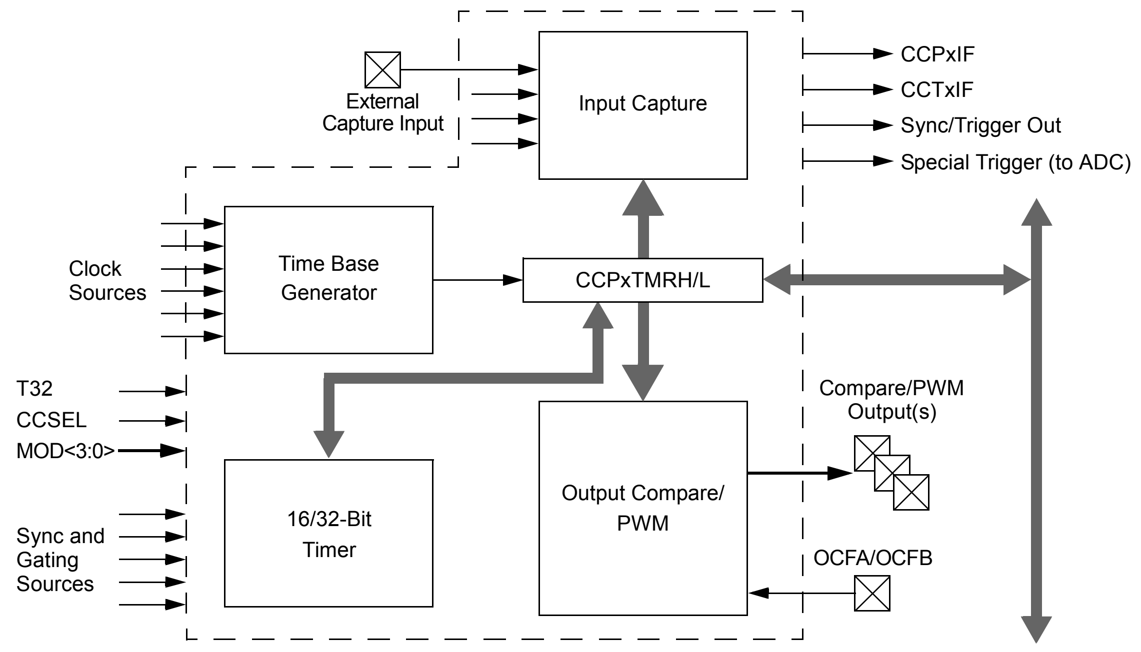
bit 13-8 **RP175R<5:0>:** Peripheral Output Function is Assigned to S1RP175 Output Pin bits(1)
(see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP174R<5:0>:** Peripheral Output Function is Assigned to S1RP174 Output Pin bits(1)
(see Table 4-31 for peripheral function numbers)

Note 1: These are virtual output ports.

FIGURE 10-1: SCCPx CONCEPTUAL BLOCK DIAGRAM

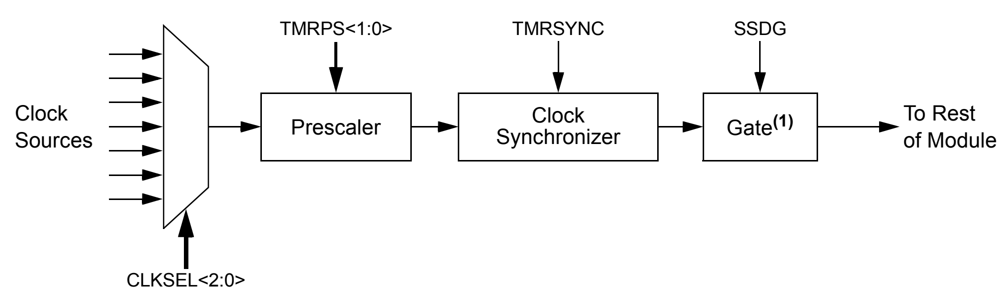


10.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 10-2.

There are eight inputs available to the clock generator, which are selected using the CLKSEL<2:0> bits (CCPxCON1L<10:8>). Available sources include the FRC and LPRC, the Secondary Oscillator and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL<2:0> = `000`).

FIGURE 10-2: TIMER CLOCK GENERATOR



Note 1: Gating is available in Timer modes only.

11.0 HIGH-SPEED ANALOG COMPARATOR WITH SLOPE COMPENSATION DAC

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed Analog Comparator Module"** (DS70005280) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 3.2 "Master Memory Organization"** in this data sheet for device-specific register and bit information.

3: The comparator and DAC are identical for both Master core and Slave core. The module is similar for both Master core and Slave core (where the x represents the number of the specific modules being addressed in Master or Slave).

The high-speed analog comparator module provides a method to monitor voltage, current and other critical signals in a power conversion application that may be too fast for the CPU and ADC to capture. There are a total of four comparator modules, one of which is controlled by the Master core and the remaining three by the Slave core. The analog comparator module can be used to implement Peak Current mode control, Critical Conduction mode (variable frequency) and Hysteretic Control mode. Table 11-1 shows an overview of the comparator/DAC module.

TABLE 11-1: COMPARATOR/DAC MODULE OVERVIEW

	Number of Comparator Modules	Identical (Modules)
Master Core	1	Yes
Slave Core	3	Yes

11.1 Overview

The high-speed analog comparator module is comprised of a high-speed comparator, Pulse Density Modulation (PDM) DAC and a slope compensation unit. The slope compensation unit provides a user-defined slope which can be used to alter the DAC output. This feature is useful in applications, such as Peak Current mode control, where slope compensation is required to maintain the stability of the power supply. The user simply specifies the direction and rate of change for the slope compensation and the output of the DAC is modified accordingly.

The DAC consists of a PDM unit, followed by a digitally controlled multiphase RC filter. The PDM unit uses a phase accumulator circuit to generate an output stream of pulses. The density of the pulse stream is proportional to the input data value, relative to the maximum value supported by the bit width of the accumulator. The output pulse density is representative of the desired output voltage. The pulse stream is filtered with an RC filter to yield an analog voltage. The output of the DAC is connected to the negative input of the comparator. The positive input of the comparator can be selected using a MUX from either of the input pins or the output of the PGAs. The comparator provides a high-speed operation with a typical delay of 15 ns.

The output of the comparator is processed by the pulse stretcher and the digital filter blocks, which prevent comparator response to unintended fast transients in the inputs. Figure 11-1 shows a block diagram of the high-speed analog comparator module. The DAC module can be operated in one of three modes: Slope Generation mode, Hysteretic mode and Triangle Wave mode. Each of these modes can be used in a variety of power supply applications.

Note: The DACOUT pin can only be associated with a single DAC or PGA output at any given time. If more than one DACOEN bit is set, or the PGA Output Enable bit (PGAOEN) and the DACOEN bit are set, the DACOUT pin will be a combination of the signals.

Note: DAC input frequency needs to be 500 MHz.

REGISTER 11-9: SLPxCONL: DACx SLOPE CONTROL LOW REGISTER (CONTINUED)

bit 11-8 **SLPSTOPA<3:0>:** Slope Stop A Signal Select bits

The selected Slope Stop A signal is logically OR'd with the selected Slope Stop B signal to terminate the slope function.

Slope Stop A Signal Selection	Master	Slave
1111	1	1
1110	Slave PWM2 Trigger 2	Master PWM8 Trigger 2
1101	Slave PWM1 Trigger 2	Master PWM7 Trigger 2
1000	Master PWM4 Trigger 2	Slave PWM8 Trigger 2
0111	Master PWM3 Trigger 2	Slave PWM7 Trigger 2
0110	Master PWM2 Trigger 2	Slave PWM6 Trigger 2
0101	Master PWM1 Trigger 2	Slave PWM5 Trigger 2
0100	Master PWM4 Trigger 1	Slave PWM4 Trigger 2
0011	Master PWM3 Trigger 1	Slave PWM3 Trigger 2
0010	Master PWM2 Trigger 1	Slave PWM2 Trigger 2
0001	Master PWM1 Trigger 1	Slave PWM1 Trigger 2
0000	0	0

bit 7-4 **SLPSTOPB<3:0>:** Slope Stop B Signal Select bits

The selected Slope Stop B signal is logically OR'd with the selected Slope Stop A signal to terminate the slope function.

Slope Start B Signal Selection	Master	Slave
1111	1	1
0100	S1CMP3 Out	CMP1 Out
0011	S1CMP2 Out	S1CMP3 Out
0010	S1CMP1 Out	S1CMP2 Out
0001	CMP1 Out	S1CMP1 Out
0000	0	0

bit 3-0 **SLPSTRT<3:0>:** Slope Start Signal Select bits

Slope Start Signal Selection	Master	Slave
1111	1	1
1110	Slave PWM2 Trigger 1	Master PWM2 Trigger 1
1101	Slave PWM1 Trigger 1	Master PWM1 Trigger 1
1000	Master PWM4 Trigger 2	Slave PWM8 Trigger 1
0111	Master PWM3 Trigger 2	Slave PWM7 Trigger 1
0110	Master PWM2 Trigger 2	Slave PWM6 Trigger 1
0101	Master PWM1 Trigger 2	Slave PWM5 Trigger 1
0100	Master PWM4 Trigger 1	Slave PWM4 Trigger 1
0011	Master PWM3 Trigger 1	Slave PWM3 Trigger 1
0010	Master PWM2 Trigger 1	Slave PWM2 Trigger 1
0001	Master PWM1 Trigger 1	Slave PWM1 Trigger 1
0000	0	0

REGISTER 15-3: I2CxSTAT: I2Cx STATUS REGISTER

HSC/R-0	HSC/R-0	HSC/R-0	U-0	U-0	HSC/R/C-0	HSC/R-0	HSC/R-0
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

HS/R/C-0	HS/R/C-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
IWCOL	I2COV	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from Slave
0 = Acknowledge was received from Slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C Master; applicable to Master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^{2}C Slave mode only)
1 = Indicates I^{2}C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^{2}C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a Master or Slave transmit operation
0 = No bus collision has been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^{2}C module is busy; must be cleared in software
0 = No collision

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = No overflow

bit 5 **D/$\overline{\text{A}}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^{2}C Slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^{2}C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

20.0 CURRENT BIAS GENERATOR (CBG)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Current Bias Generator (CBG)"** (DS70005253) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

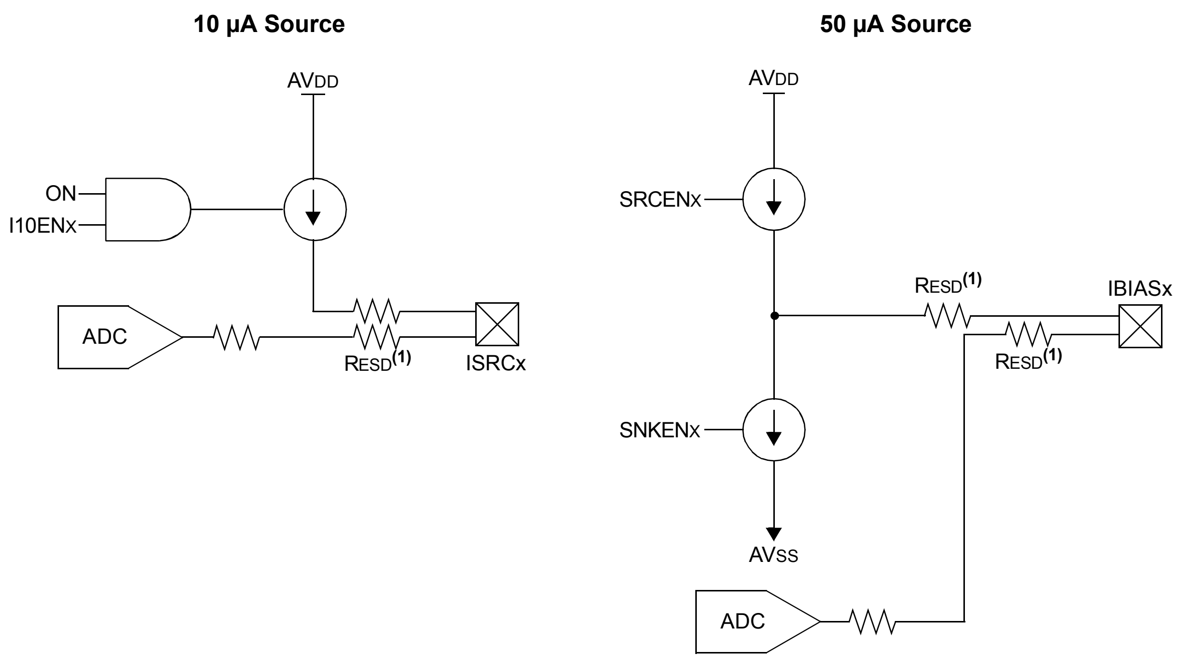
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 3.2 "Master Memory Organization"** in this data sheet for device-specific register and bit information.

The Current Bias Generator (CBG) consists of two classes of current sources: 10 µA and 50 µA sources. The major features of each current source are:

- 10 µA Current Sources:
  - Current sourcing only
  - Up to four independent sources
- 50 µA Current Sources:
  - Selectable current sourcing or sinking
  - Selectable current mirroring for sourcing and sinking

A simplified block diagram of the CBG module is shown in Figure 20-1.

FIGURE 20-1: CONSTANT-CURRENT SOURCE MODULE BLOCK DIAGRAM(2)



Note 1: RESD is typically 300 Ohms; for more information, refer to the device data sheet.

2: In Figure 20-1 only, the ADC analog input is shown for clarity. Each analog peripheral connected to the pin has a separate Electrostatic Discharge (ESD) resistor.

REGISTER 21-13: FDMT CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/PO-1
—	—	—	—	—	—	—	DMTDIS
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-1 **Unimplemented:** Read as ‘1’

bit 0 **DMTDIS:** DMT Disable bit
1 = DMT is disabled
0 = DMT is enabled

21.7 Dual Watchdog Timer (WDT)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Dual Watchdog Timer",** (DS70005250) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: The WDT is identical for both Master core and Slave core. The x is common for both Master core and Slave core (where the x represents the number of the specific module being addressed). The number of WDT modules available on the Master and Slaves is different and they are located in different SFR locations.

3: All associated register names are the same on the Master core and the Slave core. The Slave code will be developed in a separate project in MPLAB® X IDE with the device selection, dsPIC33CH128MP508**S1**, where the **S1** indicates the Slave device.

Table 21-6 shows an overview of the WDT module.

TABLE 21-6: DUAL WDT MODULE OVERVIEW

	Number of WDT Modules	Identical (Modules)
Master Core	1	Yes
Slave Core	1	Yes

The dsPIC33 dual Watchdog Timer (WDT) is described in this section. Refer to Figure 21-2 for a block diagram of the WDT.

The WDT, when enabled, operates from the internal Low-Power RC (LPRC) Oscillator clock source or a selectable clock source in Run mode. The WDT can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. The WDT can be configured in Windowed mode or Non-Windowed mode. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode (Power Save mode). If the WDT expires and issues a device Reset, the WTDO bit of the RCON register (Register 21-37) will be set.

The following are some of the key features of the WDT modules:

- Configuration or Software Controlled
- Separate User-Configurable Time-out Periods for Run and Sleep/Idle
- Can Wake the Device from Sleep or Idle
- User-Selectable Clock Source in Run mode
- Operates from LPRC in Sleep/Idle mode

Note: While executing a clock switch, the WDT will not be reset. It is recommended to reset the WDT prior to executing a clock switch instruction.

REGISTER 21-36: WDTCONH: WATCHDOG TIMER CONTROL REGISTER HIGH

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
WDTCLRKEY<15:8>							
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
WDTCLRKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.