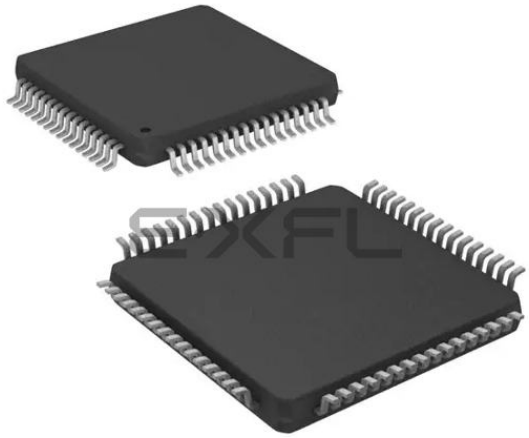
Microchip Technology - DSPIC33CH128MP206-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 34x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp206-i-pt

1.0 DEVICE OVERVIEW

Note 1:	This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 3.2 "Master Memory Organization"** and **Section 4.2 "Slave Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33CH128MP508 Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33CH128MP508 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-2 shows a general block diagram of the cores and peripheral modules of the Master and Slave. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

The Master core and Slave core can operate independently, and can be programmed and debugged separately during the application development. Both processor (Master and Slave) subsystems have their own interrupt controllers, clock generators, ICD, port logic, I/O MUXes and PPS. The device is equivalent to having two complete dsPIC® DSCs on a single die.

The Master core will execute the code from Program Flash Memory (PFM) and the Slave core will operate from Program RAM Memory (PRAM).

Once the code development is complete, the Master Flash will be programmed with the Master code, as well as the Slave code. After a Power-on Reset (POR), the Slave code from Master Flash will be loaded to the PRAM (program memory of the Slave) and the Slave can execute the code independently of the Master. The Master and Slave can communicate with each other using the Master Slave Interface (MSI) peripheral, and can exchange data between them.

Figure 1-1 shows the block diagram of the device operation during a POR and the process of transferring the Slave code from the Master to Slave PRAM.

The I/O ports are shared between the Master and Slave. Table 1 shows the number of peripherals and the shared peripherals that the Master and Slave own. There are Configuration bits in the Flash memory that specify the ownership (Master or Slave) of each device pin.

The default (erased) state of the Flash assigns all of the device pins to the Master.

The two cores (Master and Slave) can both be connected to debug tools, which support independent and simultaneous debugging. When the Slave core or Master core is debugged (non-Dual Debug mode), the S1MCLRx is not used. MCLR is used for programming and debugging both the Master core and the Slave core. S1MCLRx is only used when debugging both the cores at the same time.

In normal operation, the "owner" of a device pin is responsible for full control of that pin; this includes both the digital and analog functionality.

The pin owner's GPIO registers control all aspects of the I/O pad, including the ANSELx, CNPUx, CNPDx, ODCx registers and slew rate control.

Note:	Both the Master and Slave cores can monitor a pin as an input, regardless of pin ownership. Pin ownership is valid only for the output functionality of the port.

3.3.5 NVM CONTROL REGISTERS

REGISTER 3-4: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	U-0	U-0	R/W-0	R/C-0
WR	WREN	WRERR	NVMSIDL(2)	—	—	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	NVMOP3(3,4)	NVMOP2(3,4)	NVMOP1(3,4)	NVMOP0(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Flash voltage regulator goes into Standby mode during Idle mode
- 0 = Flash voltage regulator is active during Idle mode

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **RPDF:** Row Programming Data Format bit
- 1 = Row data to be stored in RAM is in compressed format
- 0 = Row data to be stored in RAM is in uncompressed format

bit 8 **URERR:** Row Programming Data Underrun Error bit
- 1 = Indicates row programming operation has been terminated
- 0 = No data underrun error is detected

bit 7-4 **Unimplemented:** Read as '0'

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (I_{IDLE}), and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.

3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

3.3.6 ECC CONTROL REGISTERS

REGISTER 3-9: ECCCONL: ECC FAULT INJECTION CONFIGURATION REGISTER LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	FLTINMJ
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **FLTINJ:** Fault Injection Sequence Enable bit
1 = Enabled
0 = Disabled

REGISTER 3-10: ECCCONH: ECC FAULT INJECTION CONFIGURATION REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT2PTR<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT1PTR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **FLT2PTR<7:0>:** ECC Fault Injection Bit Pointer 2
11111111-00111000 = No Fault injection occurs
00110111 = Fault injection (bit inversion) occurs on bit 55 of ECC bit order
...
00000001 = Fault injection (bit inversion) occurs on bit 1 of ECC bit order
00000000 = Fault injection (bit inversion) occurs on bit 0 of ECC bit order

bit 7-0 **FLT1PTR<7:0>:** ECC Fault Injection Bit Pointer 1
11111111-00111000 = No Fault injection occurs
00110111 = Fault injection occurs on bit 55 of ECC bit order
...
00000001 = Fault injection occurs on bit 1 of ECC bit order
00000000 = Fault injection occurs on bit 0 of ECC bit order

3.5.3 INTERRUPT RESOURCES

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.5.3.1 Key Resources

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

3.5.4 INTERRUPT CONTROL AND STATUS REGISTERS

The dsPIC33CH128MP508 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

3.5.4.1 INTCON1 through INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

3.5.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

3.5.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

3.5.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of seven priority levels.

3.5.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 3-23. For example, INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

3.5.4.6 Status/Control Registers

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 3-18 through Register 3-22 in the following pages.

REGISTER 3-18: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator A
0 = Trap was not caused by an overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by an overflow of Accumulator B
0 = Trap was not caused by an overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator A
0 = Trap was not caused by a catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by a catastrophic overflow of Accumulator B
0 = Trap was not caused by a catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

REGISTER 3-49: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI11R7	PCI11R6	PCI11R5	PCI11R4	PCI11R3	PCI11R2	PCI11R1	PCI11R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI10R7	PCI10R6	PCI10R5	PCI10R4	PCI10R3	PCI10R2	PCI10R1	PCI10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PCI11R<7:0>:** Assign PWM Input 11 (PCI11) to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **PCI10R<7:0>:** Assign PWM Input 10 (PCI10) to the Corresponding RPn Pin bits
See Table 3-30.

REGISTER 3-50: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIB1R7	QEIB1R6	QEIB1R5	QEIB1R4	QEIB1R3	QEIB1R2	QEIB1R1	QEIB1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIA1R7	QEIA1R6	QEIA1R5	QEIA1R4	QEIA1R3	QEIA1R2	QEIA1R1	QEIA1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **QEIB1R<7:0>:** Assign QEI Input B (QEIB1) to the Corresponding RPn Pin bits
See Table 3-30.

bit 7-0 **QEIA1R<7:0>:** Assign QEI Input A (QEIA1) to the Corresponding RPn Pin bits
See Table 3-30.

3.8 Controller Area Network (CAN FD) Module (Master Only)

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CAN Flexible Data-Rate (FD) Protocol Module"** (DS70005340 in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Only the Master core has a CAN FD module.

Table 3-42 shows an overview of the CAN FD module.

TABLE 3-42: CAN FD MODULE OVERVIEW

	Number of CAN Modules	Identical (Modules)
Master Core	1	NA
Slave Core	None	NA

3.8.1 FEATURES

The CAN FD module has the following features:

General

- Nominal (Arbitration) Bit Rate up to 1 Mbps
- Data Bit Rate up to 8 Mbps
- CAN FD Controller modes:
  - Mixed CAN 2.0B and CAN FD mode
  - CAN 2.0B mode
- Conforms to ISO11898-1:2015

Message FIFOs

- Seven FIFOs, Configurable as Transmit or Receive FIFOs
- One Transmit Queue (TXQ)
- Transmit Event FIFO (TEF) with 32-Bit Timestamp

Message Transmission

- Message Transmission Prioritization:
  - Based on priority bit field, and/or
  - Message with lowest ID gets transmitted first using the TXQ
- Programmable Automatic Retransmission Attempts: Unlimited, Three Attempts or Disabled

Message Reception

- 16 Flexible Filter and Mask Objects.
- Each Object can be Configured to Filter either:
  - Standard ID + first 18 data bits or
  - Extended ID
- 32-Bit Timestamp.
- The CAN FD Bit Stream Processor (BSP) Implements the Medium Access Control of the CAN FD Protocol Described in ISO11898-1:2015. It serializes and deserializes the bit stream, encodes and decodes the CAN FD frames, manages the medium access, Acknowledges frames, and detects and signals errors.
- The TX Handler Prioritizes the Messages that are Requested for Transmission by the Transmit FIFOs. It uses the RAM interface to fetch the transmit data from RAM and provides it to the BSP for transmission.
- The BSP provides Received Messages to the RX Handler. The RX handler uses acceptance filters to filter out messages that shall be stored in the Receive FIFOs. It uses the RAM interface to store received data into RAM.
- Each FIFO can be Configured either as a Transmit or Receive FIFO. The FIFO control keeps track of the FIFO head and tail, and calculates the user address. In a TX FIFO, the user address points to the address in RAM where the data for the next transmit message shall be stored. In an RX FIFO, the user address points to the address in RAM where the data of the next receive message shall be read. The user notifies the FIFO that a message was written to or read from RAM by incrementing the head/tail of the FIFO.
- The Transmit Queue (TXQ) is a Special Transmit FIFO that Transmits the Messages based on the ID of the Messages Stored in the Queue.
- The Transmit Event FIFO (TEF) Stores the Message IDs of the Transmitted Messages.
- A Free-Running Time Base Counter is used to Timestamp Received Messages. Messages in the TEF can also be timestamped.
- The CAN FD Controller module Generates Interrupts when New Messages are Received or when Messages were Transmitted Successfully.

Figure 3-23 shows the CAN FD system block diagram.

REGISTER 3-139: C1FIFOUAHx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) HIGH(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<31:24>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<31:16>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-140: C1FIFOUALx: CAN FIFO USER ADDRESS REGISTER x (x = 1 TO 7) LOW(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOUA<15:0>:** FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-141: C1TEFUAH: CAN TRANSMIT EVENT FIFO USER ADDRESS REGISTER HIGH(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<31:24>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TEFUA<31:16>:** Transmit Event FIFO User Address bits
A read of this register will return the address where the next event is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-142: C1TEFUAL: CAN TRANSMIT EVENT FIFO USER ADDRESS REGISTER LOW(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TEFUA<15:0>:** Transmit Event FIFO User Address bits
A read of this register will return the address where the next event is to be read (FIFO tail).

Note 1: This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-153: C1FLTOBJxH: CAN FILTER OBJECT REGISTER x HIGH (x = 0 TO 15)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EXIDE	SID11	EID17	EID16	EID15	EID14	EID13
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID12	EID11	EID10	EID9	EID8	EID7	EID6	EID5
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **EXIDE:** Extended Identifier Enable bit

If MIDE = 1:

1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses

bit 13 **SID11:** Standard Identifier Filter bit

bit 12-0 **EID<17:5>:** Extended Identifier Filter bits

In DeviceNet™ mode, these are the filter bits for the first two data bytes.

REGISTER 3-154: C1FLTOBJxL: CAN FILTER OBJECT REGISTER x LOW (x = 0 TO 15)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID4	EID3	EID2	EID1	EID0	SID10	SID9	SID8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **EID<4:0>:** Extended Identifier Filter bits

In DeviceNet™ mode, these are the filter bits for the first two data bytes.

bit 10-0 **SID<10:0>:** Standard Identifier Filter bits

TABLE 3-45: PTG COMMAND OPTIONS

bit 3-0	Step Command	OPTION<3:0>	Command Description
	PTGWHI(1) or PTGWLO(1)	0000	PTGI0 (see Table 3-46 for input assignments).
		• • •	• • •
		1111	PTGI15 (see Table 3-46 for input assignments).
	PTGIRQ(1)	0000	Generate PTG Interrupt 0.
		• • •	• • •
		0111	Generate PTG Interrupt 7.
		1000	Reserved; do not use.
		• • •	• • •
		1111	Reserved; do not use.
	PTGTRIG	0000	PTGO0 (see Table 3-47 for output assignments).
		0001	PTGO1 (see Table 3-47 for output assignments).
		• • •	• • •
		1110	PTGO30 (see Table 3-47 for output assignments).
		1111	PTGO31 (see Table 3-47 for output assignments).

Note 1: All reserved commands or options will execute, but they do not have any affect (i.e., execute as a NOP instruction).

4.2.8 INTERFACING PROGRAM AND DATA MEMORY SPACES

The dsPIC33CH128MP508S1 family architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33CH128MP508S1 family devices provides two methods by which Program Space can be accessed during operation:

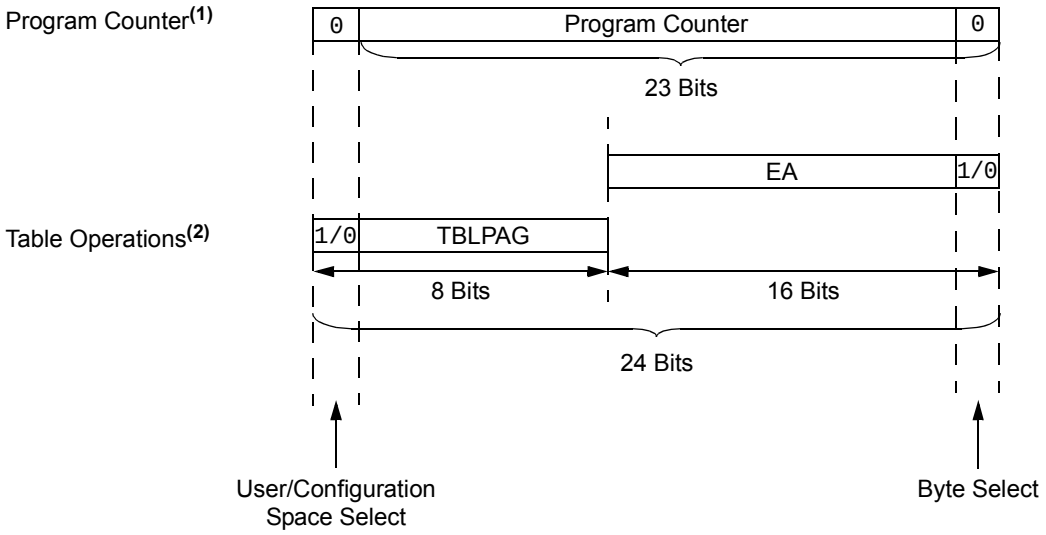
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. However, this method only provides visibility to the lower 16 bits in each location addressed.

TABLE 4-19: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xxx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 4-11: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

REGISTER 4-28: CNPUx: CHANGE NOTIFICATION PULL-UP ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPUx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CNPUx<15:0>:** Change Notification Pull-up Enable for PORTx bits
1 = The pull-up for PORTx[n] is enabled – takes precedence over pull-down selection
0 = The pull-up for PORTx[n] is disabled

REGISTER 4-29: CNPDx: CHANGE NOTIFICATION PULL-DOWN ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNPDx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CNPDx<15:0>:** Change Notification Pull-Down Enable for PORTx bits
1 = The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled)
0 = The pull-down for PORTx[n] is disabled

REGISTER 4-45: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI11R7	PCI11R6	PCI11R5	PCI11R4	PCI11R3	PCI11R2	PCI11R1	PCI11R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCI10R7	PCI10R6	PCI10R5	PCI10R4	PCI10R3	PCI10R2	PCI10R1	PCI10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PCI11R<7:0>:** Assign PWM Input 11 (S1PCI11) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **PCI10R<7:0>:** Assign PWM Input 10 (S1PCI10) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-46: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIB1R7	QEIB1R6	QEIB1R5	QEIB1R4	QEIB1R3	QEIB1R2	QEIB1R1	QEIB1R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIA1R7	QEIA1R6	QEIA1R5	QEIA1R4	QEIA1R3	QEIA1R2	QEIA1R1	QEIA1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **QEIB1R<7:0>:** Assign QEI Input B (S1QEIB1) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **QEIA1R<7:0>:** Assign QEI Input A (S1QEIA1) to the Corresponding S1RPn Pin bits
See Table 4-27.

8.1.6 CHANNEL PRIORITY

Each DMA channel functions independently of the others, but also competes with the others for access to the data and DMA buses. When access collisions occur, the DMA Controller arbitrates between the channels using a user-selectable priority scheme. Two schemes are available:

- Round Robin: When two or more channels collide, the lower numbered channel receives priority on the first collision. On subsequent collisions, the higher numbered channels each receive priority based on their channel number.
- Fixed: When two or more channels collide, the lowest numbered channel always receives priority, regardless of past history; however, any channel being actively processed is not available for an immediate retrigger. If a higher priority channel is continually requesting service, it will be scheduled for service after the next lower priority channel with a pending request.

8.2 Typical Setup

To set up a DMA channel for a basic data transfer:

1. Enable the DMA Controller (DMAEN = 1) and select an appropriate channel priority scheme by setting or clearing PRSSEL.
2. Program DMAH and DMAL with appropriate upper and lower address boundaries for data RAM operations.
3. Select the DMA channel to be used and disable its operation (CHEN = 0).
4. Program the appropriate source and destination addresses for the transaction into the channel's DMASRCn and DMADSTn registers. For PIA mode addressing, use the base address value.
5. Program the DMACNTn register for the number of triggers per transfer (One-Shot or Continuous modes) or the number of words (bytes) to be transferred (Repeated modes).
6. Set or clear the SIZE bit to select the data size.
7. Program the TRMODE<1:0> bits to select the Data Transfer mode.
8. Program the SAMODE<1:0> and DAMODE<1:0> bits to select the addressing mode.
9. Enable the DMA channel by setting CHEN.
10. Enable the trigger source interrupt.

8.3 Peripheral Module Disable

The channels of the DMA Controller can be individually powered down using the Peripheral Module Disable (PMD) registers.

8.4 Registers

The DMA Controller uses a number of registers to control its operation. The number of registers depends on the number of channels implemented for a particular device.

There are always four module-level registers (one control and three buffer/address):

- DMACON: DMA Engine Control Register (Register 8-1)
- DMAH and DMAL: DMA High and Low Address Limit Registers
- DMABUF: DMA Transfer Data Buffer

Each of the DMA channels implements five registers (two control and three buffer/address):

- DMACHn: DMA Channel n Control Register (Register 8-2)
- DMAINTn: DMA Channel n Interrupt Register (Register 8-3)
- DMASRCn: DMA Data Source Address Pointer for Channel n Register
- DMADSTn: DMA Data Destination Source for Channel n Register
- DMACNTn: DMA Transaction Counter for Channel n Register

For dsPIC33CH128MP508 devices, there are a total of 34 registers.

To set up the SPIx module for Audio mode:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   a) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H<15>) = 1.
4. Clear the SPIROV bit (SPIxSTATL<6>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

REGISTER 18-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS4<2:0>			—	DS3<2:0>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS2<2:0>			—	DS1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits (Master)

111 = Master SCCP3 auxiliary out
110 = Master SCCP1 auxiliary out
101 = CLCIND RP pin
100 = Reserved
011 = Master SPI1 Input (SDIx)(1)
010 = Slave Comparator 2 out
001 = Master CLC2 output
000 = Master PWM event

DS4<2:0>: Data Selection MUX 4 Signal Selection bits (Slave)

111 = Slave SCCP3 auxiliary out
110 = Slave SCCP1 auxiliary out
101 = Slave CLCIND
100 = Reserved
011 = Slave SPI1 Input (SDIx)(1)
010 = Slave Comparator 2 out
001 = Slave CLC2 out
000 = Slave PWM event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits (Master)

111 = Master SCCP4 Compare Event Flag (CCP4IF)
110 = Master SCCP3 Compare Event Flag (CCP3IF)
101 = CLC4 out
100 = Master UART1 RX output corresponding to CLCx module
011 = Master SPI1 Output (SDOx) corresponding to CLCx module
010 = Slave Comparator 1 output
001 = Master CLC1 output
000 = Master CLCINC I/O pin

DS3<2:0>: Data Selection MUX 3 Signal Selection bits (Slave)

111 = Slave SCCP4 Compare Event Flag (CCP4IF)
110 = Slave SCCP3 Compare Event Flag (CCP3IF)
101 = Slave CLC4 out
100 = Slave UART1 RX output corresponding to CLCx module
011 = Slave SPI1 Output (SDOx) corresponding to CLCx module
010 = Slave Comparator 1 output
001 = Slave CLC1 output
000 = Slave CLCINC I/O pin

Note 1: Valid only for the SPI with PPS selection.

TABLE 21-2: MASTER CONFIGURATION REGISTERS MAP

Register Name	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSEC	—	AIVTDIS	—	—	—	CSS2	CSS1	CSS0	CWRP	GSS1	GSS0	GWRP	—	BSEN	BSS1	BSS0	BWRP
FBSLIM	—	—	—	—	BSLIM<12:0>												
FSIGN	—	r(2)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
FOSCSEL	—	—	—	—	—	—	—	—	—	IESO	—	—	—	—	FNOSC2	FNOSC1	FNOSC0
FOSC	—	—	—	—	XTBST	XTCFG1	XTCFG0	—	r(1)	FCKSM1	FCKSM0	—	—	—	OSCIOFNC	POSCMD1	POSCMD0
FWDT	—	FWDTEN	SWDTPS4	SWDTPS3	SWDTPS2	SWDTPS1	SWDTPS0	WDTWIN1	WDTWIN0	WINDIS	RCLKSEL1	RCLKSEL0	RWDTPS4	RWDTPS3	RWDTPS2	RWDTPS1	RWDTPS0
FPOR	—	—	—	—	—	—	—	—	—	—	—	r(1)	r(1)	—	—	—	—
FICD	—	—	—	—	—	—	—	—	—	r(1)	—	JTAGEN	—	—	—	ICS1	ICS0
FDMTIVTL	—	DMTIVT<15:0>															
FDMTIVTH	—	DMTIVT<31:16>															
FDMTCNTL	—	DMTCNT<15:0>															
FDMTCNTH	—	DMTCNT<31:16>															
FDMT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMTDIS
FDEVOPT	—	—	—	SPI2PIN	—	—	SMBEN	r(1)	r(1)	r(1)	—	—	ALTI2C2	ALTI2C1	r(1)	—	—
FALTREG	—	—	CTXT4<2:0>			—	CTXT3<2:0>			—	CTXT2<2:0>			—	CTXT1<2:0>		
FMBXM	—	MBXM<15:0>															
FMBXHS1	—	MBXHSD3	MBXHSD2	MBXHSD1	MBXHSD0	MBXHSC3	MBXHSC2	MBXHSC1	MBXHSC0	MBXHSB3	MBXHSB2	MBXHSB1	MBXHSB0	MBXHSA3	MBXHSA2	MBXHSA1	MBXHSA0
FMBXHS2	—	MBXHSH3	MBXHSH2	MBXHSH1	MBXHSH0	MBXHSG3	MBXHSG2	MBXHSG1	MBXHSG0	MBXHSF3	MBXHSF2	MBXHSF1	MBXHSF0	MBXHSE3	MBXHSE2	MBXHSE1	MBXHSE0
FMBXHSEN	—	—	—	—	—	—	—	—	—	HS<H:A>EN							
FCFGPRA0	—	—	—	—	—	—	—	—	—	—	—	—	CPRA<4:0>				
FCFGPRB0	—	CPRB<15:0>															
FCFGPRC0	—	CPRC<15:0>															
FCFGPRD0	—	CPRD<15:0>															
FCFGPRE0	—	CPRE<15:0>															

Legend: — = unimplemented bit, read as '1'; r = reserved bit.

Note 1: Bit is reserved, maintain as '1'.

2: Bit is reserved, maintain as '0'.

TABLE 24-4: OPERATING VOLTAGE SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	3.0	—	3.6	V	
DC12	VDR	**RAM Retention Voltage(2)**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-3V in 3 ms
BO10	VBOR	**BOR Event on VDD Transition** High-to-Low(3)	2.68	2.84	2.99	V	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC and comparators) may have degraded performance.

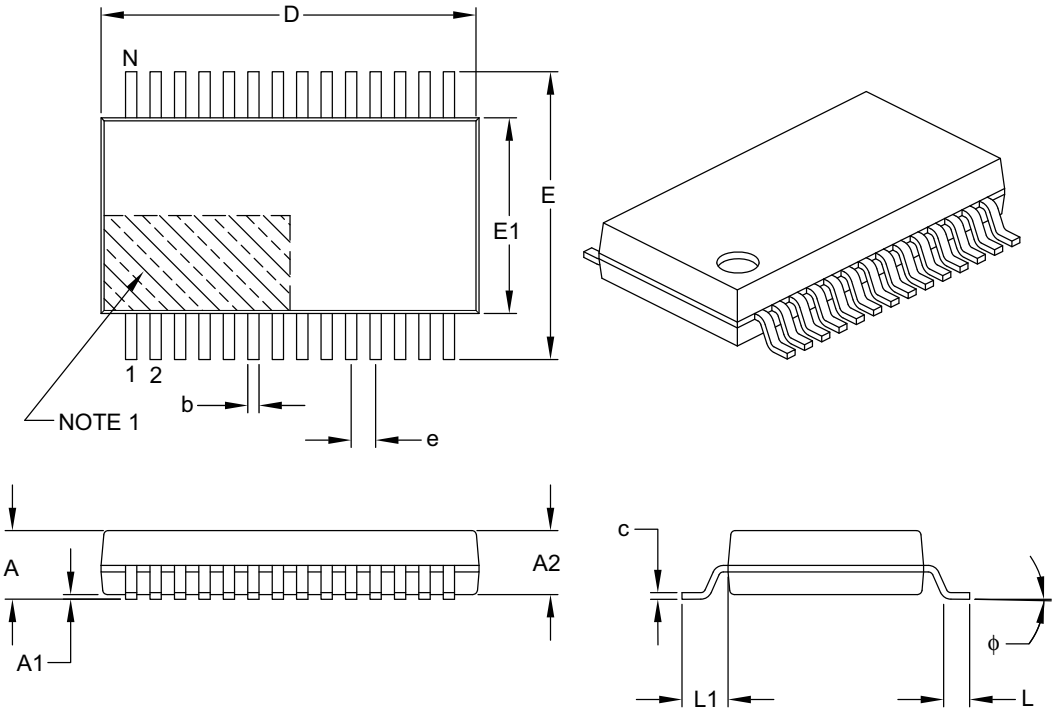
2: This is the limit to which VDD may be lowered and the RAM contents will always be retained.

3: Parameters are characterized but not tested.

25.2 Package Details

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B