Microchip Technology - DSPIC33CH128MP502-E/SS Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 23x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp502-e-ss

TABLE 6: 36-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	$\overline{\text{MCLR}}$	—
4	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
5	AN0/CMP1A/RA0	S1RA0
6	AN1/RA1	S1AN15/S1RA1
7	AN2/RA2	S1AN16/S1RA2
8	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
9	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
10	AVDD	AVDD
11	AVSS	AVSS
12	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
13	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
14	VDD	VDD
15	VSS	VSS
16	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
17	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
18	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
19	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
20	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
21	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
22	VSS	VSS
23	VDD	VDD
24	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
25	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
26	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
27	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
28	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
29	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
30	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
31	VSS	VSS
32	VDD	VDD
33	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
34	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
35	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM7L/S1RB12
36	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

2.1 Basic Connection Requirements

Getting started with the family devices of the dsPIC33CH128MP508 requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins
  regardless if ADC module is not used (see **Section 2.2 “Decoupling Capacitors”**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 “Master Clear (MCLR) Pin”**)
- PGCx/PGDx pins
  used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 “ICSP Pins”**)
- OSCI and OSCO pins
  when an external oscillator source is used (see **Section 2.5 “External Oscillator Pins”**)

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

3.1.7 CPU CONTROL/STATUS REGISTERS

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1)	IPL1(1)	IPL0(1)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Neither Accumulator A or B has overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Neither Accumulator A or B is saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop is in progress
0 = DO loop is not in progress

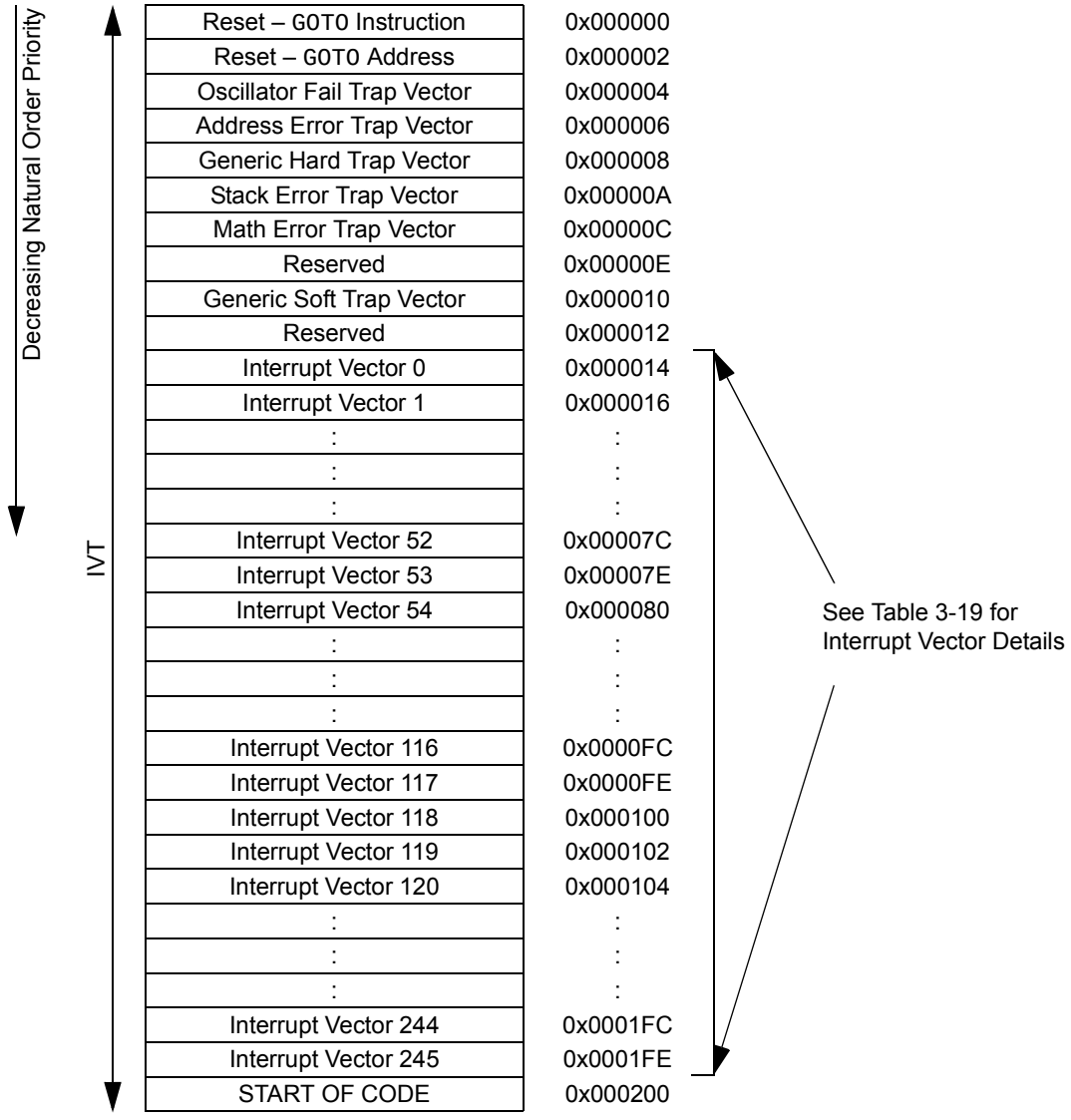
bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

FIGURE 3-17: dsPIC33CH128MP508 FAMILY MASTER INTERRUPT VECTOR TABLE



Note: In Dual Partition modes, each partition has a dedicated Interrupt Vector Table.

REGISTER 3-20: INTCON3: INTERRUPT CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CAN	NAE
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
—	—	—	DOOVR	—	—	—	APLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **CAN:** CAN Address Error Soft Trap Status bit
1 = CAN address error soft trap has occurred
0 = CAN address error soft trap has not occurred

bit 8 **NAE:** NVM Address Error Soft Trap Status bit
1 = NVM address error soft trap has occurred
0 = NVM address error soft trap has not occurred

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **APLL:** Auxiliary PLL Loss of Lock Soft Trap Status bit
1 = APLL lock soft trap has occurred
0 = APLL lock soft trap has not occurred

TABLE 3-33: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
$\overline{U1RTS}$	000010	RPn tied to UART1 Request-to-Send
U2TX	000011	RPn tied to UART2 Transmit
$\overline{U2RTS}$	000100	RPn tied to UART2 Request-to-Send
SDO1	000101	RPn tied to SPI1 Data Output
SCK1	000110	RPn tied to SPI1 Clock Output
$\overline{SS1}$	000111	RPn tied to SPI1 Slave Select
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
REFCLKO	001110	RPn tied to Reference Clock Output
OCM1	001111	RPn tied to SCCP1 Output
OCM2	010000	RPn tied to SCCP2 Output
OCM3	010001	RPn tied to SCCP3 Output
OCM4	010010	RPn tied to SCCP4 Output
OCM5	010011	RPn tied to SCCP5 Output
OCM6	010100	RPn tied to SCCP6 Output
CAN1	010101	RPn tied to CAN1 Output
CMP1	010111	RPn tied to Comparator 1 Output
PWM4H	100010	RPn tied to PWM4H Output
PWM4L	100011	RPn tied to PWM4L Output
PWMEA	100100	RPn tied to PWM Event A Output
PWMEB	100101	RPn tied to PWM Event B Output
QEICMP	100110	RPn tied to QEI Comparator Output
CLC1OUT	101000	RPn tied to CLC1 Output
CLC2OUT	101001	RPn tied to CLC2 Output
OCM7	101010	RPn tied to SCCP7 Output
OCM8	101011	RPn tied to SCCP8 Output
PWMEC	101100	RPn tied to PWM Event C Output
PWMED	101101	RPn tied to PWM Event D Output
PTGTRG24	101110	PTG Trigger Output 24
PTGTRG25	101111	PTG Trigger Output 25
SENT1OUT	110000	RPn tied to SENT1 Output
SENT2OUT	110001	RPn tied to SENT2 Output
CLC3OUT	110010	RPn tied to CLC3 Output
CLC4OUT	110011	RPn tied to CLC4 Output
U1DTR	110100	Data Terminal Ready Output 1
U2DTR	110101	Data Terminal Ready Output 2

REGISTER 3-101: DMTHOLDREG: DMT HOLD REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **UPRCNT<15:0>:** DMTCNTH Register Value when DMTCNTL and DMTCNTH were Last Read bits

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

REGISTER 3-131: C1TXQCONL: CAN TRANSMIT QUEUE CONTROL REGISTER LOW

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	FRESET	TXREQ	UINC
bit 15							bit 8

R-0	U-0	U-0	HS/C-0	U-0	R/W-0	U-0	R/W-0
TXEN	—	—	TXATIE	—	TXQEIE	—	TXQNIE
bit 7							bit 0

Legend:	HS = Hardware Settable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **FRESET:** FIFO Reset bit
- 1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset; user should poll whether this bit is clear before taking any action
- 0 = No effect

bit 9 **TXREQ:** Message Send Request bit
- 1 = Requests sending a message; the bit will automatically clear when all the messages queued in the TXQ are successfully sent
- 0 = Clearing the bit to '0' while set ('1') will request a message abort

bit 8 **UINC:** Increment Head/Tail bit

When this bit is set, the FIFO head will increment by a single message.

bit 7 **TXEN:** TX Enable bit

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **TXATIE:** Transmit Attempts Exhausted Interrupt Enable bit
- 1 = Enables interrupt
- 0 = Disables interrupt

bit 3 **Unimplemented:** Read as '0'

bit 2 **TXQEIE:** Transmit Queue Empty Interrupt Enable bit
- 1 = Interrupt is enabled for TXQ empty
- 0 = Interrupt is disabled for TXQ empty

bit 1 **Unimplemented:** Read as '0'

bit 0 **TXQNIE:** Transmit Queue Not Full Interrupt Enable bit
- 1 = Interrupt is enabled for TXQ not full
- 0 = Interrupt is disabled for TXQ not full

REGISTER 3-167: ADEIEL: ADC EARLY INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EIEN<15:0>:** Early Interrupt Enable for Corresponding Analog Input bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

REGISTER 3-168: ADEIEH: ADC EARLY INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

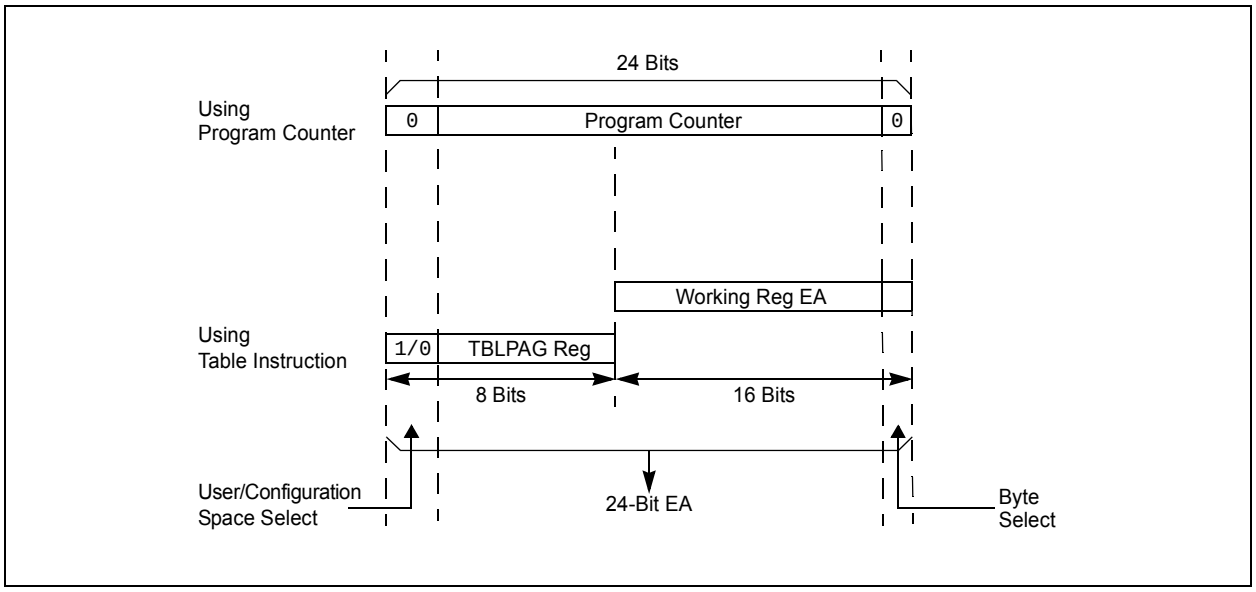
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	EIEN<20:16>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **EIEN<20:16>:** Early Interrupt Enable for Corresponding Analog Input bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

FIGURE 4-13: ADDRESSING FOR TABLE REGISTERS



REGISTER 4-57: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CLCINAR<7:0>:** Assign CLC Input A (S1CLCINA) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 4-58: RPINR46: PERIPHERAL PIN SELECT INPUT REGISTER 46

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINCR7	CLCINCR6	CLCINCR5	CLCINCR4	CLCINCR3	CLCINCR2	CLCINCR1	CLCINCR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CLCINCR<7:0>:** Assign CLC Input C (S1CLCINC) to the Corresponding S1RPn Pin bits
See Table 4-27.

bit 7-0 **CLCINBR<7:0>:** Assign CLC Input B (S1CLCINB) to the Corresponding S1RPn Pin bits
See Table 4-27.

REGISTER 4-64: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to S1RP41 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to S1RP40 Output Pin bits (see Table 4-31 for peripheral function numbers)

REGISTER 4-65: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43	RP43	RP43	RP43	RP43	RP43
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to S1RP43 Output Pin bits (see Table 4-31 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to S1RP42 Output Pin bits (see Table 4-31 for peripheral function numbers)

4.8.1 MODULE DESCRIPTION

The Programmable Gain Amplifiers are used to amplify small voltages (i.e., voltages across burden/shunt resistors) to improve the Signal-to-Noise Ratio (SNR) of the measured signal. The PGAx output voltage can be read by any of the four dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/voltage protection. Figure 4-24 shows a functional block diagram of the PGAx module. Refer to **Section 3.9 "High-Speed, 12-Bit Analog-to-Digital Converter (Master ADC)"** for more interconnection details.

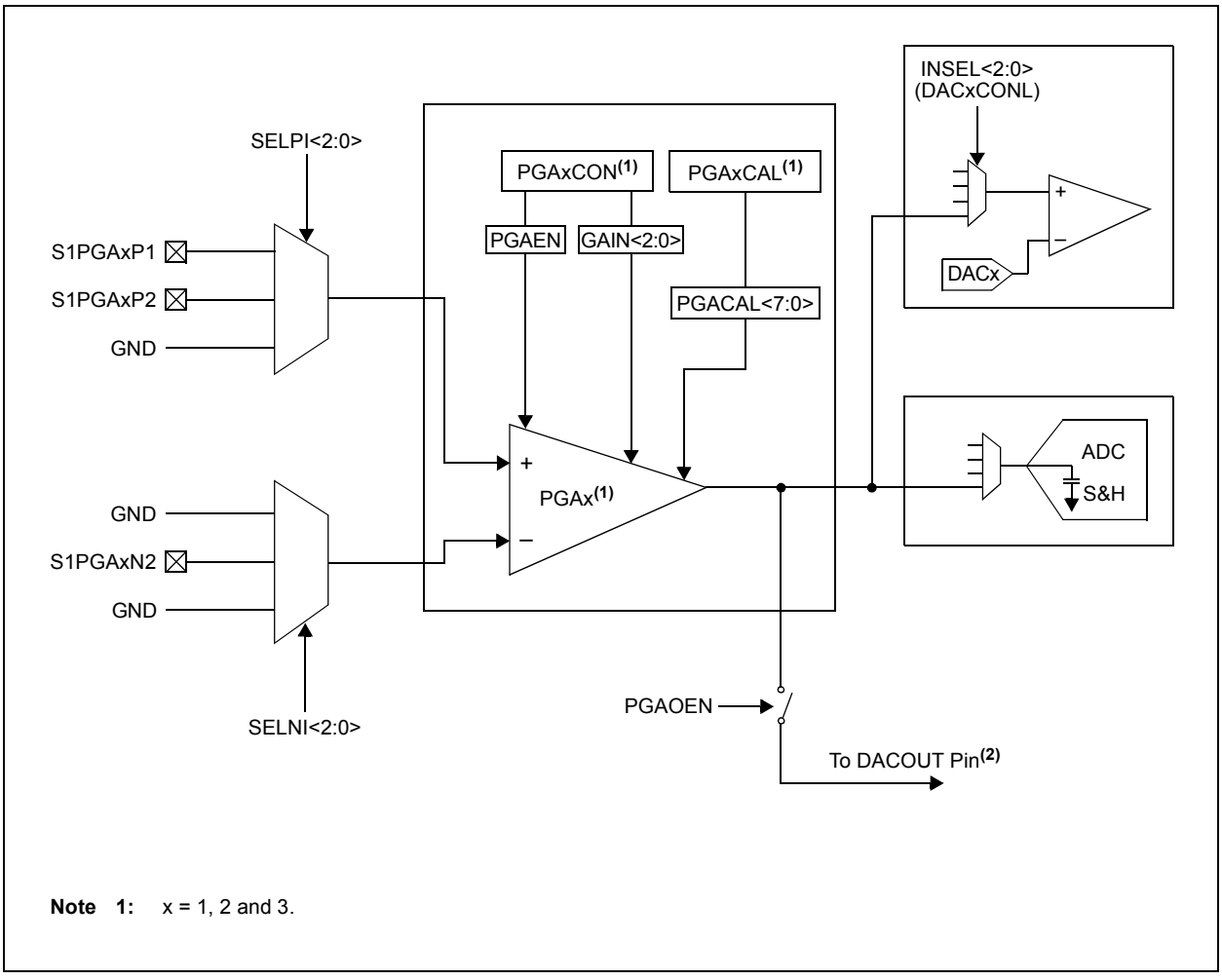
The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are four gains, ranging from 4x to 48x (with a 1.5 gain multiplier). The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of the positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select the ground as the negative input source. To provide an independent ground reference, S1PGAxN2 is available as the negative input source to the PGAx module.

Note 1: Not all PGA positive/negative inputs are available on all devices. Refer to the specific device pinout for available input source pins.

The output voltage of the PGAx module can be connected to the DACOUT pin by setting the PGAOEN bit in the PGAxCON register. When the PGAOEN bit is enabled, the output voltage of PGA1 is connected to DACOUT. There is only one DACOUT pin.

If all three of the DACx output voltages and PGAx output voltages are connected to the DACOUT pin, the resulting output voltage would be a combination of signals. There is no assigned priority between the PGAx module and the DACx module.

FIGURE 4-24: PGAx FUNCTIONAL BLOCK DIAGRAM



Note 1: x = 1, 2 and 3.

REGISTER 5-10: SI1STAT: MSI1 SLAVE STATUS REGISTER

R-0	U-0	R-0	R-0	U-0	U-0	R-0	R-0
MSTRST	—	MSTPWR1	MSTPWR0	—	—	MTSIRQ	STMIACK
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **MSTRST:** Master Reset Status bit
Indicates when the Master is in Reset as the result of any Reset source. Generates a Master Reset event interrupt to the Slave on the leading edge of being set when STMIRQ (SI1CON<9>) = 1.
1 = Master is in Reset
0 = Master is not in Reset

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **MSTPWR<1:0>:** Master Low-Power Operating Mode Status bits
11 = Reserved
10 = Master is in Sleep mode
01 = Master is in Idle mode
00 = Master is not in a Low-Power mode

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **MTSIRQ:** Master interrupt Slave bit
1 = Master has issued an interrupt request to the Slave
0 = Master has not issued a Slave interrupt request

bit 8 **STMIACK:** Master Acknowledgment Status bit
1 = If STMIRQ = 1, Master Acknowledges Slave interrupt request, else protocol error
0 = If STMIRQ = 0, Master has not yet Acknowledged Slave interrupt request, else no Slave to Master interrupt request is pending

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 6-15: PLLDIV: PLL OUTPUT DIVIDER REGISTER (SLAVE)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	VCODIV<1:0>	
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-1
—	POST1DIV<2:0>(1,2)			—	POST2DIV<2:0>(1,2)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-8 **VCODIV<1:0>:** PLL VCO Output Divider Select bits

11 = FVCO
10 = FVCO/2
01 = FVCO/3
00 = FVCO/4

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **POST1DIV<2:0>:** PLL Output Divider #1 Ratio bits(1,2)

POST1DIV<2:0> can have a valid value, from 1 to 7 (POST1DIVx value should be greater than or equal to the POST2DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **POST2DIV<2:0>:** PLL Output Divider #2 Ratio bits(1,2)

POST2DIV<2:0> can have a valid value, from 1 to 7 (POST2DIVx value should be less than or equal to the POST1DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

Note 1: The POST1DIVx and POST2DIVx divider values must not be changed while the PLL is operating.

2: The default values for POST1DIVx and POST2DIVx are 4 and 1, respectively, yielding a 150 MHz system source clock.

REGISTER 10-5: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	—	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active low
0 = Output pin polarity is active high

bit 4 **Unimplemented:** Read as '0'

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in high-impedance state when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

REGISTER 12-7: POSxHLDL: POSITION x COUNTER HOLD REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSHLD<15:0>:** Position Counter Hold for Reading/Writing Position x Counter Register (POSxCNT) bits

REGISTER 12-8: POSxHLDH: POSITION x COUNTER HOLD REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSHLD<31:16>:** Position Counter Hold for Reading/Writing Position x Counter Register (POSxCNT) bits

REGISTER 15-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 8 **SMEN:** SMBus Input Levels Enable bit
1 = Enables input logic so thresholds are compliant with the SMBus specification
0 = Disables SMBus-specific inputs

bit 7 **GCEN:** General Call Enable bit (I^2C Slave mode only)
1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6 **STREN:** SCLx Clock Stretch Enable bit
In I^2C Slave mode only; used in conjunction with the SCLREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5 **ACKDT:** Acknowledge Data bit
In I^2C Master mode during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Slave mode when AHEN = 1 or DHEN = 1. The value that the Slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
In I^2C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (I^2C Master mode only)
1 = Enables Receive mode for I^2C; automatically cleared by hardware at end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (I^2C Master mode only)
1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1 **RSEN:** Restart Condition Enable bit (I^2C Master mode only)
1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0 **SEN:** Start Condition Enable bit (I^2C Master mode only)
1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of Slave transmission; automatically cleared to '0' at the end of Slave reception.
2: Automatically cleared to '0' at the beginning of Slave transmission.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70000157).

TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS dsPIC33CH128MP508 Family	
			Master	Slave
—	3.0V to 3.6V	-40°C to +85°C	90	100
	3.0V to 3.6V	-40°C to +125°C	90	100

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 80-Pin TQFP 12x12x1 mm	θJA	50.67	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP 10x10x1 mm	θJA	45.7	—	°C/W	**1**
Package Thermal Resistance, 64-Pin QFN 9x9 mm	θJA	18.7	—	°C/W	**1**
Package Thermal Resistance, 48-Pin TQFP 7x7 mm	θJA	62.76	—	°C/W	**1**
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θJA	27.6	—	°C/W	**1**
Package Thermal Resistance, 36-Pin UQFN 5x5 mm	θJA	29.2	—	°C/W	**1**
Package Thermal Resistance, 28-Pin UQFN 6x6 mm	θJA	22.41	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SSOP 5.30 mm	θJA	52.84	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.