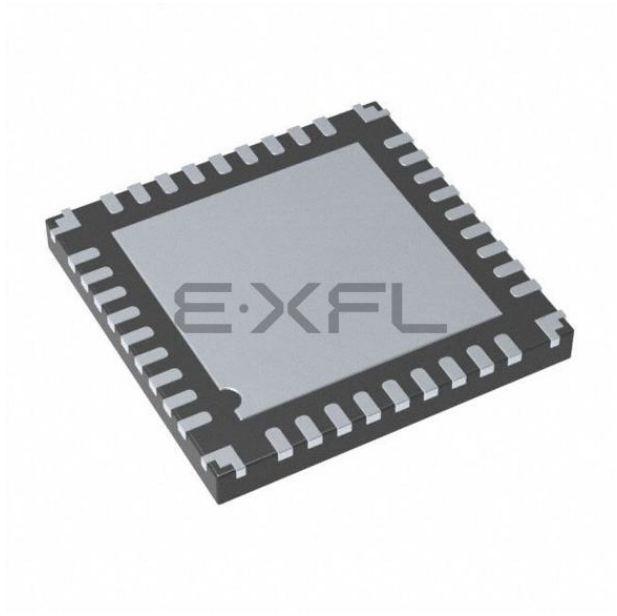

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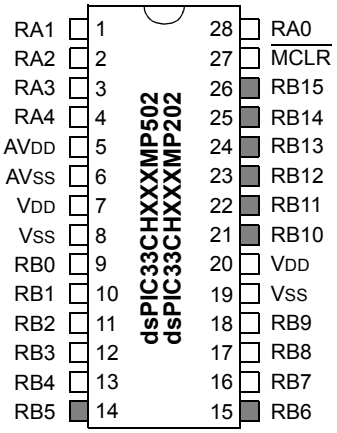
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit Dual-Core
Speed	180MHz, 200MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	27
Program Memory Size	152KB (152K x 8)
Program Memory Type	FLASH, PRAM
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 31x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFQFN Exposed Pad
Supplier Device Package	36-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ch128mp503t-i-m5

Pin Diagrams

28-Pin SSOP(1)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

TABLE 4: 28-PIN SSOP

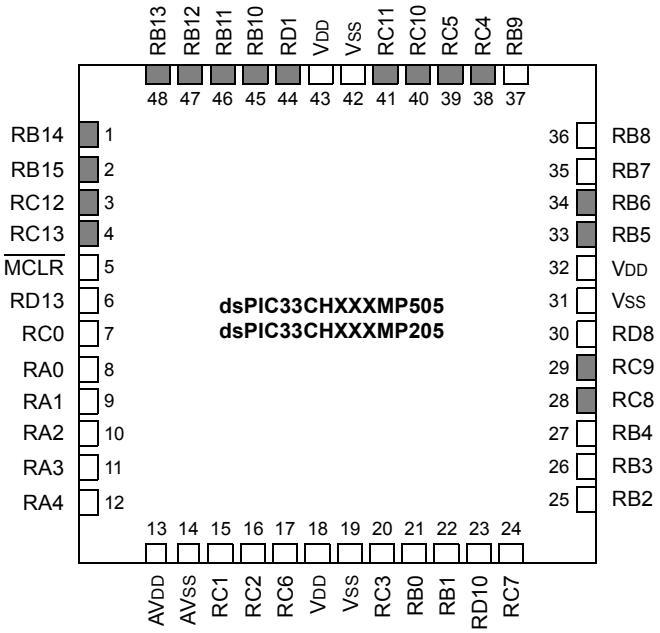
Pin #	Master Core	Slave Core
1	AN1/RA1	S1AN15/S1RA1
2	AN2/RA2	S1AN16/S1RA2
3	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
4	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR}}$3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
5	AVDD	AVDD
6	AVSS	AVSS
7	VDD	VDD
8	VSS	VSS
9	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
10	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1(1)	S1AN4/**S1RP33**/S1RB1
11	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
12	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
13	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
14	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
15	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
16	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
17	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
18	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
19	VSS	VSS
20	VDD	VDD
21	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
22	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
23	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM2H/S1RB12
24	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1PWM2L/S1RB13
25	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
26	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
27	$\overline{\text{MCLR}}$	—
28	AN0/CMP1A/RA0	S1RA0

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Note 1: At device power-up (POR), a pulse with an amplitude around 2V and a duration greater than 500 µs may be observed on this device pin, independent of pull-down resistors. It is recommended not to use this pin as an output driver unless the circuit being driven can endure this active duration.

Pin Diagrams (Continued)

48-Pin QFN/TQFP/UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

3.2.5 SFR MAPS

The following tables show dsPIC33CH128MP508 family Master SFR names, addresses and Reset values. These tables contain all registers applicable to the dsPIC33CH128MP508 family. Not all registers are present on all device variants. Refer to Table 1 and Table 2 for peripheral availability. Table 4-25 shows port availability for the different package options.

TABLE 3-4: MASTER SFR BLOCK 000h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Core			MODCON	046	00--000000000000	**CRC**		
WREG0	000	0000000000000000	XMODSRT	048	xxxxxxxxxxxxxx0	CRCCONL	0B0	0-000000010000--
WREG1	002	0000000000000000	XMODEND	04A	xxxxxxxxxxxxxx1	CRCCONH	0B2	---00000---00000
WREG2	004	0000000000000000	YMODSRT	04C	xxxxxxxxxxxxxx0	CRCXORL	0B4	000000000000000-
WREG3	006	0000000000000000	YMODEND	04E	xxxxxxxxxxxxxx1	CRCXORH	0B6	0000000000000000
WREG4	008	0000000000000000	XBREV	050	0xxxxxxxxxxxxxx	CRCDATL	0B8	0000000000000000
WREG5	00A	0000000000000000	DISICNT	052	xxxxxxxxxxxxx00	CRCDATH	0BA	0000000000000000
WREG6	00C	0000000000000000	TBLPAG	054	--------00000000	CRCWDATL	0BC	0000000000000000
WREG7	00E	0000000000000000	YPAG	056	--------00000001	CRCWDATH	0BE	0000000000000000
WREG8	010	0000000000000000	MSTRPR	058	----------00---0	**CLC**		
WREG9	012	0000000000000000	CTXTSTAT	05A	0000000000000000	CLC1CONL	0C0	0-0-00--000--000
WREG10	014	0000000000000000	DMTCON	05C	0000000000000000	CLC1CONH	0C2	------------0000
WREG11	016	0000000000000000	DMTPRECLR	060	0000000000000000	CLC1SEL	0C4	-000-000-000-000
WREG12	018	0000000000000000	DMTCLR	064	0000000000000000	CLC1GLSL	0C8	0000000000000000
WREG13	01A	0000000000000000	DMTSTAT	068	0000000000000000	CLC1GLSH	0CA	0000000000000000
WREG14	01C	0000000000000000	DMTCNTL	06C	0000000000000000	CLC2CONL	0CC	0-0-00--000--000
WREG15	01E	0000100000000000	DMTCNTH	06E	0000000000000000	CLC2CONH	0CE	------------0000
SPLIM	020	xxxxxxxxxxxxxxx	DMTHOLDREG	070	0000000000000000	CLC2SEL	0D0	-000-000-000-000
ACCAL	022	xxxxxxxxxxxxxxx	DMTPSCNTL	074	0000000000000000	CLC2GLSL	0D4	0000000000000000
ACCAH	024	xxxxxxxxxxxxxxx	DMTPSCNTH	076	0000000000000000	CLC2GLSH	0D6	0000000000000000
ACCAU	026	xxxxxxxxxxxxxxx	DMTPSINTVL	078	0000000000000000	CLC3CONL	0D8	0-0-00--000--000
ACCBL	028	xxxxxxxxxxxxxxx	DMTPSINTVH	07A	0000000000000000	CLC3CONH	0DA	------------0000
ACCBH	02A	xxxxxxxxxxxxxxx	**SENT**			CLC3SEL	0DC	-000-000-000-000
ACCBU	02C	xxxxxxxxxxxxxxx	SENT1CON1	080	0000000000000000	CLC3GLSL	0E0	0000000000000000
PCL	02E	0000000000000000	SENT1CON2	084	0000000000000000	CLC3GLSH	0E2	0000000000000000
PCH	030	--------00000000	SENT1CON3	088	0000000000000000	CLC4CONL	0E4	0-0-00--000--000
DSRPAG	032	------0000000001	SENT1STAT	08C	0000000000000000	CLC4CONH	0E6	------------0000
DSWPAG	034	-----00000000001	SENT1SYNC	090	0000000000000000	CLC4SEL	0E8	-000-000-000-000
RCOUNT	036	xxxxxxxxxxxxxxx	SENT1DATL	094	0000000000000000	CLC4GLSL	0EC	0000000000000000
DCOUNT	038	xxxxxxxxxxxxxxx	SENT1DATH	096	0000000000000000	CLC4GLSH	0EE	0000000000000000
DOSTART	03A	1111111111111111	SENT2CON1	098	0000000000000000	ECCCONL	0F0	---------------0
DOSTARTL	03A	1111111111111110	SENT2CON2	09C	0000000000000000	ECCCONH	0F2	0000000000000000
DOSTARTH	03C	0000000011111111	SENT2CON3	0A0	0000000000000000	ECCADDRL	0F4	0000000000000000
DOENDL	03E	xxxxxxxxxxxxxx0	SENT2STAT	0A4	0000000000000000	ECCADDRH	0F6	0000000000000000
DOENDH	040	---------xxxxxxx	SENT2SYNC	0A8	0000000000000000	ECCSTATL	0F8	0000000000000000
SR	042	0000000000000000	SENT2DATL	0AC	0000000000000000	ECCSTATH	0FA	------0000000000
CORCON	044	x-xx000000100000	SENT2DATH	0AE	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address and Reset values are in hexadecimal and binary, respectively.
Note 1: SFR shown is for the superset 80-pin device.

REGISTER 3-136: C1TEFCONH: CAN TRANSMIT EVENT FIFO CONTROL REGISTER HIGH

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSIZE<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FSIZE<4:0>:** FIFO Size bits(1)

11111 = FIFO is 32 messages deep
...
00010 = FIFO is 3 messages deep
00001 = FIFO is 2 messages deep
00000 = FIFO is 1 message deep

bit 7-0 **Unimplemented:** Read as '0'

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 3-195: PTGQPTR: PTG STEP QUEUE POINTER REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the Step queue.

Note 1: These bits are read only when the module is executing step commands.

REGISTER 3-196: PTGQUEn: PTG STEP QUEUE n POINTER REGISTER (n = 0-15)(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP2n+1<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP2n<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP2n+1<7:0>:** PTG Command 4n+1 bits
A queue location for storage of the STEP2n+1 command byte, where 'n' is from PTGQUEn.

bit **STEP2n<7:0>:** PTG Command 4n+2 bits
A queue location for storage of the STEP2n command byte, where 'n' are the odd numbered Step Queue Pointers.

Note 1: These bits are read-only when the module is executing Step commands.
2: Refer to Table 3-1 for the Step command encoding.

TABLE 4-31: OUTPUT SELECTION FOR REMAPPABLE PINS (S1RPn)

Function	RPnR<5:0>	Output Name
Default PORT	000000	S1RPn tied to Default Pin
S1U1TX	000001	S1RPn tied to UART1 Transmit
$\overline{\text{S1U1RTS}}$	000010	S1RPn tied to UART1 Request-to-Send
S1SDO1	000101	S1RPn tied to SPI1 Data Output
S1SCK1OUT	000110	S1RPn tied to SPI1 Clock Output
$\overline{\text{S1SS1OUT}}$	000111	S1RPn tied to SPI1 Slave Select
S1REFCLKO	001110	S1RPn tied to Reference Clock Output
S1OCM1	001111	S1RPn tied to SCCP1 Output
S1OCM2	010000	S1RPn tied to SCCP2 Output
S1OCM3	010001	S1RPn tied to SCCP3 Output
S1OCM4	010010	S1RPn tied to SCCP4 Output
S1CMP1	010111	S1RPn tied to Comparator 1 Output
S1CMP2	011000	S1RPn tied to Comparator 2 Output
S1CMP3	011001	S1RPn tied to Comparator 3 Output
S1PWMH4	100010	S1RPn tied to PWM4H Output
S1PWML4	100011	S1RPn tied to PWM4L Output
S1PWMEA	100100	S1RPn tied to PWM Event A Output
S1PWMEB	100101	S1RPn tied to PWM Event B Output
S1QEICMP1	100110	S1RPn tied to QEI Comparator Output
S1CLC1OUT	101000	S1RPn tied to CLC1 Output
S1CLC2OUT	101001	S1RPn tied to CLC2 Output
S1PWMEC	101100	S1RPn tied to PWM Event C Output
S1PWMED	101101	S1RPn tied to PWM Event D Output
MPTGTRG1	101110	Master PTG24 Output
MPTGTRG2	101111	Master PTG25 Output
S1CLC3OUT	110010	S1RPn tied to CLC3 Output

TABLE 4-32: SLAVE PPS OUTPUT CONTROL REGISTERS

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPOR0	—	—	RP33R5	RP33R4	RP33R3	RP33R2	RP33R1	RP33R0	—	—	RP32R5	RP32R4	RP32R3	RP32R2	RP32R1	RP32R0
RPOR1	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP34R5	RP34R4	RP34R3	RP34R2	RP34R1	RP34R0
RPOR2	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0
RPOR3	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0
RPOR4	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
RPOR5	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
RPOR6	—	—	RP45R5	RP45R4	RP45R3	RP45R2	RP45R1	RP45R0	—	—	RP44R5	RP44R4	RP44R3	RP44R2	RP44R1	RP44R0
RPOR7	—	—	RP47R5	RP47R4	RP47R3	RP47R2	RP47R1	RP47R0	—	—	RP46R5	RP46R4	RP46R3	RP46R2	RP46R1	RP46R0
RPOR8	—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0
RPOR9	—	—	RP51R5	RP51R4	RP51R3	RP51R2	RP51R1	RP51R0	—	—	RP50R5	RP50R4	RP50R3	RP50R2	RP50R1	RP50R0
RPOR10	—	—	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0	—	—	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
RPOR11	—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
RPOR12	—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
RPOR13	—	—	RP59R5	RP59R4	RP59R3	RP59R2	RP59R1	RP59R0	—	—	RP58R5	RP58R4	RP58R3	RP58R2	RP58R1	RP58R0
RPOR14	—	—	RP61R5	RP61R4	RP61R3	RP61R2	RP61R1	RP61R0	—	—	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
RPOR15	—	—	RP63R5	RP63R4	RP63R3	RP63R2	RP63R1	RP63R0	—	—	RP62R5	RP62R4	RP62R3	RP62R2	RP62R1	RP62R0
RPOR16	—	—	RP65R5	RP65R4	RP65R3	RP65R2	RP65R1	RP65R0	—	—	RP64R5	RP64R4	RP64R3	RP64R2	RP64R1	RP64R0
RPOR17	—	—	RP67R5	RP67R4	RP67R3	RP67R2	RP67R1	RP67R0	—	—	RP66R5	RP66R4	RP66R3	RP66R2	RP66R1	RP66R0
RPOR18	—	—	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0	—	—	RP68R5	RP68R4	RP68R3	RP68R2	RP68R1	RP68R0
RPOR19	—	—	RP71R5	RP71R4	RP71R3	RP71R2	RP71R1	RP71R0	—	—	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0
RPOR20(1)	—	—	RP171R5	RP171R4	RP171R3	RP177R2	RP171R1	RP171R0	—	—	RP170R5	RP170R4	RP170R3	RP170R2	RP170R1	RP170R0
RPOR21(1)	—	—	RP173R5	RP173R4	RP173R3	RP173R2	RP173R1	RP173R0	—	—	RP172R5	RP172R4	RP172R3	RP172R2	RP172R1	RP172R0
RPOR22(1)	—	—	RP175R5	RP175R4	RP175R3	RP175R2	RP175R1	RP175R0	—	—	RP174R5	RP174R4	RP174R3	RP174R2	RP174R1	RP174R0

Note 1: The RPOR20, RPOR21 and RPOR22 registers are for virtual output pins.

REGISTER 4-93: ADCORExL: DEDICATED ADC CORE x CONTROL REGISTER LOW (x = 0 TO 1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SAMC<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SAMC<9:0>:** Dedicated ADC Core x Conversion Delay Selection bits

These bits determine the time between the trigger event and the start of conversion in the number of the Core Clock Periods (TADCORE). During this time, the ADC Core x still continues sampling. This feature is enabled by the SAMCxEN bits in the ADCON4L register.

1111111111 = 1025 TADCORE
...
0000000001 = 3 TADCORE
0000000000 = 2 TADCORE

REGISTER 5-3: MSI1KEY: MSI1 MASTER INTERLOCK KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
MSI1KEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **MSI1KEY<7:0>:** MSI1 Key bits
The MSI1KEYx bits are monitored for specific write values.

REGISTER 5-4: MSI1MBXS: MSI1 MASTER MAILBOX DATA TRANSFER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRDY<H:A>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **DTRDY<H:A>:** Data Ready Status bits

1 = Data transmitter has indicated that data is available to be read by data receiver in MSI1MBXnD (DTRDYx is automatically set by a data transmitter processor write to assigned MSI1MBXnD); Meaning when configured as a:
- Transmitter: Data is written. Waiting for receiver to read.
- Receiver: New data is ready to read.

0 = No data is available to be read by receiver in MSI1MBXnD (or the handshake protocol logic block is disabled)

REGISTER 7-11: PMD2: SLAVE PERIPHERAL MODULE DISABLE 2 CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CCP4MD	CCP3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **CCP4MD:** SCCP4 Module Disable bit
1 = SCCP4 module is disabled
0 = SCCP4 module is enabled

bit 2 **CCP3MD:** SCCP3 Module Disable bit
1 = SCCP3 module is disabled
0 = SCCP3 module is enabled

bit 1 **CCP2MD:** SCCP2 Module Disable bit
1 = SCCP2 module is disabled
0 = SCCP2 module is enabled

bit 0 **CCP1MD:** SCCP1 Module Disable bit
1 = SCCP1 module is disabled
0 = SCCP1 module is enabled

TABLE 10-6: SYNCHRONIZATION SOURCES (MASTER)

SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	Module's Own Timer Sync Out
00010	Sync Output SCCP1
00011	Sync Output SCCP2
00100	Sync Output SCCP3
00101	Sync Output SCCP4
00110	Sync Output SCCP5
00111	Sync Output SCCP6
01000	Sync Output SCCP7
01001	INT0
01010	INT1
01011	INT2
01100-01111	Reserved
10000	Master CLC1 Output
10001	Master CLC2 Output
10010	Slave CLC1 Output
10011	Slave CLC2 Output
10100-10110	Reserved
10111	Comparator 1 Output
11000	Slave Comparator 1 Output
11001	Slave Comparator 2 Output
11010	Slave Comparator 3 Output
11011-11110	Reserved
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

REGISTER 12-15: INTXxHLDL: INDEX x COUNTER HOLD REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTXHLD<15:0>:** Hold for Reading/Writing Interval Timer Value Register (INDXCNT) bits

REGISTER 12-16: INTXxHLDH: INDEX x COUNTER HOLD REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTHLD<31:16>:** Hold for Reading/Writing Interval Timer Value Register (INDXCNT) bits

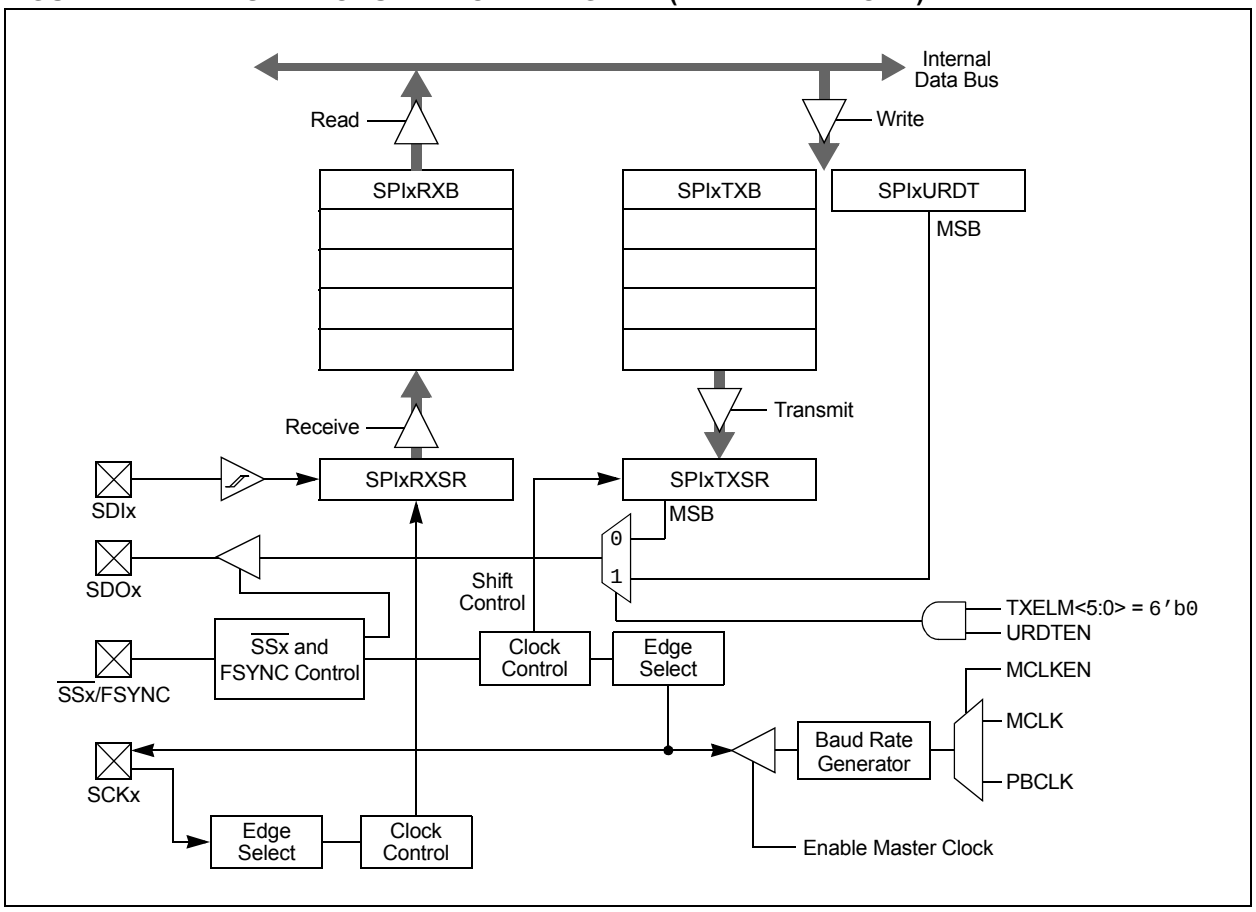
To set up the SPIx module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

FIGURE 14-2: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



REGISTER 21-5: FOSC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	U-1	r-1
—	—	—	XTBST	XTCFG1	XTCFG0	—	—
bit 15							bit 8

R/PO-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	—	—	—	OSCIOFNC(1)	POSCMD1	POSCMD0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as '1'

bit 12 **XTBST:** Oscillator Kick-Start Programmability bit
1 = Boosts the kick-start
0 = Default kick-start

bit 11-10 **XTCFG<1:0>:** Crystal Oscillator Drive Select bits
Current gain programmability for oscillator (output drive).
11 = Gain3 (use for 24-32 MHz crystals)
10 = Gain2 (use for 16-24 MHz crystals)
01 = Gain1 (use for 8-16 MHz crystals)
00 = Gain0 (use for 4-8 MHz crystals)

bit 9 **Unimplemented:** Read as '1'

bit 8 **Reserved:** Maintain as '1'

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5-3 **Unimplemented:** Read as '1'

bit 2 **OSCIOFNC:** OSCO Pin Function bit (except in XT and HS modes)(1)
1 = OSCO is the clock output
0 = OSCO is the general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Select bits
11 = Primary Oscillator is disabled
10 = HS Crystal Oscillator mode (10 MHz-32 MHz)
01 = XT Crystal Oscillator mode (3.5 MHz-10 MHz)
00 = EC (External Clock) mode

Note 1: The OSCO pin function is determined by the S1OSCIOFNC Configuration bit. If both the Master core OSCIOFNC and Slave core S1OSCIOFNC bits are set, the Master core OSCIOFNC bit has priority.

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS dsPIC33CH128MP508 Family	
			Master	Slave
—	3.0V to 3.6V	-40°C to +85°C	90	100
	3.0V to 3.6V	-40°C to +125°C	90	100

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 80-Pin TQFP 12x12x1 mm	θJA	50.67	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP 10x10x1 mm	θJA	45.7	—	°C/W	**1**
Package Thermal Resistance, 64-Pin QFN 9x9 mm	θJA	18.7	—	°C/W	**1**
Package Thermal Resistance, 48-Pin TQFP 7x7 mm	θJA	62.76	—	°C/W	**1**
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θJA	27.6	—	°C/W	**1**
Package Thermal Resistance, 36-Pin UQFN 5x5 mm	θJA	29.2	—	°C/W	**1**
Package Thermal Resistance, 28-Pin UQFN 6x6 mm	θJA	22.41	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SSOP 5.30 mm	θJA	52.84	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 24-13: DC CHARACTERISTICS: PWM DELTA CURRENT(1,2,3)

DC CHARACTERISTICS	Master and Slave		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
DC100	6	8	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 500 MHz), AVCO = 1000 MHz, PLLFBD = 125, APLLDIV = 2
	6	6.7	mA	+25°C, 3.3V	
	6.3	8	mA	+125°C, 3.3V	
DC101	4.9	6	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 400 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 1
	4.9	5.5	mA	+25°C, 3.3V	
	4.9	5.6	mA	+125°C, 3.3V	
DC102	2.6	3.4	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 200 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 2
	2.7	3	mA	+25°C, 3.3V	
	2.7	3.2	mA	+125°C, 3.3V	
DC103	1.5	2.9	mA	-40°C, 3.3V	PWM Output 500 MHz, PWM Input (AFPLLO = 100 MHz), AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 4
	1.5	2.1	mA	+25°C, 3.3V	
	1.5	2.2	mA	+125°C, 3.3V	

Note 1: The APLL current is not included. The APLL current will be the same if more than one PWM or all eight PWMs are running.

2: Delta current is for the one instance of PWM running.

3: PWM configured for Low-Resolution mode. All parameters are characterized but not tested during manufacturing.

TABLE 24-14: DC CHARACTERISTICS: APLL DELTA CURRENT

DC CHARACTERISTICS	Master or Slave(2)		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions(1)**	
DC110	—	9.4	mA	-40°C.,3.3V	AFPLLO @ 500 MHz, AVCO = 1000 MHz, PLLFBD = 125, APLLDIV = 2
	7.2	9.4	mA	+25°C,3.3V	
	—	18	mA	+125°C,3.3V	
DC111	—	5.7	mA	-40°C.,3.3V	AFPLLO @ 400 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 1
	5	5.8	mA	+25°C,3.3V	
	—	14	mA	+125°C,3.3V	
DC112	—	4.7	mA	-40°C.,3.3V	AFPLLO @ 200 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 2
	2.9	4.7	mA	+25°C,3.3V	
	—	14	mA	+125°C,3.3V	
DC113	—	4	mA	-40°C.,3.3V	AFPLLO @ 100 MHz, AVCO = 400 MHz, PLLFBD = 50, APLLDIV = 4
	2.3	4	mA	+25°C,3.3V	
	—	12	mA	+125°C,3.3V	

Note 1: The APLL current will be the same if more than one PWM or DAC is run to the APLL clock. All parameters are characterized but not tested during manufacturing.

2: Current is for the APLL for the Master or Slave, not the combined current.

FIGURE 24-12: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 0) TIMING CHARACTERISTICS

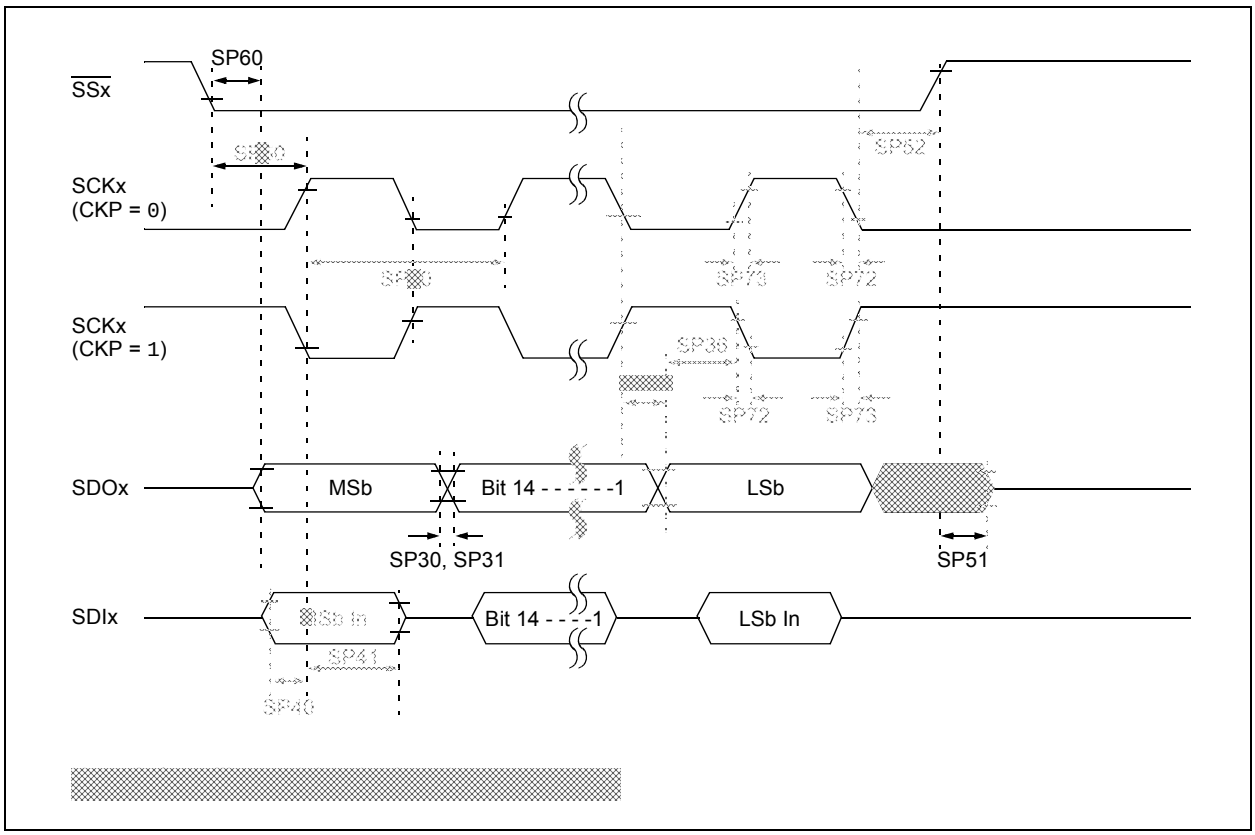
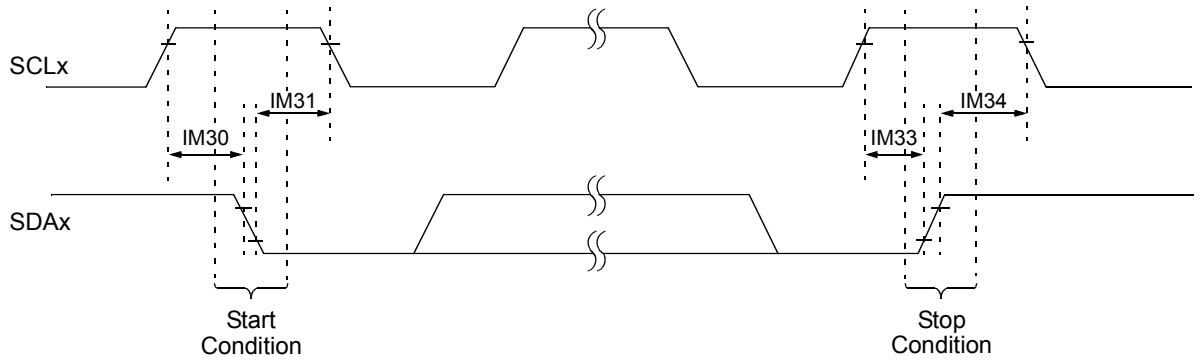
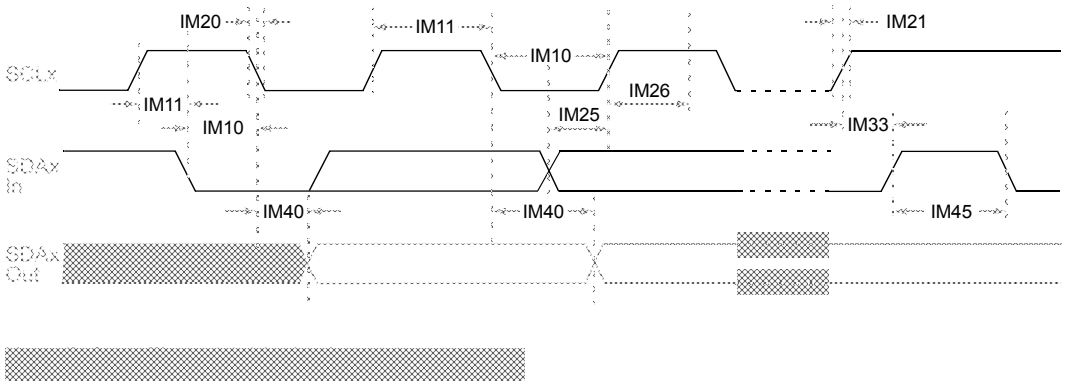


FIGURE 24-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



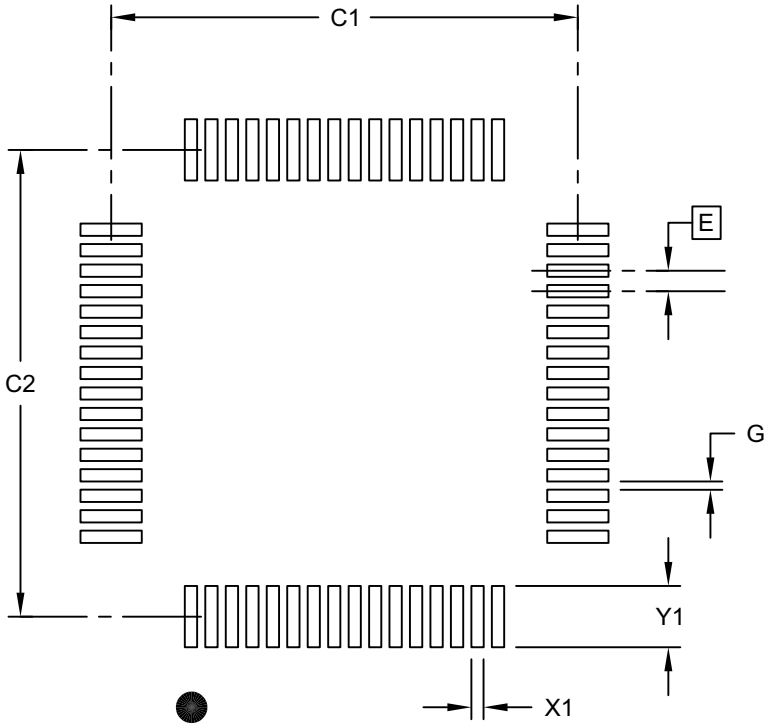
Note: Refer to Figure 24-1 for load conditions.

FIGURE 24-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1